TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Unter http://www.FlowCAD.de/TrainingKontakt.php können Sie sich zum Training anmelden.

Course Title	**Allegro FPGA System Planner**
Course Category	**System Interconnect Design – Allegro & OrCAD**
Duration	**2 Days**

Course Description

In the Allegro® FPGA System Planner (FSP) course, you learn to define your FPGA system and synthesize the connections in your design. You generate a schematic and PCB Editor database, so the FPGA I/O assignments can be optimized in the board environment.

Learning Objectives

After completing this course, you will be able to:

- Identify how data flows from the FPGA System Planner (FSP) to the schematic and PCB
- Create a design in FSP
- Define the protocols and interfaces in an FSP design
- Synthesize the connections in FSP protocols and interfaces
- Add terminations and external ports in an FSP design
- Generate an Allegro Design Entry HDL schematic from your FSP design
- Export your FSP placement to the PCB Editor
- Backannotate pin swaps and design changes from the schematic and PCB Editor to FSP

Software Used in This Course

- Allegro FPGA System Planner
- Allegro Design Entry HDL
- Allegro PCB Editor

Course Agenda

Day 1

- FPGA System Creation
- FPGA System Synthesis
- FPGA System Completion

Day 2

- Integration with Design Entry HDL and PCB Editor
- Postlayout Optimization
- Importing FPGA Constraint Files and Virtual Interfaces
- FSP Models

Audience

- Design Engineers
- FPGA Designers
- PCB Designers

Prerequisites

You need to have experience with or already have knowledge of Logic Design.