TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Unter http://www.FlowCAD.de/TrainingKontakt.php können Sie sich zum Training anmelden.

Course Title	**Allegro Design Reuse**
Course Category	**System Interconnect Design – Allegro & OrCAD Advance with Engineer Explorer Series**
Duration	**1 Day**

Course Description

Design Reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse. Any EDA user who has time-to-market pressures will benefit from Design Reuse. Design Reuse adds scalability and modularity to your design process, saving time and reducing error by facilitating the reuse of known good IP.

Learning Objectives

- After completing this course, you will be able to:
- Create a subdesign state file
- Create a layout module file
- Document and store the reuse design
- Use properties to control reuse packaging
- Work with hierarchical constraints
- Make changes to subdesigns while in reuse
- Customize packaging with Occurrence Edit
- Apply reuse methodology to existing (flat) designs
- Use macros and parameters
- Search for related solutions on Cadence Online Support (COS)

Software Used in This Course

- Allegro PCB Designer

Course Agenda

- Exploring a Design Reuse Example
- Creating a Reusable Block
- Reusing the Block in Other Designs
- Managing Changes
- Advanced Topics
- Summary and Conclusion

Audience

- Engineering Managers
- PCB Designers
- Design Engineers

Prerequisites

You must have experience with or knowledge of the following:

- Allegro® Design Entry HDL and PCB Editor tools. This course does not teach basic tool operations.
- Hierarchical design and the need to reuse logical blocks and associated part placement and signal routing.

Or you must have completed the following courses:

- Allegro Design Entry HDL Front-to-Back Flow
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AllegroDesignEntryHDLFronttoback.pdf