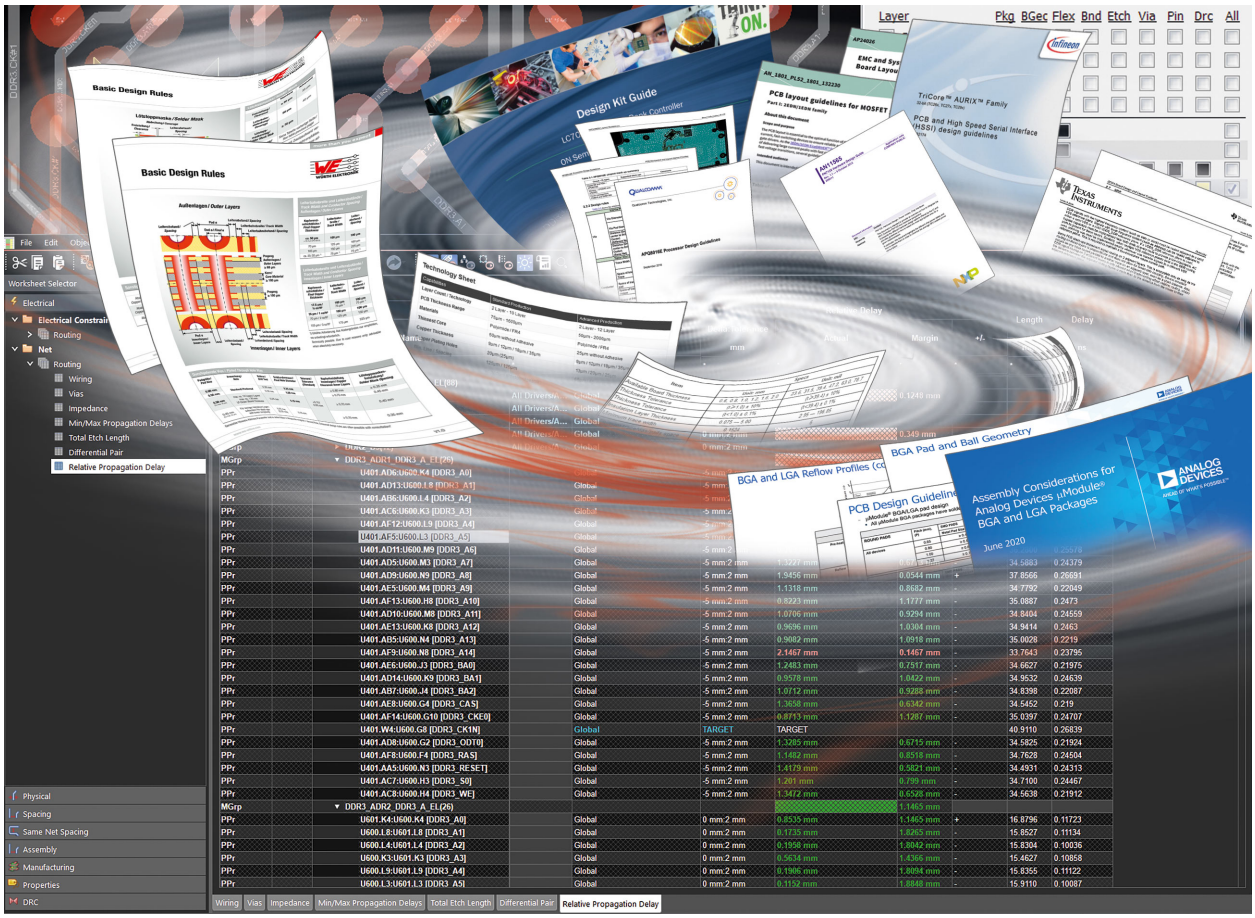
FlowCAD



Save Cost with Constraint Management

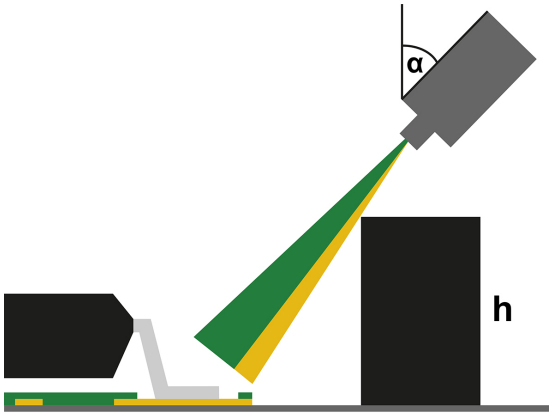
If you look at PCB Design you see basically two tasks. On one hand the engineer is capturing the design intent for the desired functionality of the circuit. On the other hand, all design rules and constraints of physics and manufacturing restrictions have to be followed when implementing the circuit in a PCB layout. With continuous miniaturization, increasing form factors, and higher demand for reliability the number of PCB design rules grows exponentially year of year. At the same time the development time is shrinking. Managing Constraints has become the key task in PCB Design.

"Everything used to be easier". This phrase is often heard in context with PCB development. Once there was a local EMS, the PCB designer had the rough specification for production in mind and could create the layouts. He received handwritten notes or entered properties in the schematic from the developer for the few rules to be followed. Today it is different. Design rules have become more complex, extensive and even partly contradict each other. The number of design rules to be observed increases exponentially in a similar way to Moore's Law. This corresponds to a doubling of the number of rules to be observed every two years. The tolerances of the design rules become narrower with each technological leap. The smallest violations of the specifications can already cause a circuit to no longer function reliably. The guidelines and notes of that time have become a multitude of complex rules, some of which have been optimized by simulations.

What are Design Rules?

Design rules are specifications for the layout of printed circuit boards. Physical specifications come from manufacturing, assembly and testing. For example, there are minimal spacings and trace widths that must not be undercut, as smaller structures cannot be dissolved in the chemical etching process. Production is not guaranteed in this case and short circuits and interruptions may occur. Other rules from manufacturing include minimum distances from hole to hole, dimensions for residual rings, or distances to milling or v-cut edges. These distances depend on the manufacturing process and the machines used.

The rules for placement and testing come from the placement. Thus, there are different spacings depending on the angle and with which neighbors a component is placed. For example, low components to high components have to keep a greater distance, otherwise they cannot be assembled.



Picture 1: Component shadow while AOI

Depending on which test method is used, there are special rules for shading with automatic optical inspection (AOI) or mechanical accessibility with flying test probes or test adapters.

In addition to the physical spacing, electrical specifications are also added. For example, at higher voltages, greater distances between two conductors are necessary, which prevent sparks by air gap or creep distance. At higher currents, larger cable diameters are required, which can be implemented on a PCB by thicker copper and/or wider traces.

For high-speed signals with steep edges or high clock rates for data transmission, impedance-controlled traces are required. They can be implemented by a suitable layer stackup and precisely defined trace widths. Lengths, topologies, approved vias and a defined current return path must also be adhered to. All these rules are typically defined at an early stage of development in the schematic.

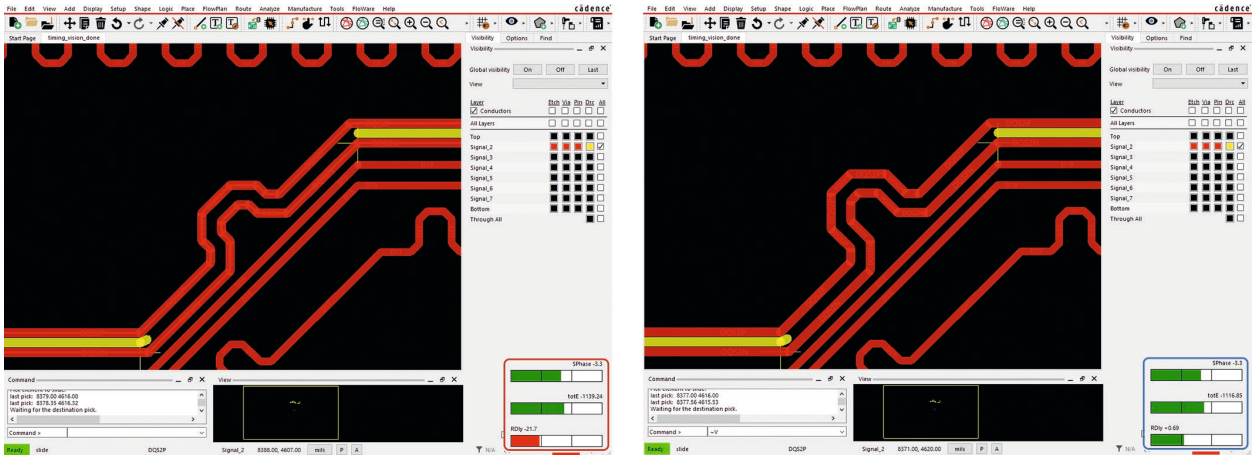
Constraint Manager

At first glance, a Constraint Manager resembles an Excel spreadsheet. Each electrical connection (nets) can be assigned different rules, such as width, length, or maximum number of vias. But a Constraint Manager is much more than just a table. It is deeply integrated into the entire PCB Design Flow as well as the design tools and serves as the basis for the Design Rule Checks (DRC). Modern design tools such as OrCAD and Allegro examine whether the rules are

being followed in real time while the designer is placing its components or routing traces and vias. In the event of violations, immediately provides feedback through visual markings and detailed text information.

For example, if two components are placed so far apart when placing parts that the maximum length rule is violated, even if a direct connection is placed, there is an immediate DRC error already at this stage. By repositioning the component, the error can be avoided directly.

When routing differential lines of a PCI Express interface, the values for trace length (propagation delay), static and dynamic phase tolerance can be displayed via three displayed displays. The differential pairs can thus be reconciled until all rules are complied with.



Picture 2: Dynamic display of delay error (left) and matched timing (right).

The benefit of the Constraint Manager increases with the number of rules entered. The more rules need to be followed in a design, the greater the usefulness of a central constraint manager to have an overview of all the rules. And the more specifications the tool checks as DRC in the background, the better the quality of the design later on.

Advantages of a Central Constraint Manager

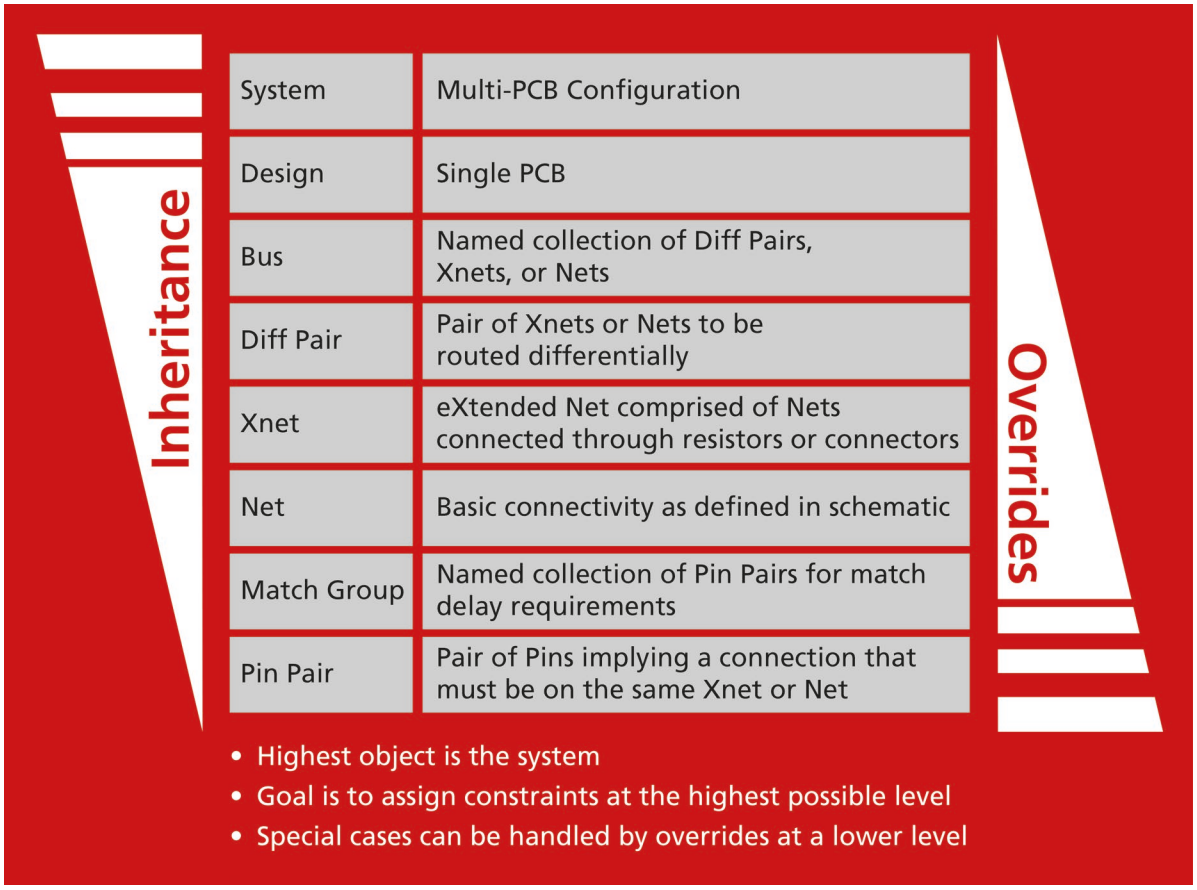
The Constraint Manager is centrally integrated in the flow with schematic, layout and simulation. When Cadence introduced the Constraint Manager in 2000 as the first EDA company, the electrical rules were in focus. Prior to the introduction, there were often misunderstandings and therefore flawed designs due to the different and ambiguous use of terms and units of measurement by developers, procurement, PCB designers and external manufacturing. By centralizing the rules, the terms were unified and there was only one place for the rules (Single Source of Truth). Thus, the use of outdated rules and instructions was excluded and there was no more confusion due to different rule designations. The inconsistencies caused by changes between the schematic, PCB layout and other tools involved in the PCB Flow are also excluded. All team members always use the same values for the same object in the schematic and PCB layout.

Due to the many advantages, Constraint Management is now a must for professional PCB design software. Cadence has gradually improved and perfected this technology since its introduction about 20 years ago.

As the number of electrical rules increased, so did the number of physical rules. In the meantime, all rules are managed in the Constraint Manager.

For a normal printed circuit board with a CPU, memory and interfaces, the number of rules to be observed can quickly increase above 10,000. At first, this number of rules seems rather confusing. Hierarchical rule sets are used to manage this large number. For example, in a rule set, all parameters of a differential signal can be described. The rule set is then applied to all lines of a data bus. In our example, all rules were assigned to all nets in seconds. The hierarchy inherits the rule from the data bus to all child nets.

Similarly, the minimum spacing between lines and other copper elements of 5mil / 100 microns can be defined once for the entire design, and all buses, nets, and extended nets (X-net) inherit the same value. However, if a larger spacing is required for the power supply, the inherited value on the affected lines can be overwritten in a targeted manner. For more clarity, the values of overridden default rules are marked in blue.



Picture 3: Hierarchical inheritance or overriding rules

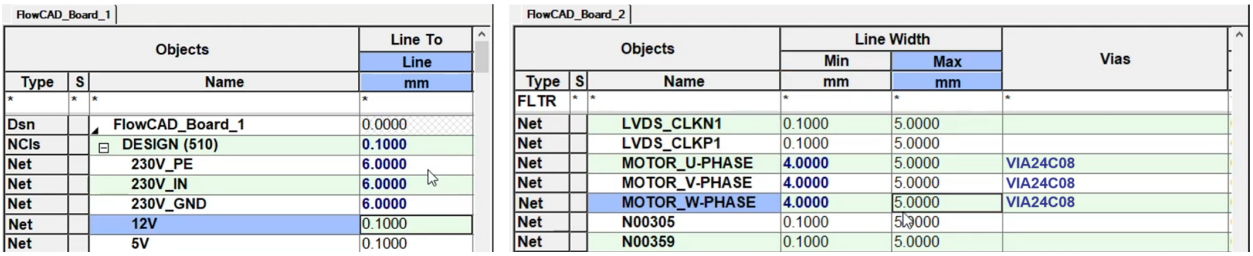
Rules are defined once at the top of the hierarchy and inherited to all underlying elements. Similarly, rule changes from bottom to top are overwritten consistently, quickly, automatically, and thus error-free.

International and interdisciplinary teams can present the values in their preferred view. The trace length can be switched between mil and mm or the developer can see the signal runtime

over indoor and external positions in nanoseconds. The actual rule remains unchanged. The conversion takes place in the Constraint Manager with the help of a field solver in the background and in the display, you can switch between time and length.

Complex rules such as the equal length of signal or address lines in a bus per byte group and the byte groups among each other are also defined once for the PCI Express interface and assigned as a constraint set in the design. The rule can be automatically updated with the pin delays of the ICs and the PCB designer can see its entire timing budget. The specifications can also be used for automated length or phase matching with AiDT (Tune Delay) and AiPT (Phase Tune).

In the design review, it is possible to quickly check whether all rules are up-to-date and assigned to all required nets. Because the rule sets have self-explanatory names, such as "230V net", "10A, max+30°C", "PCI-EXP-IMP", hundreds of rules can be checked very quickly at a glance.



FlowCAD_Board_1

Objects			Line To Line
Type	S	Name	mm
*	*	*	*
Dsn		FlowCAD_Board_1	0.0000
NCls		DESIGN (510)	0.1000
Net		230V_PE	6.0000
Net		230V_IN	6.0000
Net		230V_GND	6.0000
Net		12V	0.1000
Net		5V	0.1000

FlowCAD_Board_2

Objects			Line Width		Vias
			Min	Max	
Type	S	Name	mm	mm	
FLTR	*	*	*	*	*
Net		LVDS_CLKN1	0.1000	5.0000	
Net		LVDS_CLKP1	0.1000	5.0000	
Net		MOTOR_U-PHASE	4.0000	5.0000	VIA24C08
Net		MOTOR_V-PHASE	4.0000	5.0000	VIA24C08
Net		MOTOR_W-PHASE	4.0000	5.0000	VIA24C08
Net		N00305	0.1000	5.0000	
Net		N00359	0.1000	5.0000	

Picture 4: Overview with example rule sets with self-explanatory names

Reuse of IP (Intellectual Property)

Rule sets can be stored in the library and reapplied to other designs. The constraint sets can be kept flexible, so that they can also be applied to different layer stackups. Reusing proven rule sets has the great advantage that rules do not always need to be redefined and can be used with the same quality in multiple designs. This saves time and avoids errors compared to multiple manual creation of the rules.

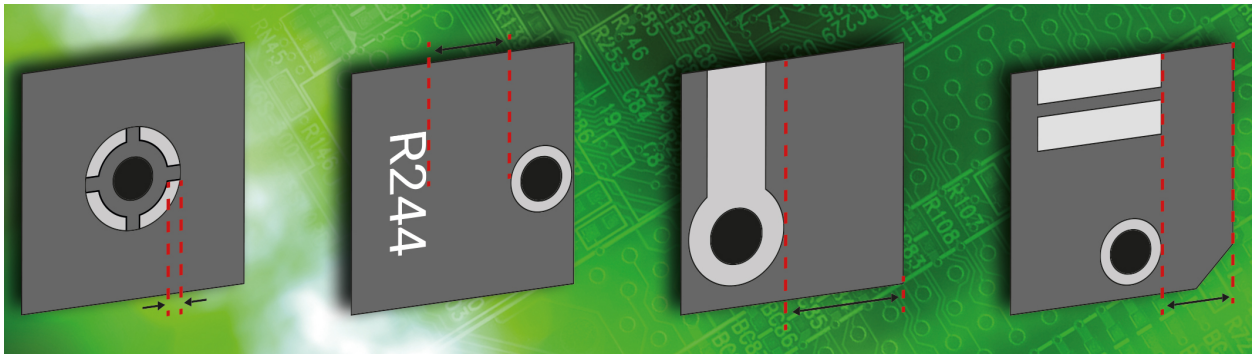
Different Design for Manufacturing (DfM) rules can be assigned as rule sets to a design, depending on the fabricator, assembly or test method. If there are no errors in a design for two sites of manufacturing, a second source is verified for one design.

Once developed, Constraint Sets can also be used by inexperienced or new team members. As a result, they and the company benefit from the knowledge stored in the constraint sets. The development of constraint sets for protocols such as DDR X, PCI or other applications can be expanded into a know-how data base. This secures a company's IP (intellectual property).

Constraint Sets can be imagined as a modular system from which the designer can compose the predefined and pre-qualified rule sets relevant to his design.

Manufacturing Quality

Manufacturing processes can be described by design rules. The more rules defined and adhered to, the better the design data fits the production. Applicable rule sets and real-time DRCs in the layout do not add time for the PCB Designer.



Picture 5: Different rules for production equipment

In addition to the company-specific manufacturing rules, DfM, DfT and DfF rules can also be requested online from the manufacturer via the DFM portal (www.flowcad.de/dfm) and the rule sets can be imported into OrCAD or Allegro. OrCAD uses about 200 different DFx rules. Higher Allegro license levels offer an even more detailed rule set with approx. 2500 rules. The rules-based DRC verifies the special specifications of the PCB manufacturer and take into account, among other things, machine characteristics, such as bracket spacing or specifications for placement machines or tolerances of drilling diameters. Depending on the production line at a manufacturer, different machines may be used, and different distances must be maintained.

Conclusion

The goal of efficient development is "First Time Right", i.e. to avoid mistakes from the beginning before they even arise. The additional costs caused by a late CAD flow checked and corrected problem can be saved without any effort. There is no loss of time due to redundant and possibly erroneous development and the input of rules as properties.

The number of rules and the subsequent compliant implementation increases the design quality and avoids additional costs as well as time lost due to redesigns, prototypes and tests.

More Information

www.FlowCAD.com