

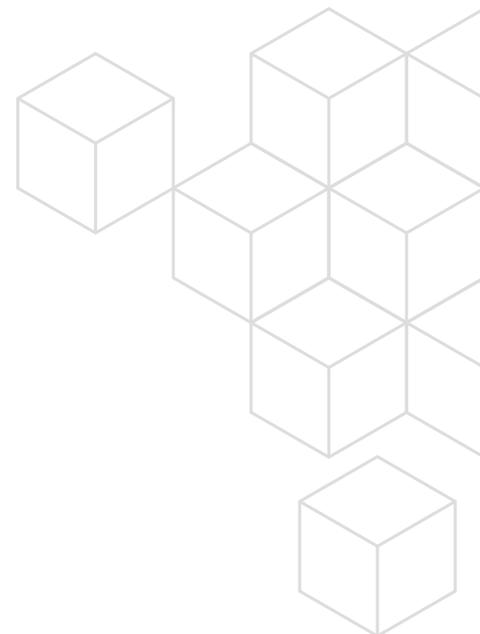
# Thermal and Stress Analysis of 3D-ICs with Celsius Thermal Solver

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This white paper helps designers understand the cross-fabric thermal and stress challenges introduced by 3D-ICs and how the Cadence® Celsius™ Thermal Solver helps designers analyze the impact and develop strategies to mitigate this impact, particularly for 3D-ICs.

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## Design Overview

As electronics get smaller and faster, the environment for thermal issues is becoming more and more challenging. These problems are widespread and can appear in the chip, the board, the package, and the entire system. Figure 1 shows some of the thermal challenges in today's modern electronics.

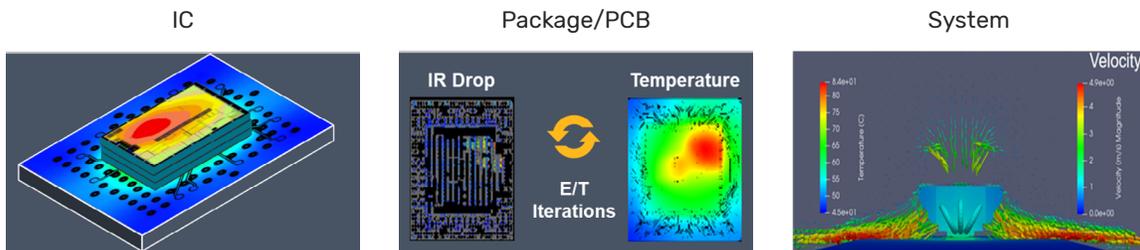


Figure 1: IC, package/board, and system design challenges

3D-ICs integrate many dies (Figure 1, left) that are densely packed, which leads to heat generation resulting in a rise in temperature that causes performance issues. Consequently, it is important to accurately place the temperature sensor in the hot spot to quickly capture and mitigate the temperature rise.

In packages and PCBs (Figure 1, center), the thermal challenges are due to the Joule heating impact, the infrared (IR) drop, and performance. In 3D-ICs, these issues are exacerbated because of the multiple dies. In systems (Figure 1, right), it is important to have a vision of thermal performance to optimize the thermal cooling strategy.

Several years ago, Cadence introduced the Celsius Thermal Solver to address these thermal heating challenges in chips, packages, and systems. The Celsius Thermal Solver is the industry's first complete electrothermal co-simulation solution for the full hierarchy of electronic systems from ICs to physical enclosures. The tool offers end-to-end capabilities for in-design through to signoff (Figure 2).

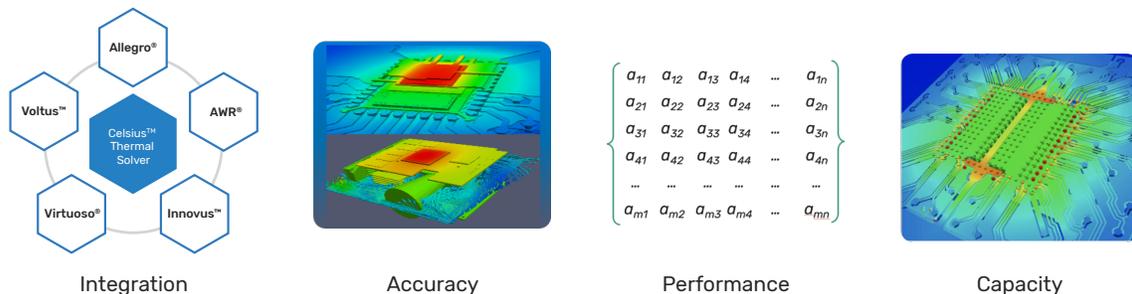


Figure 2: The Celsius Thermal Solver's end-to-end capabilities for both design and signoff

The advantages the Celsius Thermal Solver provides include integration with other Cadence design tools, accuracy with both finite element analysis (FEA) and computational fluid dynamics (CFD), high performance through distributed computing that significantly shortens simulation time, and expanded capacity to import detailed package and PCB models (Figure 3).

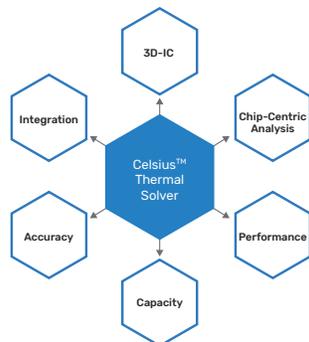


Figure 3: The Celsius Thermal Solver is a complete solution

### Integration

In order to run a simulation, it is often necessary to prepare an input model that, when performed using multiple software tools, can be challenging because it requires teams of CAD, power, and thermal engineers to collaborate on the input model. Because the Celsius Thermal Solver is integrated into other Cadence design tools, these integration challenges are no longer an issue. The Celsius Thermal Solver is not only integrated in Cadence’s Allegro® PCB Package Designer and Allegro PCB Design technology, OrbitIO™ Interconnect Designer with concurrent die/package planning and route optimization, and AWR Design Environment® Platform with RF/microwave design and analysis for PCB and package design, it is also integrated within the Virtuoso® RF Solution, the Voltus™ IC Power Integrity Solution, the Innovus™ Implementation System, OrbitIO Interconnect Designer, and the AWR Design Environment Platform for chip design (Figure 4).

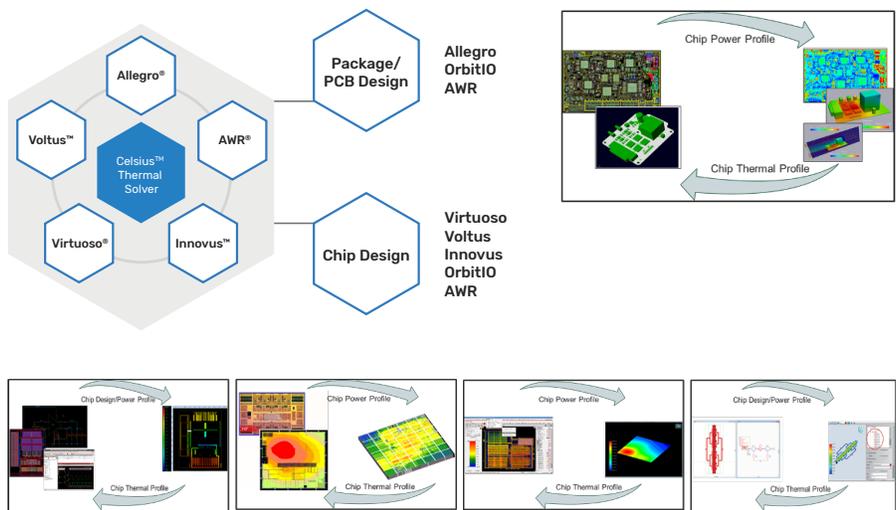


Figure 4: The Celsius Thermal Solver is integrated with Cadence tools for both package/board and chip design

### Accuracy

The Celsius Thermal Solver offers detailed analysis for FEA and CFD of the entire system and is capable of detailed thermal model analysis of chip, package, and board designs. The top of Figure 5 shows the Celsius Thermal Solver package/PCB model analysis process with the thermal profile of the wire bonding of the entire package. The tool performs fine-grain power input for accurate thermal response of the chip. The middle right picture in Figure 5 shows a detailed fine-grain power profile in accurate chip thermal mode, as opposed to the left middle picture of a single power profile for the entire IP, known as a peanut-butter spread, that less robust tools provide. The Celsius Thermal Solver’s integration with the Voltus IC Power Integrity Solution can divide the IP into many different grids and generate a power profile for each of those grids. It also offers advanced 3D finite-element method (FEM) meshing technology that can mesh any system model from very fine detail all the way to a very large system (Figure 5, bottom).

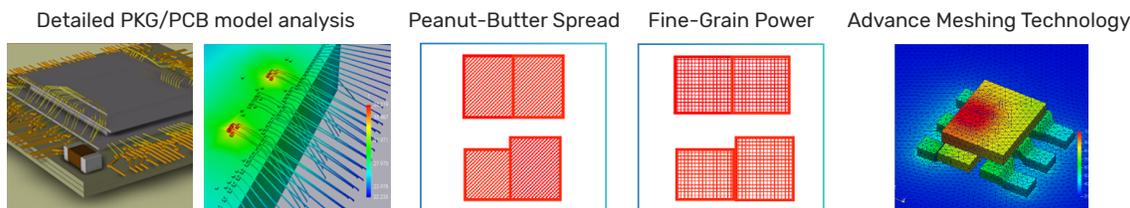


Figure 5: The Celsius Thermal Solver’s accurate, detailed analysis of the entire system

## Capacity

One of the advantages of the Celsius Thermal Solver is that it can import and analyze large, detailed PCB/package design models and analyze large designs with no input simplification needed. For 3D-IC detailed analysis, it addresses the 3D-IC, the die-to-die bonding, and through silicon vias (TSVs). Finally, Celsius can perform joule heating and stress and warpage analysis, as well as co-simulation of electrical transients (E/T), along with CFD modeling for accurate PCB and package design (Figure 6).

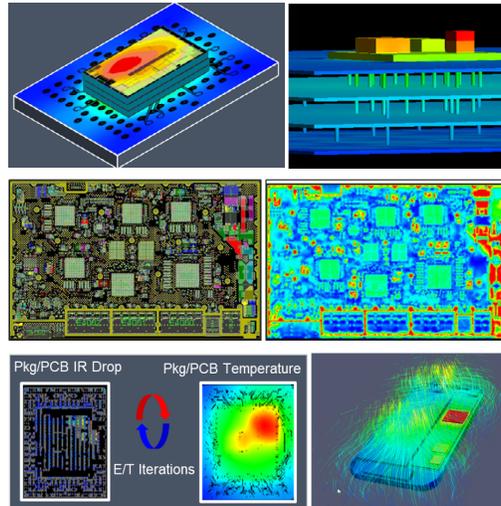


Figure 6: The Celsius Thermal Solver analyzes large, detailed designs with no input simplification

## Performance

The Celsius Thermal Solver uses parallel processing to shorten simulation runtimes. It leverages not only multi-threading but also distributed processing to complete simulations 10X faster. The massively parallelized matrix solver can analyze very complex 3D-ICs and 3D structures, as shown in Figure 7.

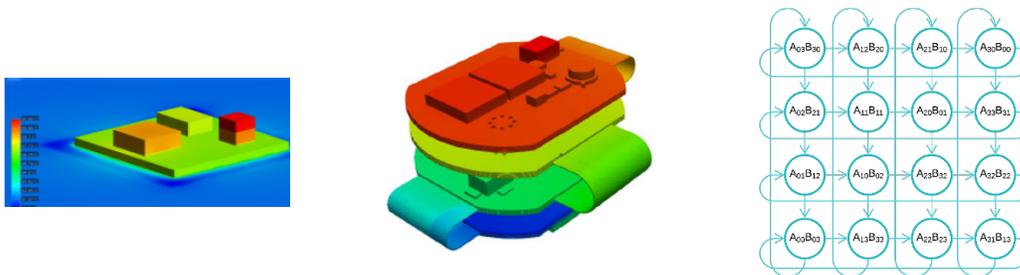


Figure 7: Celsius parallel processing technology shortens simulation runtimes for complex 3D-ICs

## Controlling 3D-IC Thermal and Stress Impact from the Early Design Stage to Signoff

Growing thermal and stress challenges introduced by 3D-ICs include high power density due to increased integration, non-homogenous power distribution inside the chiplet stacks, and greater thermal resistance due to the insulating dielectrics.

Additionally, new stress is emerging due to 3D-IC stacking, bonding, and soldering, TSV drilling and filling, wafer and die thinning, and more (Figure 8).

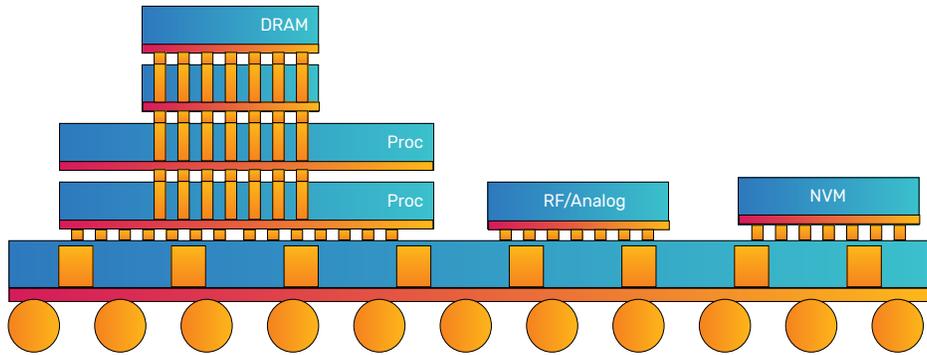


Figure 8: Thermal and stress challenges of 3D-ICs

Temperature and stress issues impact the power consumption, design performance and reliability, and cost of 3D-ICs. Power, infrared (IR), performance, thermal, and stress complications are all highly coupled, and, in addition, thermal and stress in 3D-ICs are cross-fabric problems rather than simply issues within a single design. These myriad problems cannot be solved individually by controlling each package or chip design separately; they must be carefully managed from early in the design stage to signoff with chip/interposer/package co-design and co-analysis using sophisticated EDA tools.

Cadence uniquely meets this need with its complete 3D-IC design and analysis solution from a single EDA vendor. The unified platform for design planning, implementation, and signoff provides quick power integrity (PI), signal integrity (SI), thermal integrity (TI), and mechanical integrity (MI) in-design feedback, system-driven power, performance, and area (PPA), and fast design closure (Figure 9).

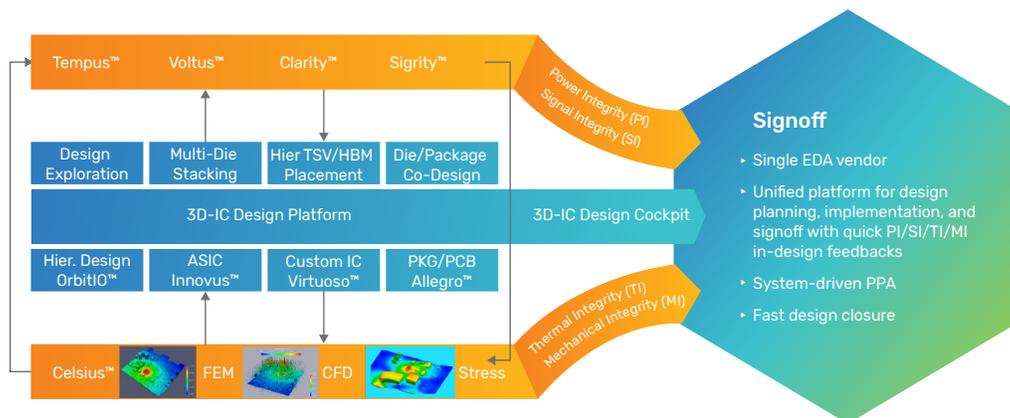


Figure 9: Cadence's unified platform for design planning, implementation, and signoff

Within the single 3D-IC platform is a 3D-IC design cockpit that includes the OrbitIO Interconnect Designer for hierarchical design, the Innovus Implementation System for the application-specific IC (ASIC) and system-on-chip (SoC) design, the Virtuoso environments for customer IC design, and Allegro technology for package/PCB design, as well as design exploration, multi-die stacking, hierarchical TSV, and high-bandwidth memory (HBM) placement and die/package co-design. All these design cycles are bonded by different tools that co-simulate to address the PI and SI, as well as TI and MI, in each design cycle and provide instantaneous feedback for each design cycle, ensuring all phases are performed in guided design steps all the way to signoff.

## 3D-IC Design Exploration with OrbitIO Interconnect Designer and Celsius Thermal Solver

From an early design stage, the Celsius Thermal Solver works with the OrbitIO Interconnect Designer for 3D-IC design exploration. The verlog network, constraints, chiplets (HBMs, redistribution layer (RDL), interposer, package, PCB), TSV/bump descriptions, total power per die and/or block-level power maps, and thermal tech files are all input. Next, the OrbitIO Interconnect Designer will simulate high-level die stacking and TSV/bump planning, after which the design will be saved to a 3D-IC stack database, which can be shared by all the Cadence tools. The Celsius Thermal Solver then accesses that database to perform a simulation and/or stress analysis inside the OrbitIO Interconnect Designer, after which the results and a report can be viewed (Figure 10).

A “what-if” analysis can be performed after comparing the design requirements with the results, and, if the requirements are not met, the designer can go back and adjust the die stacking, TSV/bump numbers, and location inside OrbitIO Interconnect Designer. The database will be updated, after which the simulation can be run again.

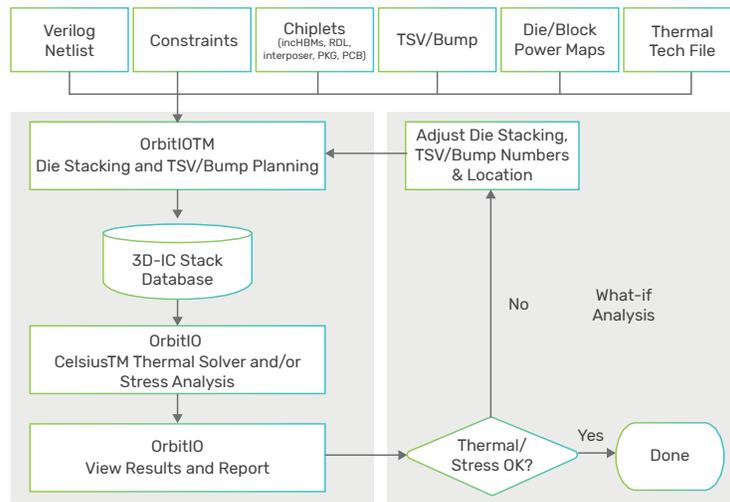


Figure 10: OrbitIO Interconnect Designer and Celsius Thermal Solver work together for 3D-IC design exploration

Figure 11 shows the OrbitIO design stack and Celsius thermal analysis results. Notice the tab for 3D-IC thermal analysis on the left, which provides design stack information, including a side view of what the chiplet stack will look like. For Celsius thermal analysis, the designer can specify power or load in a power value and the model configuration will be generated, enabling the designer to load a real package or create a model prototype package or PCB, run a thermal simulation, and view the results. After simulation, the very detailed temperature distribution for the TSVs can be seen, as well as the RDL layers, die stacking, and, if there are also heat sinks, that can be displayed.

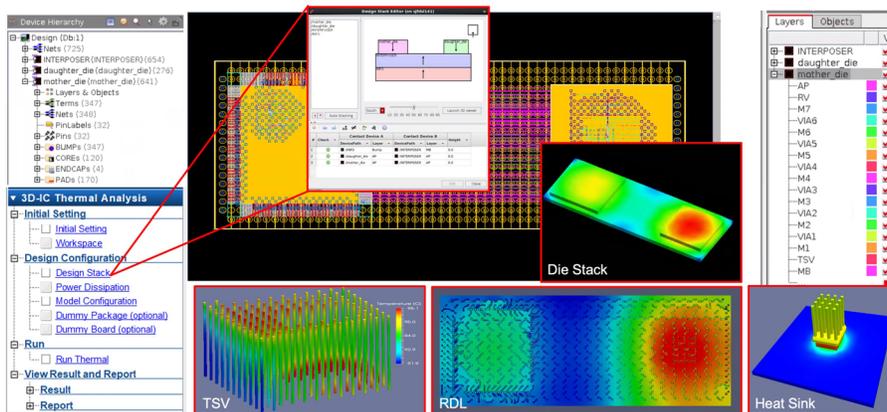


Figure 11: OrbitIO Interconnect Designer design stack and Celsius Thermal Solver analysis results

Figure 12 provides an example of early design stage of the Celsius Thermal Solver's internal stress and warpage analysis of 3D-IC designs. The left side shows Die 1, Die 2, and Die 3 with a package on the top, a TDV connector, and TSVs. The thermal simulation and thermal-mechanical stress analysis are shown on the right, with the TSVs/TDV and the first principal stress on Die 2 below.

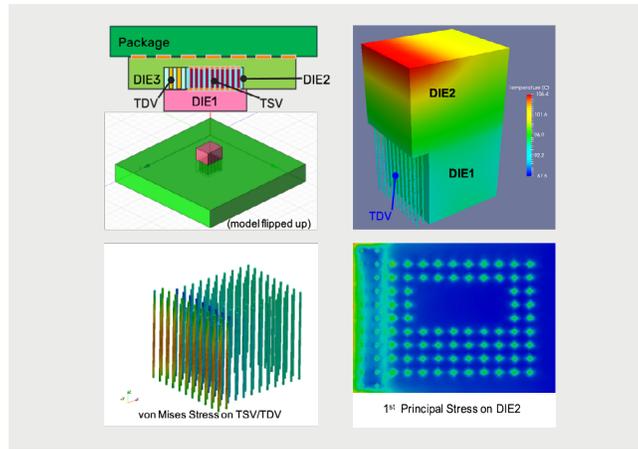


Figure 12: Thermal-mechanical co-simulation of a 3D-IC design under operation

Figure 13 is an example of the warpage analysis of an early design stage chiplet stacking with an ASIC with two HBMs on it, as well as an interposer, package, and PCB. The bottom image shows the maximum warpage on the interposer is  $183\mu\text{m}$ . Sweeping can be performed for different sizes with a different type of analysis.

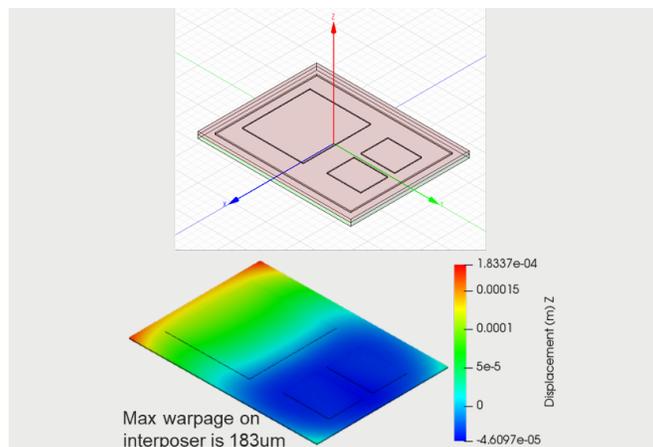


Figure 13: Temperature from 175C-25C of chiplets stacking

## 3D-IC Signoff with Voltus IC Power Integrity Solution and Celsius Thermal Solver

When a 3D-IC design is ready for implementation, the engineer can stay within the same platform and invoke the Voltus solution for chip-level, multi-die IR analysis to obtain more details on the layout and for signoff. Figure 15 shows the Voltus solution being used for IR flat and hierarchical analysis of the multi-dies, interposer, and PCB/package model. For the power analysis, the Voltus solution will channel the design to its die thermal model, after which the package/PCB layout, heat sink, fan, chassis, thermal tech file (TSB/TDV) and HBM thermal model are all taken up to the system-level simulation for the Celsius Thermal Solver's system thermal analysis. The temperature map per die is produced for the Voltus solution to perform thermal-aware signoff, while the system thermal gradient signoff and thermal stress signoff are performed on the Celsius Thermal Solver side (Figure 14).

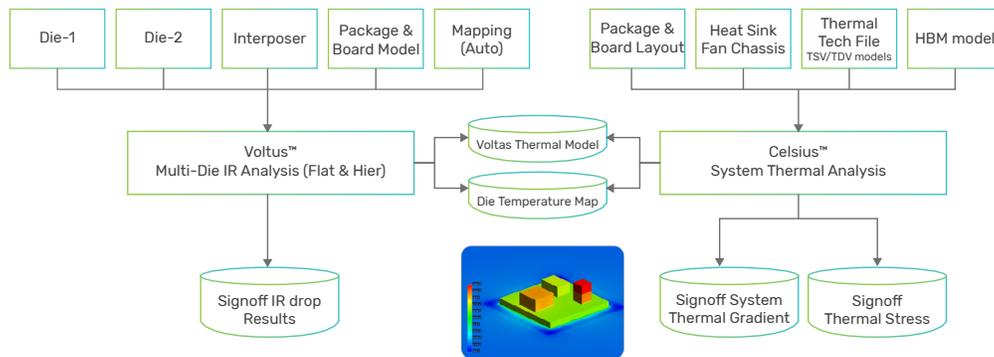


Figure 14: The Voltus solution and Celsius Thermal Solver 3D-IC signoff process

### Fine-Grain Thermal Model Generation with Voltus IC Power Integrity Solution

Figure 15 shows the process for fine-grain thermal model generation.

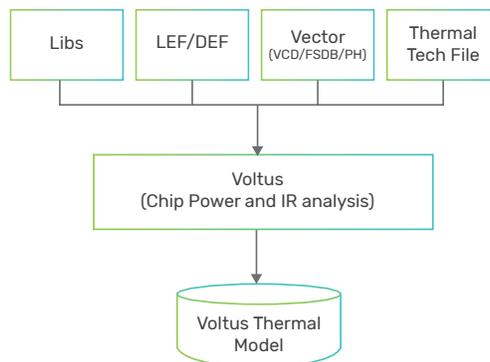


Figure 15: The Voltus solution's thermal model generation

The libraries, library exchange format (LEF)/design exchange format (DEF), vector waveform files (VCD/FSDB/PH), and thermal tech file are fed into the Voltus solution for chip power and IR analysis. The thermal model contains the die materials and thermal properties, layer-based metal densities, and temperature-dependent leakage power and internal and switching power information. This can be either static or time based, as the software can do transient simulation for time-based thermal analysis. The model granularity can be controlled by the user and supports using a different number of tiles per layer, so the power map, power grid, and metal density grid can all be different. The Voltus solution also supports the ability to merge multiple tiles from different IP (Figure 16).

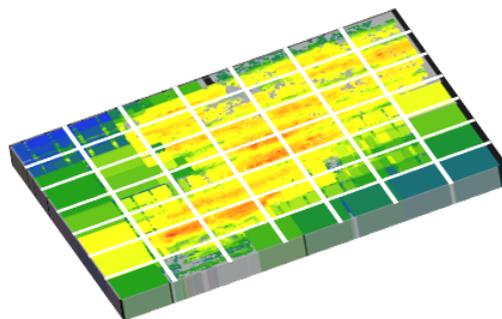


Figure 16: The Voltus solution supports analysis of a different number of tiles per layer

Where the designer is working on a top-level design and has important IP information such as CPUs and GPUs, if more fine-grain resolution is needed for power intensive IP, the Voltus solution can be used for a fine grain thermal model. For the less important portion such as the chip thermal model, a coarser grain can be used. The Celsius Thermal Solver combines the fine-grain and coarse grain blocks into a merged model that supports simulation of multiple tiles sizes corresponding to each IP thermal model (Figure 17).

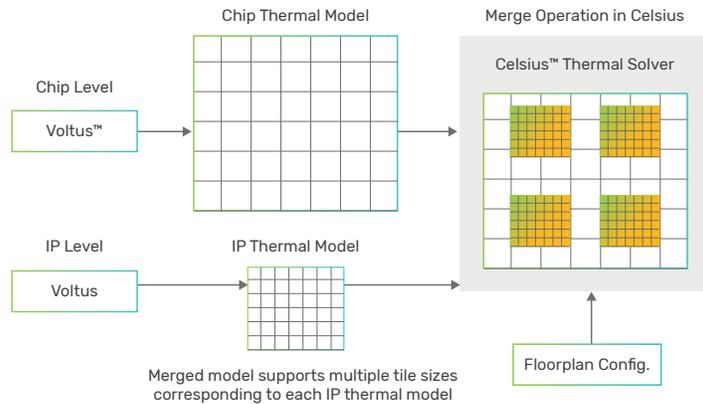


Figure 17: Fine-grain IP and coarse grain thermal models merged in Celsius Thermal Solver

### Fast and Accurate Die-Centric Thermal Analysis with Celsius Thermal Solver

The Celsius Thermal Solver enables thermal signoff analyses and decisions more quickly. In the example in Figure 18, a high-resolution die model has been imported, as well as the temperature dependent leakage and dynamic power definition for each individual tile. The graph shows the thermal results for the simulation of temperature and total power versus the time for the die and individual tiles. The fine-grain thermal analysis was performed much faster than other tools. In this case, the Celsius Thermal Solver ran the simulation in three minutes versus two hours for other tools. The mesh in Figure 19 alone took more than a half hour for other tools to solve.

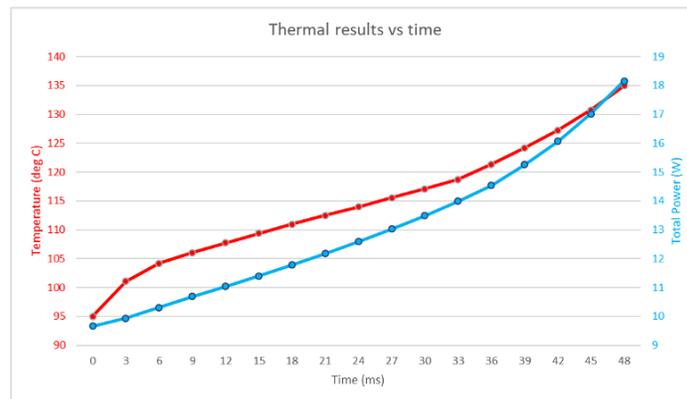


Figure 18: An example of Celsius Thermal Solver’s fast and accurate die-centric thermal analysis

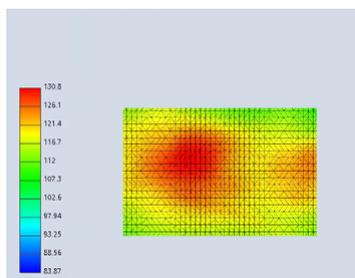


Figure 19: Fine-grain thermal analysis of the mesh

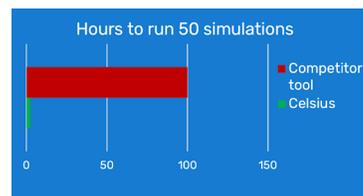


Figure 20: Thermal analysis with Celsius Thermal Solver can take less person hours

Note that the leakage of power grows when temperatures rise, thus total power includes leakage in the switch and the different temperature matchings. The risks of not doing sufficient thermal analysis include functional and parametric yield loss and over-constrained chip performance because of conservative thermal mitigation strategies. Faster thermal simulations can help engineers run more analyses and make better design decisions before tapeout (Figure 20).

## Thermal Throttling Analysis

The Celsius Thermal Solver also offers thermal throttling analysis. The customer example in Figure 21 shows how the software improves the performance benchmark score via thermal mitigation from dynamic voltage frequency scaling mode (DVFS). The graph on the left shows the CPU power profile and temperature result without any mitigation. It can be seen in the middle region that some dynamic voltage and frequency scaling definitely still needs to be applied. For the GPU power profile and temperature variations graph on the right, it can be seen that without thermal mitigations the temperature would be higher than 75°C. But in this case, the designer is looking for 70°C and with thermal mitigation the temperature can be controlled.

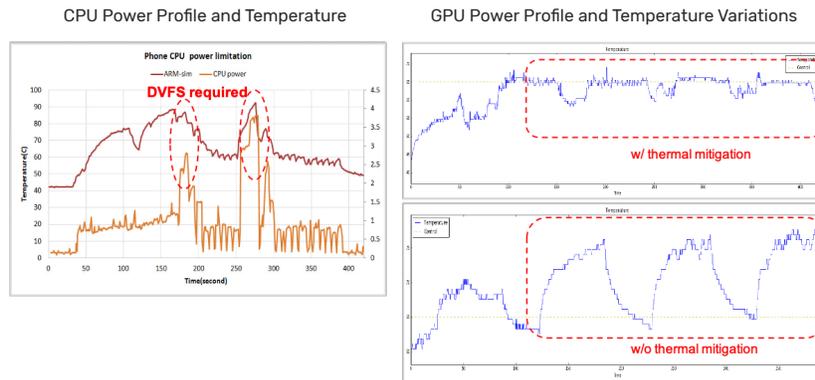


Figure 21: CPU power profile and temperature (left) and GPU power profile and temperature variations (right)

For this example, the Voltus solution’s thermal model was input for each DVFS mode using the Celsius Thermal Solver’s multi-mode configuration, and thermal runaway detection was run. Thermal sensor location optimization was also performed using the Celsius Thermal Solver’s transient thermal throttle analysis because when doing thermal mitigation, it is important to obtain accurate temperature sensor results and feedback for the different voltage and scaling modes to mitigate potential thermal risks. Figure 22 shows the CPU benchmark scores for DVFS configurations 1 and 2, and that the scores have been improved via the refined DVFS scheme.

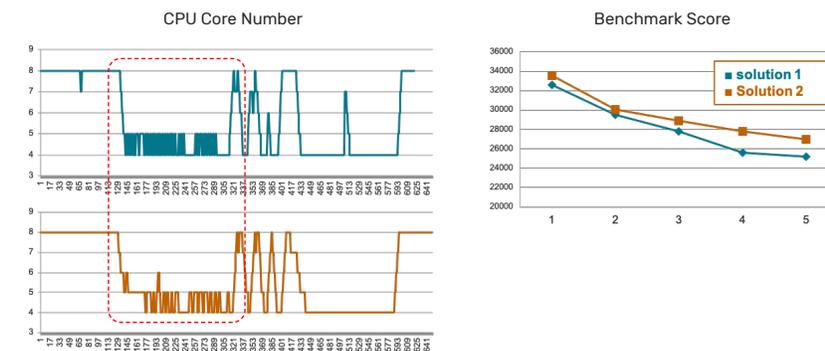


Figure 22: Improved performance benchmark score via thermal mitigation from DCVS

## Accurate FEA and CFD Co-Simulation of CPU/Package/PCB/Heatsink

The Celsius Thermal Solver provides high-fidelity temperature distribution on a detailed layout, resulting in accurate simulation results. The tool offers two solvers inside one: FEA for conduction and CFD. Combined, they give the best and most accurate simulation results for on-die temperature measurement.

For the design example in Figure 23, the die thermal model created in the Voltus solution was loaded into the Celsius Thermal Solver, as well as the package and PCB designs imported from the system in package (SiP) and board layout and the heat sink mechanical CAD design imported from STEP. A real-world convection and radiation simulation was performed, along with a detailed analysis of the conduction layout. The air flow analysis for the enclosure in the CFD domain is on the left of Figure 23 and the high-fidelity temperature contour detailed layout for the package and PCB is on the right. The temperature distribution across the vias and traces, etc., can be seen.

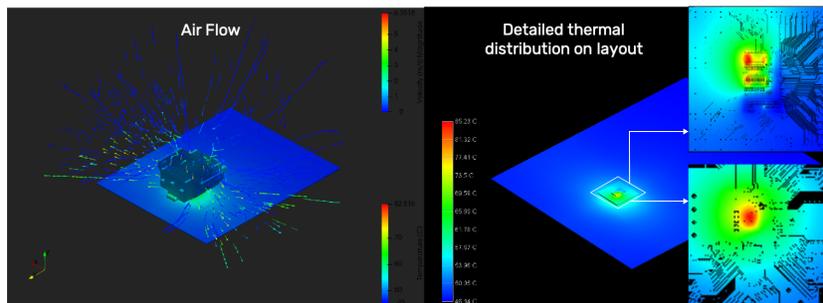


Figure 23: The conduction layout analysis

Figure 24 compares the different die measurements performed by the customer for a simplified model for the PCB and package using the Celsius Thermal Solver for FEA only, for CFD only, for FEA and CFD combined, and a third-party tool. There is a 10°C difference using the third-party tool, a 5.75°C difference using FEA only, and a -2.18°C difference with using CFD only. The co-simulation between FEA and CFD yielded a much better correlation with a measurement of only 0.23°C difference.

	On Die Tj (°C)	ΔT(°C)
Measurement	75	NA
Other Tool	85	-10.00
Celsius FEA Only	90.76	5.76
Celsius CFD Only	82.82	-2.18
Celsius FEA+CFD	85.23	0.23

Figure 24: FEA and CFD combined give the best match for on-die temperature measurement

## Conclusion

The Celsius Thermal Solver provides many advantages for 3D-IC design, including a single tool for thermal FEA, CFD, and stress analysis with seamless integration with the Innovus implementation and OrbitIO interconnect 3D-IC design platforms and the Voltus IC Power Integrity Solution for power signoff. For TSV and 3D-IC planning, the Celsius Thermal Solver provides flexible thermal and stress analysis, as well as high performance and accurate thermal and stress analysis for signoff. It also supports foundry 3D-IC and advanced technology.

Cadence offers several key 3D-IC solution advantages. It provides a single EDA vendor for a full-system PPA-driven solution with co-design analysis for PT/SI/TI/MI with digital/analog die, package, and board. It also provides a unified platform for design planning, implementation, and signoff, enabling fast design closure and turnaround time, as well as margins and cost cuts.