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Advances in EM Analysis and Design Flows for RF System Development

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With the move toward higher frequencies and component densities, RF/mixed signal PCB systems and heterogeneous system-in-package (SiP) technologies are increasingly susceptible to delayed product development turnaround times that threaten delivery schedules. These delays often occur late in development during integration when components that met the design specifications fail to achieve the required system performance collectively. Systems are especially at risk in cases where higher levels of integration, shrinking system footprints, and the move to higher frequencies lead to increased electromagnetic (EM) coupling, as well as electrothermal concerns resulting from the power dissipation of densely packed electronics.

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Overview

This paper overviews the Cadence design platforms that address this growing problem by providing seamlessly integrated EM and multiphysics/thermal simulation with the capacity to solve large-scale design and integration problems across IC, package, and board, to address advanced system integration. In addition, groundbreaking cross-platform interoperability between the Cadence® AWR Design Environment® platform for RF/microwave design, the industry-leading Virtuoso® design platform for RFIC/SiP design, and the Allegro® platform for PCB and IC package design supports RF to millimeter-wave (mmWave) intellectual property (RF IP) integration across heterogeneous technologies.

Advanced Integration Technology and Evolving RF/Mixed-Signal Systems

Traditionally, custom IC designs based on the latest advanced node technology have been the path to superior performance; however, complex designs today increasingly rely on heterogeneous integration to gain a performance edge. RF and mixed-signal engineering efforts have embraced diverse semiconductor processes along with advanced cross-fabric packaging, system- and package-in-package (SiP/PiP) technologies, 3D-ICs, and integrated antenna-in-package (AiP) solutions. Figure 1 shows this evolution of packaging technology and integration over the past four decades.

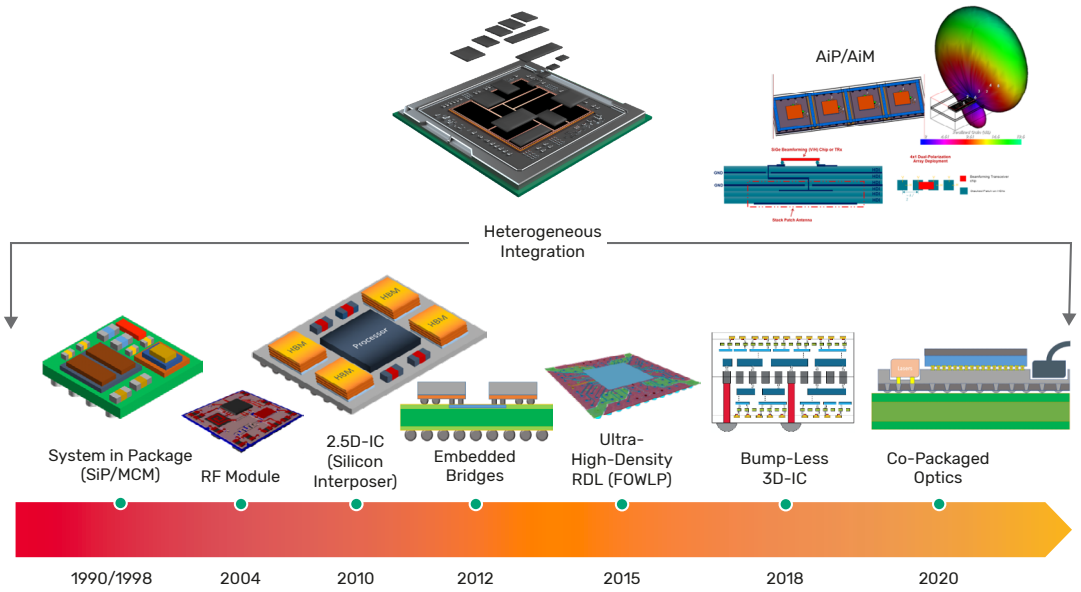

Figure 1: Timeline of evolving integrated multi-chip packaging technologies

Heterogeneous integration mitigates the high cost of homogeneous system-on-chip (SoC) solutions by enabling designers to combine proven RFIC and monolithic microwave IC (MMIC) designs on substrates using newer packaging technologies. Advanced integration methodologies such as fanout wafer-level packaging (FOWP) can result in smaller and more efficient systems, yet, these highly integrated systems are more complicated and error-prone due to the interdependencies of the individual components, the complex network of cross-fabric interconnects, and the challenges of assembling cross-platform design data from multiple sources.

Developing heterogenous systems calls for a host of simulation technologies integrated within the design platform that best support the physical circuit realization for a given manufacturing process. As heterogeneous systems rely on multiple technologies to achieve the overall system requirements, they involve multiple design platforms and simulation technologies. Cadence design and analysis solutions address silicon and compound semiconductor RFIC/MMIC, module, and PCB design and integration with support from Cadence EM extraction technologies for system-level analysis of the chip, package, and board. Figure 2 presents a guide to the technology specific design platforms and integrated analysis software. Among these different technologies, this paper primarily focuses on EM analysis for RF to mmWave gallium arsenide (GaAs), gallium nitride (GaN), and silicon (Si) MMICs and PCB technologies.

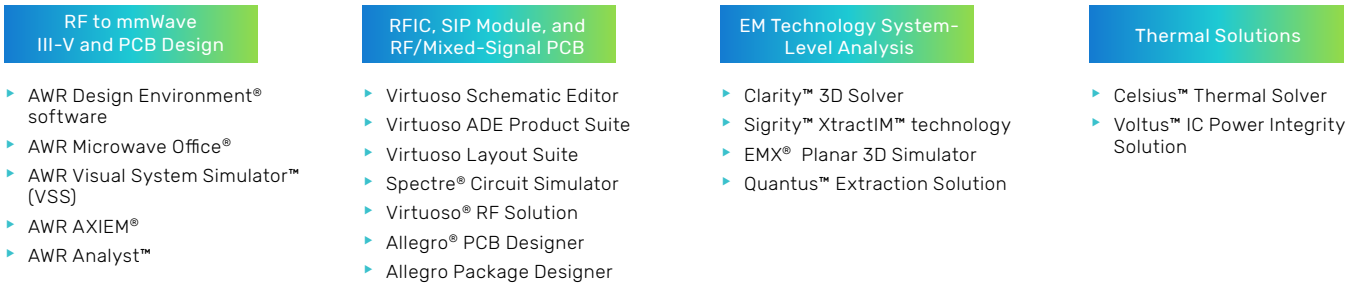

Figure 2: Cadence portfolio for RF front-end design and manufacturing flows

The Cadence AWR Design Environment platform supports RF/microwave design with fully integrated high-frequency circuit, system, EM and thermal simulation technologies. This allows the RF component designer to develop linear designs, such as filters and couplers, and nonlinear designs such as power amplifiers (PAs) with in-situ, full-wave EM extraction and system-level testbenches for simulator communication metrics, such as bit error rate (BER) and error vector magnitude (EVM). The AWR platform, which features Microwave Office® circuit simulation, has recently integrated the Clarity™ 3D finite element method (FEM) and Celsius™ Thermal solvers directly into the AWR Design Environment, providing a powerful and user-friendly, extraction-on-demand technology that supports in-situ circuit/EM co-simulation. The Clarity 3D FEM simulator addresses large-scale EM structures through its massively parallelized solver technology.

Clarity 3D FEM Analysis for Large Capacity RF Network Design

Historically, true 3D simulations are costly in terms of design time and computer resources. Large simulation jobs required for system verification are often segmented into smaller jobs and the results are stitched together, adding risk to the design cycle. These systems need 3D simulation that is efficient and scalable to solve problems quickly with on-premise computer resources, and solve extremely large problems quickly, readily, and securely in the cloud.

3D EM simulators solve Maxwell's equations to provide full-wave modeling of high frequency structures. In a typical EM simulation flow applied by most commercial 3D solvers, the design is imported into the solver either through the MCAD or ECAD process and an initial mesh is performed, followed by the adaptive mesh refinement. Mesh refinement in the Clarity 3D Solver is an automated process, followed by a frequency sweep with interpolated frequencies over the user-specified band of interest for which S-parameters are generated.

Many EM simulators follow this procedure, but the unique approach of the Clarity 3D Solver to solving matrices gives this simulator a distinct advantage in addressing the larger problems associated with integrated heterogeneous RF systems. Clarity employs a state-of-the-art massively parallelized matrix solver with breakthrough algorithms in the adaptive mesh refinement and frequency sweep processes. The elastic compute architecture is partitioned automatically and can be used on any capacity machines with unbounded scalability. Furthermore, cloud-optimizing distribution provides dynamic deployment and fault-tolerant restart while prioritizing lower cost.

In addition to the massive parallelization and automated mesh refinement offered by the Clarity 3D Solver's performance scaling, capacity, and cloud readiness make it uniquely suited for heterogeneous system verification and its seamless integration with the AWR Design Environment, Virtuoso, and Allegro SiP and PCB platforms make the design flow repeatable, scalable, and traceable.

Bigger Problems Solved with a Smaller Memory Footprint

Figure 3 illustrates the breakthrough architecture that enables the Clarity 3D Solver to offer a significant computational advantage in addressing large problems over other EM simulators. With traditional solvers, the design is either imported or created in the tool on a master computer, which then creates the initial mesh followed by the adaptive mesh. The initial mesh and adaptive meshing are performed on a single machine, where the adaptive meshing becomes a performance bottleneck. After the adaptive mesh has been carried out on the master computer, the flow distributes the frequency sweeps to individual machines in parallel. Frequency sweeping is distributed to multiple machines to speed up simulation run times, but the multi-frequency point distribution doesn't improve the solver's overall capacity and ability to solve larger problems.

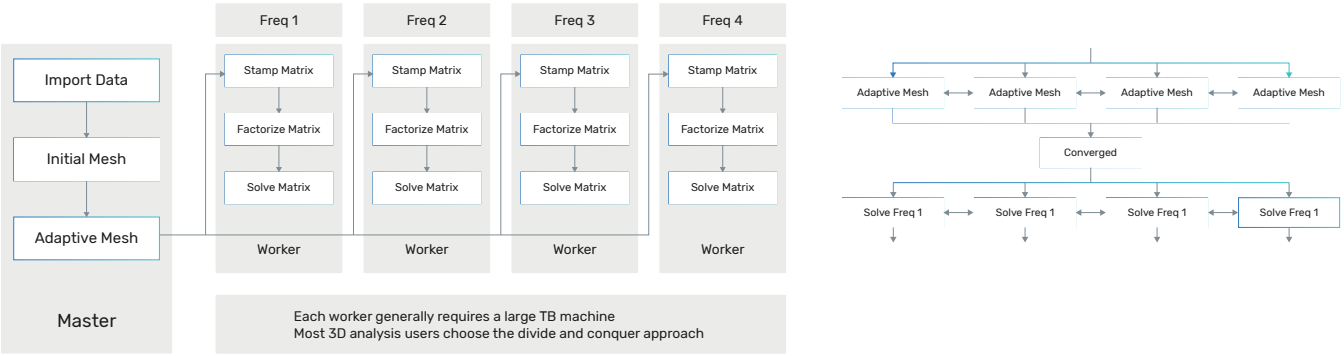

Figure 3: Comparison of traditional EM solvers vs. Clarity's distributed processing workflows

In contrast, the distributed processing flow in the Clarity 3D Solver uses a new approach called massively parallelized matrix solver that applies to both the adaptive meshing and frequency sweeping stages. A breakthrough decomposition algorithm with near-linear scalability supports multithreading, distributed processing, and cloud computing. Big jobs are split into small ones and distributed to different machines, each with a small amount of memory. This is the main essence of the Clarity 3D Solver—parallelization applied to both adaptive meshing and frequency sweep, enabling designers to use fewer computing resources for each distributed job and less time to solve the problem without a loss in accuracy. As a result, Clarity's distributed processing flow offers superior speed and capacity without loss of accuracy than the legacy approach to EM simulations.

FOWP Example

The Clarity 3D Solver was used to analyze 40 DDR4 signal and power traces that were distributed across a four-layer, fanout wafer level, package-on-package system from DC to 20GHz. This design, developed for 5G RF handset-to-base station transmissions, took a traditional 3D EM simulator 62 hours to solve. The Clarity simulator solved this problem in under five hours using 256 CPUs across eight machines (32 CPUs per machine) resulting in a 12.3X improvement in simulation time. In addition, Clarity 3D Solver required only 41GB of memory per machine versus 500GB for the legacy solver.

5G Antenna Example

In a second case study, the Clarity 3D Solver was used to simulate a 5G antenna in the presence of a tablet case, display, batteries, and PCB to simulate the antenna response, return loss, and crosstalk between the antenna port and the PCBs. The simulation time using 40 cores was one hour for the antenna response and six hours for de-sensing. Figure 4 shows the simulated return loss over frequency results for the isolated antenna, antenna with case, antenna with case and display, and, finally, the full design. This illustrates the importance of simulating the entire system to understand the true behavior of the finished product.

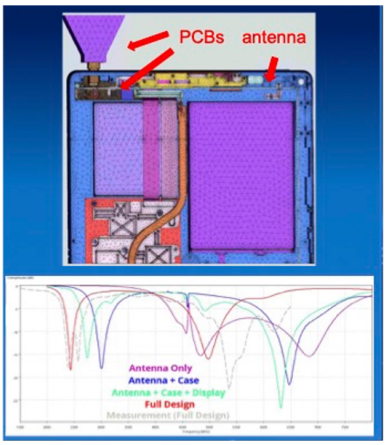

Figure 4: 5G antenna analysis and de-sensing showing the impact of the tablet components on the antenna performance

AWR/Clarity 3D EM Integration

The integration of the Clarity 3D Solver into the AWR Design Environment platform enables RF design teams and system integrators to tackle extremely large, system-level EM problems without the need to partition the structure into smaller parts. As a result, AWR software users can now address RF integrity concerns that occur during multi-technology integration while significantly reducing simulation run times for design optimization and verification. Late-stage design problems and potential respins can be reduced through early identification and individual circuit designers and design teams can perform in-situ EM analysis, while Clarity users can leverage additional design automation features in AWR software that enhance productivity.

AWR® introduced its own advanced EM Socket™ EM integration technology in 2003. This seamless interface supports circuit/EM co-simulation and in-situ full-wave S-parameter extraction for both planar and arbitrary structures using the AXIEM® 3D planar EM analysis and Analyst™ 3D FEM tools. The EM Socket now supports the exact same functionality and integration with the Clarity tool, providing RF system-level design verification and in-situ co-simulation with Microwave Office software from within a single platform.

MMIC Die in QFN Package Example

The integration of a high frequency MMIC die in a quad flat no-lead (QFN) type package illustrates the need for 3D EM simulation with the capacity to address RF system-level design verification along with RF circuit co-simulation. The example is based on an X-band GaN MMIC power amplifier (PA) in a QFN package on a PCB test fixture with sub-miniature Version A (SMA) connectors.

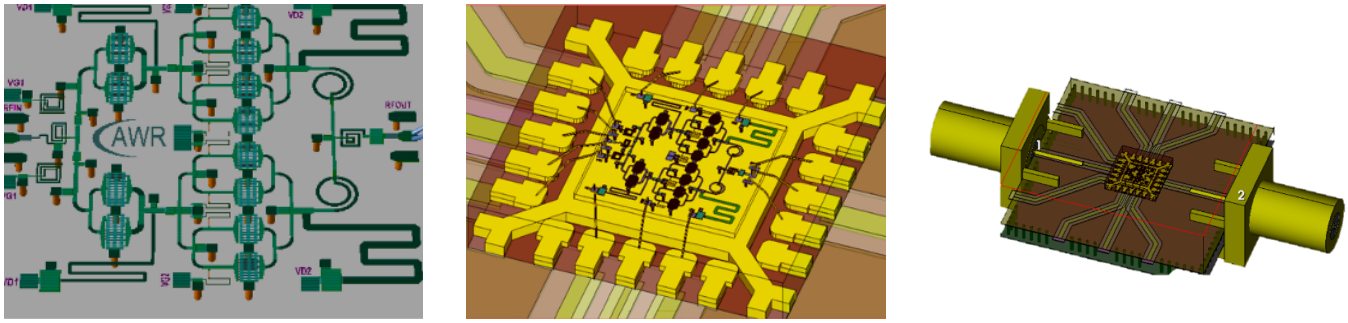

Figure 5: X-band GaN MMIC PA in a QFN package on a PCB test fixture with SMA connectors

The simulation results in Figure 6 for the two-stage MMIC PA show good gain flatness over the target frequency until the inclusions of the package model and the PCB, which introduces parasitic inductances to ground, thereby, significantly degrading the performance over the operating band. Through circuit/EM co-simulation, designers could make modifications to the PCB grounding to the package, addressing the degradation in gain flatness over the band. In a heterogeneous system, the GaN MMIC PA bare die could be mounted directly into a multi-chip module and the analysis would focus on the interactions between the die and module. System level EM analysis and circuit co-simulation allows design teams to investigate and optimize chip, package, and board interactions with greater fidelity.

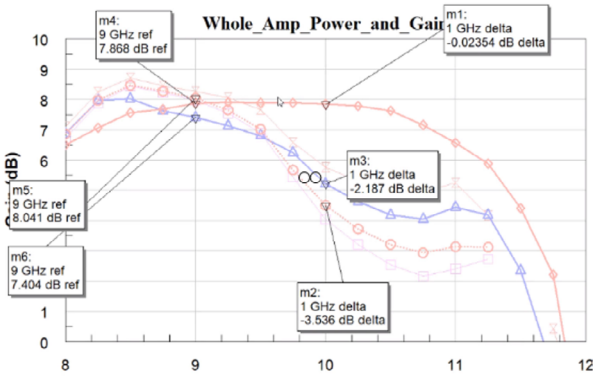

Figure 6: Simulation results of the MMIC with package model and PCB

RF Circuit Design and Integrated EM Analysis Workflows

The EM Socket technology supports multiple workflows to reduce the level of effort required to set up a design for EM analysis, extract a full-wave model from an existing design, and obtain EM/circuit co-simulation results. Data and design information can be shared within a single project, between different projects, and with other design platforms, thereby, optimizing engineering efficiency and productivity while reducing the potential for design entry errors. Three common workflows leverage the integration between the AWR Design Environment and supported EM simulators such as the Clarity 3D Solver. These include an RF design verification flow, an RF in-design flow, and an antenna and antenna array system flow.

The RF Design Verification Workflow

RF design verification using the Clarity 3D Solver can occur entirely within the AWR Design Environment platform when the layout information and design have been built entirely within Microwave Office software. The design verification workflow also enables EM analysis of large RF/mixed-signal, multi-technology RF systems by taking advantage of AWR PCB design import automation. Design verification occurs towards the end of the overall design process with the optimization and integration of individual components into a system. The design team needs to ensure that all the individual parts work together as a single product. This is where the Clarity 3D Solver's capacity for solving large structures provides a significant advantage. As Figure 7 shows, the design automation offered by AWR software, especially the PCB design import wizard, facilitates this workflow.

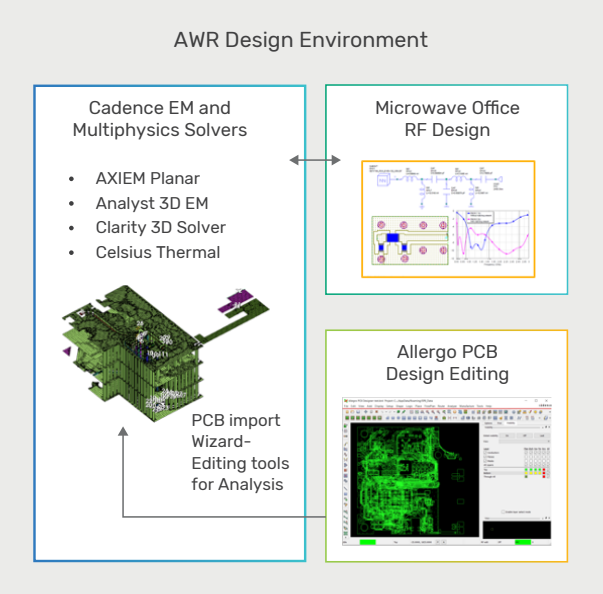

Figure 7: RF and mixed signal designs created in Microwave Office software and integrated in Allegro PCB Designer platform

RF and mixed-signal designs with RF content created in Microwave Office software are often integrated along with the mixed-signal and power electronics in a PCB tool such as Allegro PCB Designer. Designers can import large designs from the Allegro platform using AWR's PCB import/editing functionality, prep structures for EM analysis with shape preprocessing rules, smart shape select, and more. It allows analyzing larger PCB systems with RF IP embedded alongside high-speed traces and characterizing large port count laminates and packages, including off-chip RF design components.

Figure 8 shows the 5G handset reference design, in which board data, including the board stackup, conductor layers, and metal information, were imported into AWR software and prepared for EM analysis. Without smart automation, this process can be labor-intensive, slow, and prone to error. Fortunately, the PCB import wizard in AWR software provides smart selection and editing functionality to construct an EM document from the PCB import using data obtained directly from the Allegro board data itself.

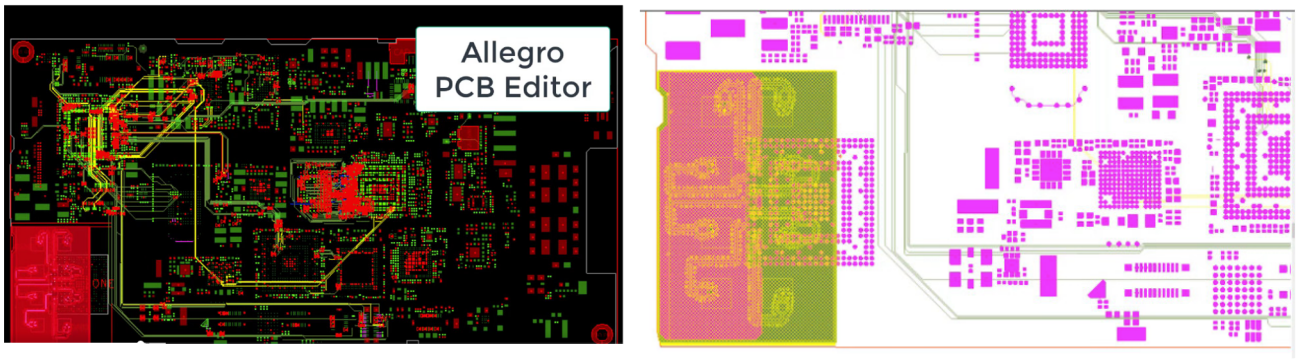

Figure 8: The import wizard automates the process of importing PCB data including board stackup into the AWR Design Environment

Alternatively, neutral PCB formats such as IPC-2581, ODB++, and Gerber file data can be used when a different PCB editor is the source of the layout information. After selecting the desired format and file data, the import creates a new layer property flow (LPF) file containing the layer definitions that are specific to the imported PCB. The user can preview layers on the PCB import dialog and choose to import only the layers that will contribute to the electrical response of the design for EM verification.

The next step in the process is to create an EM document. After importing the PCB design, the user can create an EM document by selecting net names individually or as a group, or by selecting a specific region from the imported PCB design, using their cursor to actively select the area of interest. After identifying the desired shape or clip region, the user performs a "copy to EM structure" operation, which opens the EM Structure dialog box, allowing the user to assign a specific solver, such as the AXIEM 3D planar or Clarity 3D Solver, to the newly created EM document (Figure 9).

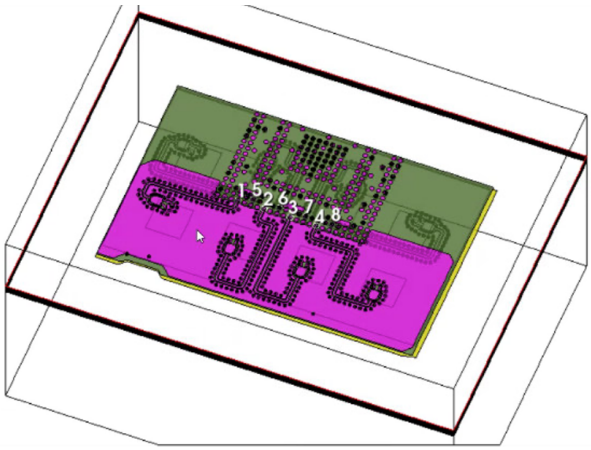

Figure 9: 3D view of an EM document containing the RF section imported from a larger PCB system

The user has the option to apply shape preprocessing rules to the layout in the EM structure creation process. This allows the designer to decrease the complexity of the structure for EM simulation. The newly created document in the project tree includes the imported design as well as the enclosure definitions, which include the boundary conditions for all sides of the enclosure, and the material stack-up definition, including the thicknesses and electrical properties of all metal and dielectric layers associated with the newly created document.

Cellular IoT Example

The next example is based on a cellular internet of things (IoT) reference design that uses a surface mount antenna represented by an S-parameter model provided by the manufacturer. The model is available as a component in the standard Microwave Office vendor library for developing band-specific impedance matching networks to optimize antenna efficiency, the ratio of the power radiated to the power supply to the antenna. The antenna vendor, Igneon, uses Microwave Office software and its network synthesis capabilities to develop band-specific impedance matching networks (Figure 10).

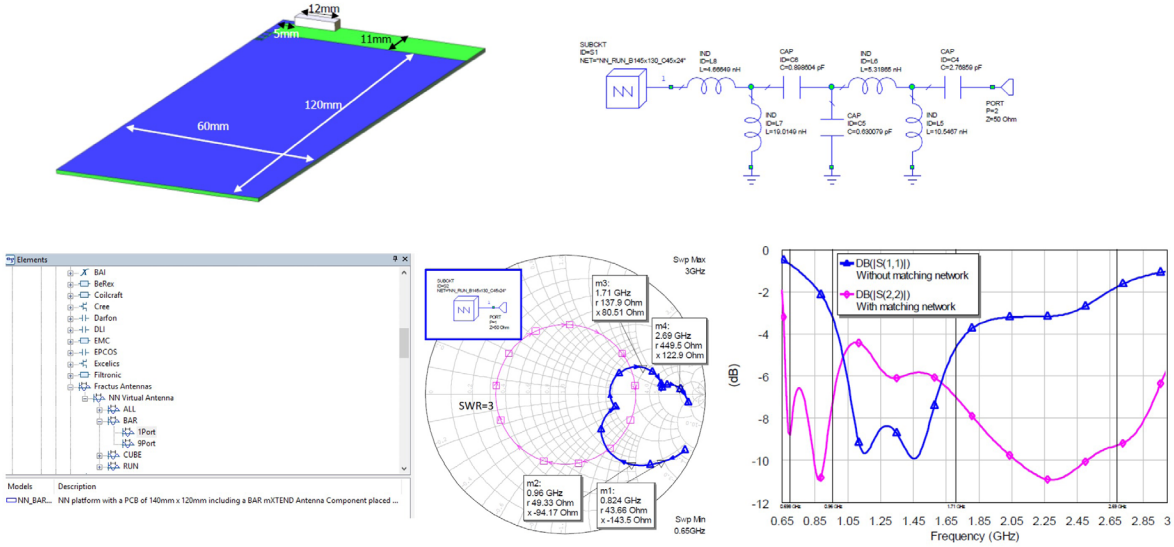

Figure 10: External impedance matching network consisting of discrete lumped-element surface-mount component is placed on the PCB to tune the frequency response of the antenna

One of the main advantages of this antenna product is that it can be easily tuned to a specific frequency region through the proper adjustment of the matching network. The impedance matching networks were developed with the AWR network synthesis wizard, a goal-driven synthesis tool that creates matching networks according to simulation measurements and user-specified performance goals. In addition to developing the matching network, AWR software and the EM tools were used to analyze the board itself to ensure that the matching circuit works properly when incorporated into a larger structure with likely parasitics.

Using the PCB import process previously described, the reference design board was imported into the AWR Design Environment platform and used to create an EM document based on a four-layer stackup. During the creation process, shape preprocessing rules were applied to simplify the via structures for faster simulation without sacrificing accuracy. The structure was easily solved in a few minutes on a single machine. A closeup view of the RF section on the right in Figure 11 shows the four-layer board with alternating signal ground planes, as well as the port definitions, which enabled the designer to insert circuit-based models for the actual matching components.

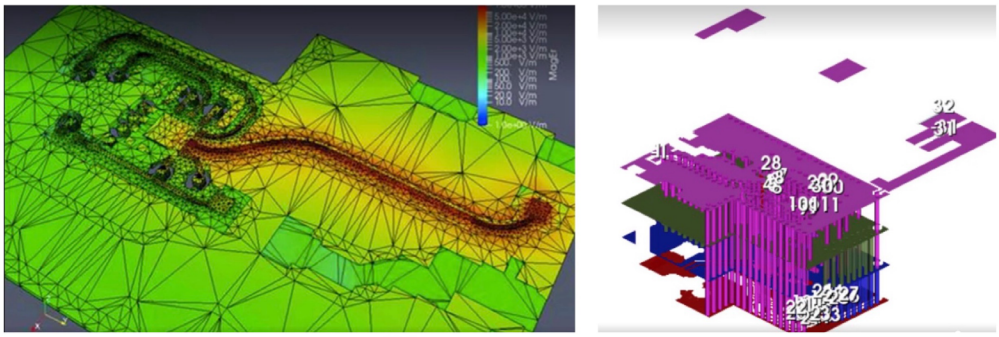

Figure 11: Four-layer PCB imported from the layout design file (Gerber) and converted into an EM document for the Clarity 3D EM simulation

For co-simulation with the circuit-based matching network components, the EM structure can be placed as a subcircuit symbol in the Microwave Office schematic editor. EM subcircuit schematic symbols are created automatically and are available for insertion into larger networks. In addition to the default symbol (box with ports), a script is available to create a custom schematic symbol using the physical layout. This feature helps the designer manage the port connections for inserting components and other subcircuits by providing a visual aid with a one-to-one representation of the EM structure layout (Figure 12). This is very useful when dealing with large number of ports and components that need to be embedded into the design. When fully assembled, the designer can examine the input impedance looking into the matching network terminated with the antenna model and embedded in the PCB design modeled by Clarity EM simulation.

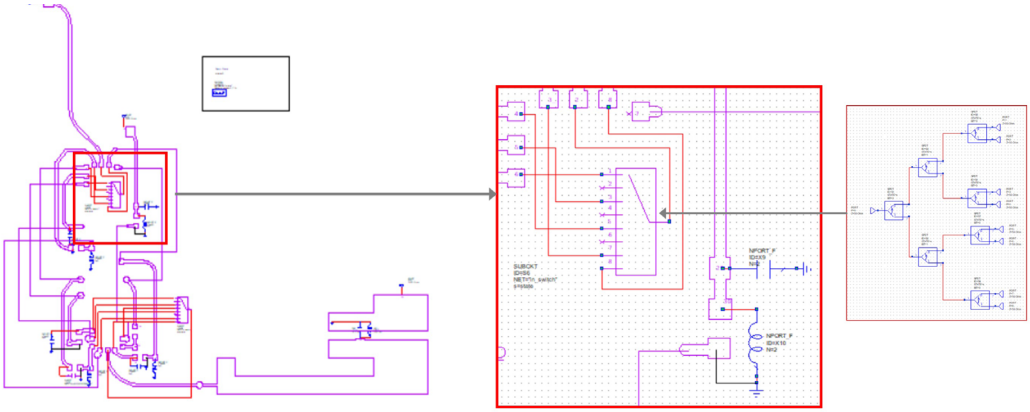

Figure 12: PCB design represented by an EM document is embedded into a larger network that includes multi-pole RF switches and band-specific impedance matching networks

The AWR/Clarity In-Design Workflow

The Clarity RF/EM in-design workflow provides EM optimization, parameterization, 3D EM libraries, and circuit co-design, as well as Microwave Office user interactive full-wave EM extraction and multi-fabric EM hierarchy support. It leverages the many automation features in the AWR Design Environment for the parameterization and optimization of EM structures using EM-based libraries and design kits to reduce design entry and management efforts, and to support circuit and EM co-simulation. RF EM in-design technology allows design teams to transition from the ideal circuit design to physical designs with EM-level accuracy, building more complex circuits in a very logical and disciplined approach that helps the design team achieve their goals in the fastest time possible.

The Clarity 3D FEM Solver can be used for the early stages of RF design, component EM modeling, circuit extraction, and optimization to uncover issues before they surface in the prototyping stage. This is possible through the design automation inherent in the AWR Design Environment platform. These capabilities include 3D EM parameterized components and model libraries, support for hierarchical EM analysis of heterogenous designs, and EM extraction-on-demand features.

EM Component Models

EM components for RF design can be developed from scratch using different methods, including the reuse of pre-existing structure models that may come from an arbitrary CAD tool or native EM components developed in AWR's 2D or 3D editors. EM-based models can be parameterized so that the designer can change their physical attributes and organized into part libraries developed by manufacturers, internal support teams, or the individual designer. For example, foundries often create process design kits (PDKs) that include EM simulation-ready passive components such as spiral inductors that incorporate process technologies, constraints, and other factors important to design and manufacturing success.

AWR software supports the simulation and integration of EM components into larger, more complex systems through its powerful design hierarchy for EM structures, which enables heterogeneous technology integration across chip, package, and board. Parametrization, optimization, and powerful parallel simulation across computer resources ensures higher performance through practical and efficient design space exploration. Adding a new Clarity EM structure to an AWR project follows the standard procedure to create, import, or link either a 3D planar or arbitrary 3D structure or import a 2D layout in the form of a DXF or GDS2 file or 3D .sat file.

When creating a new Clarity structure from scratch using the 3D planar layout editor, the user can define a new stackup and enclosure, choose an existing stackup in the projects global definitions (several support heterogenous technologies), or associate the stackup with any layout process files defined in the project. This helps designers manage multiple substrates that may be used within a single project, ensuring the circuit layout and EM structure definitions are in sync. At the same time, the amount of design entry and engineering effort needed to accelerate the overall design process reduces, making it easier for design teams to manage projects and share process technologies.

The designer can also launch the Clarity 3D workbench by clicking on the object and selecting the native editor option from the pulldown menu. This option launches the Clarity 3D workbench if the designer is interested in performing additional operations from that environment; however It is not necessary to leave the AWR Design Environment to run a simulation in the Clarity 3D Solver. Staying within the AWR environment, the EM interface to the Clarity tool supports back-annotation of simulation results for overlaying far-field and current graphics and the generation of standard Microwave Office measurement plots.

The use of 3D EM models organized into libraries offers designers an opportunity to efficiently create complex designs from individual components that are optimized for performance. In addition, scripting and parameterization allow the designer to modify these components for different requirements. A 3D EM model can be applied to a more advanced parametric QFN MMIC package model that is available in the standard 3D model library. Users can specify the number of leads, lead pitch, over-molding, the method of singulation, materials, and other package parameters and properties. The element is used in 3D EM documents and intends demonstrate the use of a 3D parameterized cell (PCell) for EM analysis.

EM Hierarchy

AWR supports hierarchy among EM blocks within a project so that the designer can properly model EM structures that are based on different substrate technologies but integrated into a single design and need to be analyzed as one. We demonstrated an example of this in the previous X-band MMIC in QFN package on PCB, a design based on three separate material stackup definitions. AWR's support for EM hierarchy allows RF module designers to use the Clarity 3D Solver to simulate systems implemented through heterogeneous technology integration. The support for EM hierarchy is especially critical in RF module design and system verification.

EM Extraction-on-Demand

The EM extraction feature automates the process of converting the layout of a schematic-based design into an EM document for EM/circuit co-design with the Microwave Office simulator. The extraction block is a control element placed directly on the schematic, which allows designers to choose individual or groups of components and subcircuits to generate a new EM document. Designers can use multiple extraction blocks in a single schematic to create multiple EM extractions for a given network.

The resulting EM document uses a stackup based on the user specified multi-layer substrate stackup definition block that can be placed in either the schematic or in global definitions. The extraction block also lets users specify the EM simulator to use, including the AXIEM, Analyst, and Clarity solvers. The simulated response for the EM document created by the extraction block is automatically inserted into the network as defined by the schematic during simulation, supporting in-situ circuit/EM co-design (Figure 13).

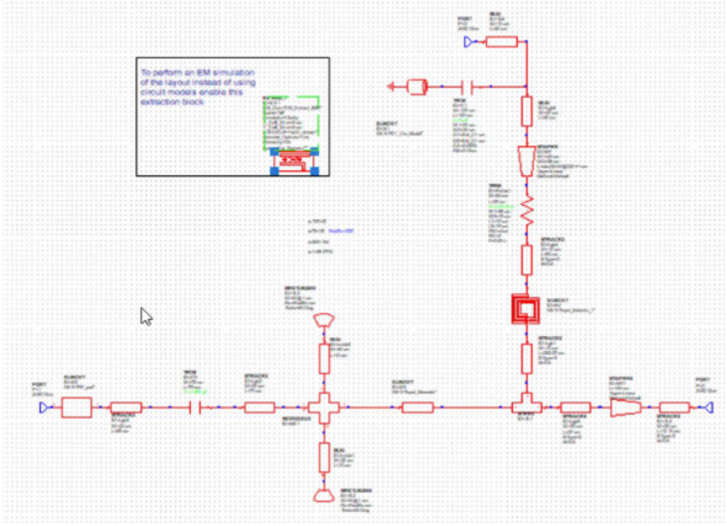

Figure 13: The extraction block enables designers to specify components within a schematic

Designers can add components to the EM extraction block through the model option tab of their property dialog box and incorporate them into different EM extraction documents. Clicking on the extraction block highlights all the components in the schematic and corresponding layout editor assigned to a given extraction block, and will therefore, be included in the generated EM document. Designers can create multiple EM documents, allowing them to compare the results from different solver technologies.

The extraction block allows designers to perform a complete MMIC extraction as part of the design verification by placing the element at the top level of the circuit schematic and selecting all the components with layout representation from the schematic (Figure 14).

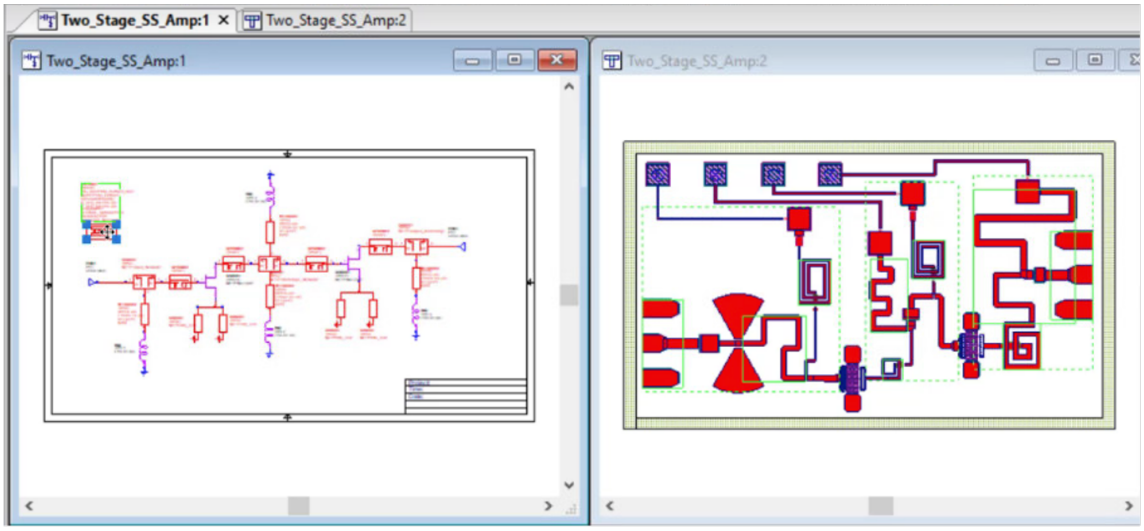

Figure 14: The extraction block allows designers to perform a complete MMIC extraction as part of the design verification

Control and measurement components such as the gamma probes can be inserted in the schematic to determine the impedances being presented to the output of the first stage and the input of the second stage using EM modeling of the interstage match without having to create individual sub-circuits and additional simulations. All these blocks are automatically assembled, along with the field-effect transistor (FET) models, to support the simulation of the entire two-stage device, where the designer can plot amplifier gain, return loss, or other metrics, such as power compression, if they have to run a harmonic balance nonlinear co-simulation along with the EM analysis.

Antenna Design Workflow

The third workflow is specific to antenna and antenna-array system design. Functionality for the development of antennas and phased-array systems within AWR software, and in particular, Microwave Office software, can be used with the Clarity 3D Solver to tackle highly integrated antenna arrays and their supporting electronics. Designers can apply AWR antenna measurements to Clarity EM analysis, enabling them to optimize antenna parameters for peak performance. Furthermore, the AWR Visual System Simulator™ (VSS) phased-array wizard can use Clarity simulation results to predict/construct user-specified phased array systems (Figure 15).

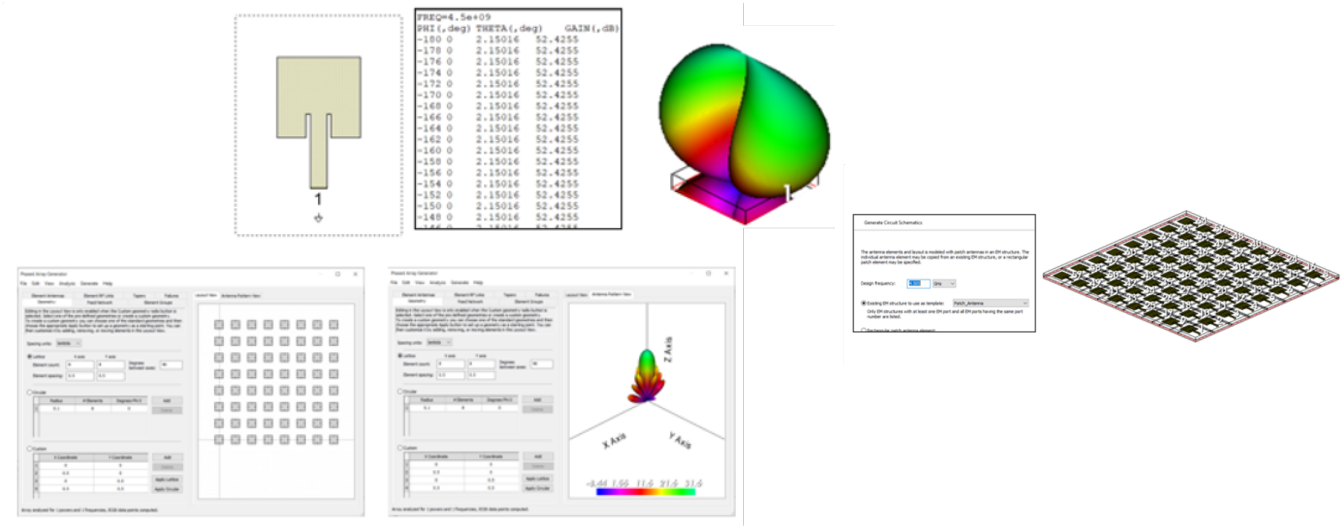

Figure 15: The entire phased-array system, from one element to 64 elements, can be developed with the VSS phased array wizard and simulated with the Clarity solver

Using either the AXIEM planar or Clarity 3D Solver, designers can simulate a single element to obtain a radiation pattern, define the array configuration (number of elements, orientation, and spacing) using the phased-array wizard, and assign a radiation pattern to an individual element and review the resulting array far field versus steer angle, power, and frequency derived through superposition of the contributing radiation patterns. Different radiation patterns can be assigned to individual elements based on their position in an array to account for differences in the radiation patterns as would occur between corner, edge, and center antenna elements. Designers can apply gain tapering, feed network, and element link definitions such as insertion loss and power compression characteristics.

The information supplied to the phased array generator is used to create an entire phased array system schematic that includes a feed network using the electrical responses of the defined RF link and a physical array based on the specified number of elements, spacing, etc. The generated physical array uses ideal rectangular patch antennas for the individual elements unless the user specifies an existing antenna geometry from the project. Therefore, a designer can use the radiation pattern and physical design of a single antenna to quickly synthesize a physical array ready for EM analysis using the user specified simulator of choice (AXIEM, Analyst or Clarity). Furthermore, the array is part of the complete system diagram that is composed of subcircuits containing the power splitters and parameterized phase shifters/gain control blocks that support beamsteering from the top level.

With the phased array generator, engineers can rapidly develop their early design to develop a physical array for more rigorous EM analysis, replace ideal behavioral blocks with more detailed RF components models, and develop the routing between the beam steering / RF front-end electronics and the individual antenna elements.

Antenna Array with Feed Structure Example

An electronically large array, including its feed structure, was simulated with the Clarity 3D Solver within AWR software. The design included a 2x16 element array and feed structure in which the antenna elements were based on tightly coupled dipoles. The design also included a corporate feed based on a multi-layer PCB construction, internal baluns (32), tapered transmission lines (impedance x-formers), and a through-substrate feed out to the patch.

Using a traditional finite-difference time-domain (FDTD) solver, the simulation took about one week and about 200GB of RAM. Table 1 shows the results, where the Clarity 3D Solver was used for the same simulation, took about 6 hours using eight cores and 1 hour 45 minutes using 64 cores. The Clarity 3D Solver took just under an hour to complete the initial mesh and the adaptive mesh took just under 24 minutes with 8 cores and just under 13 minutes with 64 cores. The Clarity 3D Solver quickly and easily solved this hefty problem with a fair number of elements and over 10 million unknowns.

Table 1

# cores	Initial mesh	Adaptive mesh	Sim. Run time	Total time	# of frequencies	# of elements	# of unknowns
8	0:51.31	0:23:49	5:5:31	6:21:07	182	2,423,906	10,916,034
64	0:51.55	0:12:45	0:42:26	1:47:23	118	2,423,906	10,916,034

Conclusion

This paper highlights recent technology trends in system integration that are driving the need for EM analysis with the capacity to solve large-scale problems directly from within the design platform. RF/mixed-signal systems that utilize heterogeneous technologies such as RFIC, MMIC, SiP/PiP, advanced modules, and PCBs, are particularly susceptible to failure due to unforeseen EM issues that occur with the move to higher frequencies and levels of integration. This paper demonstrates that Clarity 3D EM Solver and its massive parallelization, unique decomposition algorithm, and automatic mesh refinement solves larger, higher-capacity problems much more efficiently than traditional EM simulators. This paper also presents multiple workflows showing the integration of Clarity within the AWR Design Environment to support design verification, RF in-design, and antenna/antenna array system design.