The Cadence® Allegro® PCB Router — an integral part of the Allegro system interconnect design platform — is the market’s leading solution for automatic and interactive interconnect routing. Designed to handle routing challenges from simple designs to high-density PCBs requiring complex, high-speed design rules, the Allegro PCB Router uses powerful shape-based algorithms to make the most efficient use of the routing area. The result is increased productivity and shorter design cycles.

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect — between I/O buffers and across ICs, packages, and PCBs — to eliminate hardware re-spins, decrease costs, and reduce design cycles. The Allegro constraint-driven flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With silicon design-in kits, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter™ and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.
FEATURES

- Available on Windows, UNIX, and Linux operating systems with licensing that floats between platforms
- High-speed rules/constraint support for delay, crosstalk, impedance control, differential pair, and net scheduling — including virtual pins
- Real-time routing to net scheduling, delay, crosstalk, impedance, and differential pair rules
- Auto net shielding with auto via stitching
- True 45-degree or orthogonal routing
- Full Microvia structure support
- Layer Set routing
- Recursive mitering engine for hand-routed-looking results
- Interactive routing and component floorplanning capabilities
- Automatic component floorplanning
- Seamless integration with Allegro PCB Editor, Allegro Package Designer 610, and Allegro PCB SI 610
- Interfaces available for Mentor Board Station and Mentor PowerPCB

HIGH-SPEED, RULES-DRIVEN ROUTING

Allegro PCB Router high-speed features provide the capabilities to handle net scheduling, timing, crosstalk, layer set routing, and special geometry requirements demanded by today’s high-speed circuits.

NET TOPOLOGY

Net topology scheduling defines the routing order of the pins on a net and even insert intermediate routing points known as T-points. This allows designers to apply constraints to each segment of the schedule for precise interconnect control, even when a net contains a discrete device such as a termination resistor. With every topology-constrained net, you can control the length of your conductors using delay or length specifications. You can also define the minimum or maximum conductor delay or length to ensure a particular signal arrives at its destination within a specified time period.

CROSSTALK

Crosstalk is limited by geometric or parallelism rules. You can define the acceptable gap and length parameters, and the Allegro PCB Router automatically separates the parallel lines after a specified distance. You can also create a gap versus length table to more accurately model crosstalk. Crosstalk is reduced by evaluating the geometric or physical layout of conductors and the electrical properties of signals carried by the conductors. Noise associated with conductors both on the same layer and adjacent layers is considered. Cumulative noise crosstalk is controlled by coupled noise rules that incorporate the design’s electrical properties. Users can define the maximum cumulative crosstalk noise in millivolts allowed by each class or net. PCB Router dynamically computes the maximum cumulative crosstalk noise during routing by adding all parallel and tandem conductors.

LAYER SET

Layer Set routing defines routing layer “sets” and uses them to control routing. During routing of impedance controlled trace(s) or buses, a layer change may be necessary in order to complete routing. These changes in layers, if not controlled, can cause changes in impedance based on where the new layer is located in the PCB stack up. To eliminate this problem, the desired target layer(s) will have the same characteristic impedance as the source layer. The Layer Set feature allows the definition of a number of layer sets on which the net or bus is allowed to be routed. This is usually related to the similar impedance values of those particular layers in the set. Layers not included in the set will not be available for routing.

DIFFERENTIAL PAIRS, SHIELDED NETS, AND AREA RULES

PCB Router also has the flexibility to handle the special geometry requirements of high-performance designs. For differential pair routing, users define the gap between the two conductors and the autorouter takes care of the rest. PCB Router intelligently handles
Shielded signals get auto-generated shields with vias inserted at user-defined intervals, tying the shield to the ground layer.

Routing around or through vias and automatically conforms to any defined minimum length criteria. Automatic net shielding is used to reduce noise on noise-sensitive nets. Separate design rules may be applied to different regions of the design. For example, you can specify tight clearance rules in the connector area of your design and less stringent rules elsewhere.

With signal margins shrinking rapidly, the use of net shielding is becoming commonplace on most high-speed designs. In order for net shielding to perform correctly, a shield needs to be connected to the ground plane at regular intervals so that any stray noise can be effectively absorbed. PCB Router not only auto-generates the shield around specified nets, but it also ties the shield route to the chosen ground plane by automatically inserting vias at specified distances.

ADVANCED PHYSICAL RULES

The advanced rule set feature within PCB Router enables electrical parameter control, crosstalk reporting, and conductor-length rule violations—requirements demanded by today’s large designs. Electrical parameter controls include the flexibility to assign specific rules to each element in your design. Users define the rules required to meet the electrical class characteristics unique to each layer, via type, conductor width, or set of connections. Using this feature, a larger via can be used to support the increased current capacity required by power and ground connections. This conserves design space because only the selected signals use larger vias. Additionally, you can improve signal impedance matching by assigning different width and clearance rules to different layers.

Outer layers generally have higher impedance and are assigned larger conductor widths. Inner layers generally have lower impedance and are assigned narrower widths to match the impedance of the outer layers. Impedance matching can also be improved by controlling routed nets on certain layers or layer pairs. Reports include coupled noise by using the geometric or physical layout of conductors and electrical properties of signals. Noise associated with signals on the same layer and on adjacent layers is considered. Possible timing problems are reported by showing minimum and maximum wire length violations. All of this information is reported in a file and displayed graphically.

MICROVIA RULES

With today’s dense multilayer designs, many companies are considering the benefits of multilayer build-up technologies that employ new manufacturing techniques to greatly reduce board size and layer count and to increase signal performance. One of the major requirements for these new build-up technologies is the support of complex via structures. The Allegro PCB Router Microvia functionality was developed with Matsushita for the support of Matsushita’s industry-leading ALIVH technology. This option includes support for plural vias (i.e., a cluster or array of vias), which allows for greater current capacity in wide traces. Stacked vias permit blind and buried vias to be stacked in the same X-Y location on different layers of the board. Enhanced via fanout allows blind and buried vias under SMD pads. When the Microvia feature is selected, the fanout feature allows stacked vias under SMD pads even when there are pads directly opposite each other on both sides of the board.

ADVANCED SUBSTRATE RULES

PCB Router provides capabilities to handle blind or buried vias, wirebonding, and vias under surface mounted pads—requirements demanded by today’s ceramic PCB and IC packages. Blind and buried via controls automatically use blind or buried vias when required, to transition between layers. You control the clearance between vias on different layers as well as the clearance between adjacent vias on the same layer. You can place a via under an SMD pad at the origin or at the grid point nearest the origin. You can also control whether vias placed under SMD pads fit entirely within the boundary of the pad. If the via shape on the pad layer extends beyond a pad’s boundary, the via is not placed. Wirebond support automatically handles devices that require wirebonding. Bond sites are placed and automatically routed with discrete wires from each site to the pads of a chip mounted on the PCB. You define the type of bond site and the maximum acceptable distance between the component pad and the bond site.

DESIGN FOR MANUFACTURING

The PCB Router’s design for manufacturing capability significantly improves manufacturing yields with a spread command that automatically increases conductor clearances on a space-available basis. It also miters corners and adds test points automatically after autorouting.
Automatic conductor spreading is used to improve manufacturability by repositioning conductors to create extra space between conductors and pins, conductors and SMD pads, and adjacent conductor segments. Users have the flexibility to define a range of spacing values or to use the default values. Miter corners automatically replace 90-degree corners with a chamfer by using either the default or a user-specified setback value. You can miter corners throughout the entire design or on specific layers and specify a single value or a range of setback values. The design for manufacturing capability automatically uses the optimal setback within the range, starting from the largest to the smallest value.

**TEST POINT INSERTION**

Test point insertion automatically adds testable vias or pads as test points. Testable vias can be probed on the front, back, or both sides of the PCB, thereby supporting both single side and clamshell testers. You have the flexibility to select the test point insertion methodology that conforms to your manufacturing requirements. Test points can be “fixed” to avoid costly test fixture modifications. Test point constraints include test probe surfaces, via sizes, via grids, and minimum center-to-center distance.

**ALLEGRO PCB ROUTER PLACEMENT EDITOR**

The Allegro PCB Router Placement Editor allows you to place components quickly while simultaneously evaluating space, logic flow, and congestion before beginning to route your PCB.

**Move mode** allows components to be flipped, rotated, aligned, pushed, and moved either as individual components or as a group.

**Guided-place mode** selects the component with the highest connectivity and computes an optimal placement location that does not violate design rules or constraints. Users have the option of accepting or rejecting the location. You can also place components by directly entering their X-Y locations. This is particularly useful for placing connectors and components with fixed locations.

**Density analysis** graphically displays circuit congestion by overlaying the PCB with a color map showing highly congested areas in relation to lightly congested areas. This helps you determine where placement adjustments might be made to relieve congestion and improve routing.

**ALLEGRO PCB ROUTER AUTOPLACEMENT**

Allegro PCB Router autoplacement is a shape-based automatic component placement program that supports boards with 256 routing layers and unlimited component pins. It allows placement of components without the need for grid definitions or length setup for different size components. Autoplacement allows you to place some components interactively while automatically placing others. Rooms can be defined for split power, height constraints, power dissipation, or for separation of analog, CPU, memory, TTL, and ECL circuitry. It can position components on both sides of the PCB simultaneously with front-to-back alignment of SMDs. To address the needs of pick-and-place machines, spacing rules can be defined by layer, component type, or specific component.

**ROUTE EDITOR**

The fully integrated Route Editor revolutionizes the editing process with its advanced routing and editing capabilities.

**PLOWING, SHOVING, AND GHOSTING**

As new conductors are routed, the plowing feature automatically pushes existing conductors aside and routes around pins. Using the shoving feature, you can move conductor segments or vias against existing traces and push ahead — over other pins and vias if necessary. The ghosting feature makes the evaluation of “what if” scenarios easy. As a conductor segment or via is moved under cursor control, the surrounding conductor is shoved and displayed dynamically. You evaluate the adjusted routing before accepting a final configuration. Additionally, a multilevel undo feature allows you to revert to previous routing configurations.

**ADVANCED EDITING FEATURES**

On dense, multilayer boards, legal via sites can be difficult to find. The Route Editor lets you position vias by simply clicking twice at a chosen location. If possible, the chosen site is used by shoving conductors aside on layers as needed. Otherwise, Route Editor displays a design rule violation and shows the legal via sites nearby. Copy route simplifies bus construction by letting you copy an existing route to complete unrouted bus connections. The new route uses the same topology with length automatically adjusted. Route Editor also lets you use the cornering option that works best for your design requirements. Use orthogonal, 45-degree, or all-angle routing — Route Editor will automatically snap corners to your preference. The critic function removes extra bend points created during the editing process. Select the area of interest, or the entire board, and critic simplifies routing to improve manufacturability.

**LENGTH RULES AND TIMING CONSTRAINTS**

With the high-performance rules in Route Editor, you can easily route nets to satisfy timing constraints through the dynamic application of minimum and maximum length rules. Two innovative graphical techniques are provided to help you route nets with timing constraints. First, there is a display that details length information...
through a color-coded meter that is updated as you route. This shows whether your route is satisfying minimum and maximum length constraints. The meter display is controlled by adding the distance routed to the remaining Manhattan length to the target. This instantaneous feedback keeps you on track and shows you the amount of length you have left as you route. Second, a graphical display also provides a more global view of whether you are meeting timing constraints. A green polygon displays around the current cursor location and the target pin if you are within a maximum defined length. The polygon does not display if the maximum length will be exceeded. A red polygon displays when minimum length is violated.

**ALLEGRO PCB ROUTER FEATURES**
- Routing of up to 256 signal layers
- True shape-based routing or grid-based autorouting
- SMD fanout to vias
- 45-degree ECO routing
- Memory bus routing (SMD or through-hole)
- Multipass recursive miter
- Via rules by net or net class
- Wire and clearance rules by layer
- Net/net-class rules by layer
- Soft and hard fences
- Layer set routing
- Automatic wire spreading
- Automatic test point generation
- Blind, buried, and micro vias
- Vias under SMD pads
- Automatic wirebonding
- Automatic gate and pin swapping during routing
- Parallelism control
- Accumulative noise control
- Maximum/minimum/matched delay and length control
- User-defined elongation methodologies
- Automatic differential pair routing
- Rules/clearance by area
- Net shielding
- Virtual pins for topology control

**PLACEMENT EDITOR FEATURES**
- Online design rule checking
- Floorplanning
- Guided placement mode
- Flip, rotate, align, push, and move individual components or groups of components
- Placement density analysis
- Direct X-Y location component placement

**AUTOPLACEMENT FEATURES**
- Automatic, double-sided component placement
- Rules by layer, component, and/or component type
- Automatic gate and pin swapping
- Auto-clustering

**ROUTE EDITOR FEATURES**
- Plowing, shoving, and ghosting
- Interactive via search
- Online design rule checking
- Automatic routing clean-up
- Online meter displays length tolerance
- Global violation indicator
- Dynamically calculates and displays available slack
- Color feedback on all indicators and meter
- Multiple net (bus) routing
- Automatic single net autorouting

**OPERATING SYSTEM SUPPORT**
- Red Hat Linux 7.3, 8.0
- Windows 2000 with Service Pack 2, XP Professional
- Sun Solaris 7, 8, 9
- HP-UX 11.0, 11.11
- IBM AIX 5.1

**CADENCE SERVICES AND SUPPORT**
- Cadence application engineers can answer your technical questions by telephone, email, or Internet — they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions — 24 hours a day, 7 days a week — including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more
## Allegro PCB Router feature summary for Allegro PCB design 200 & 600 series

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### Automatic single-net routing
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### Multiple net/bus routing
- PCB Performance

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**FOR MORE INFORMATION**

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or value-added reseller (VAR) in your area, visit www.cadence.com/contact_us.