Allegro System Capture

System architecture design and implementation for multi-board PCB systems

System architecture design and implementation are disconnected, which makes creating a system that meets cost, performance, and formfactor requirements challenging. Hardware designers need tools that help them engineer their system to meet their end products' goals within the time-to-launch window. Cadence® Allegro® System Capture is a scalable and easy-to-use solution for fast system design intent creation that allows the high-level system architecture and functional diagram to stay connected to the detailed implementation of each board.

Overview

Allegro System Capture is a scalable solution for engineering a multi-board electronic system. It provides an intuitive, easy-to-use environment for hardware designers and architects to engineer a system that is correct by construction, enables partitioning a system into multiple boards, and ensures that the system assembly and connectivity are current from the beginning and throughout the design process. It also enables the high-level functional and architectural description of the multi-board system to stay in sync with the detailed implementation of each of the boards in the system.

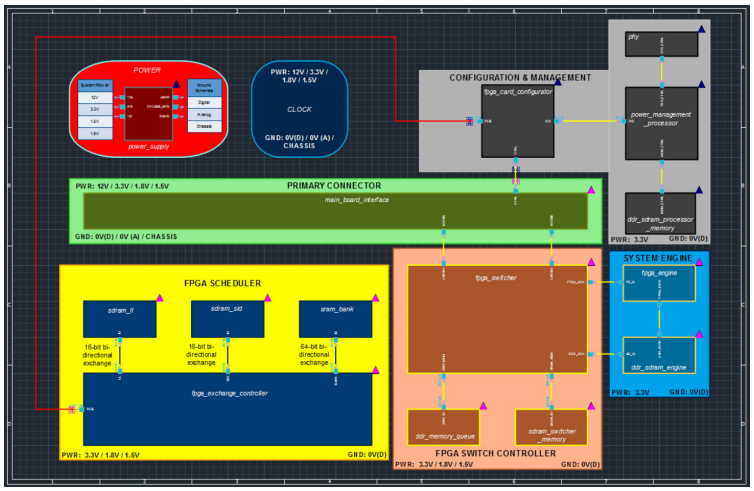

Figure 1: Electronic system definition that drives the detailed implementation

Benefits

- Shorten time to create a multi-board system definition
- Keep a high-level functional definition in sync with detailed board-level implementation
- Quickly validate system assembly early in the design cycle (to avoid building "paper doll" models or other manual techniques)
- Ensure system connectivity is consistent with the design intent throughout the design process
- Shorten time to create schematics for a board

System Definition and Functional Block Diagrams

Most hardware engineers use Microsoft's Visio or PowerPoint applications to describe the high-level architecture of their system of boards. In almost all cases, the functional diagram and detailed implementation are disconnected, which leads to a longer system-definition time. With Allegro System Capture, you can keep the high-level definition of a system synchronized with the detailed implementation of each of the boards that make up the system. Hardware architects can hand off their system blueprint to the next phase of the design process, where a functional block diagram can be created that has more information for detailed implementation. Engineers can define details of connectivity, use notes to communicate intent or requirements, and add in images to identify different sub-sections, all while creating a functional block diagram that can be linked to the detailed implementation.

Partitioning and Assembly Integrity

With Allegro System Capture, engineers can functionally partition a system and graphically identify the various functional blocks that make a physical board. With the partitioning integrated with the higher level functional diagram, extended teams can provide input and feedback on the impact of the partitioning decisions earlier in the design cycle, such as, will the boards all fit into the enclosure, will the assembly of boards meet the cost targets, and will the critical signals have expected performance after crossing a board boundary? If initial architectural proposals are not practical, re-partitioning can be performed and the re-partitioned design can be returned to the design teams.

In addition, engineers can also ensure that the right connectors are chosen during the partitioning process for size and compatibility by viewing the 3D models of the connectors. This allows them to avoid surprises later in the design cycle with mismatched connectors or mismatched connector orientations.

System Connectivity Integrity

With the system definition and detailed implementation disconnected, designers of multi-board systems must manually check connectivity across boards to ensure system connectivity integrity. This manual effort often involves writing utilities to extract data from the board files, then comparing the extracted data in a spreadsheet. Any errors in this process or lack of rigor to check it before the designs are handed off to manufacturing will result in an unnecessary spin of the board(s) to match the right signals on two sides of the mating connectors.

With Allegro System Capture, the system connectivity integrity is maintained. Any change on one board that wasn't matched on the corresponding board will be identified, thereby avoiding any surprises in the system integration test in the lab.

Signal Traceability

With integrated high-level and detailed implementation within Allegro System Capture, tracing a signal across a board is easy. It saves a lot of time for engineers when they are reviewing the design and also during the debug stage in the lab.

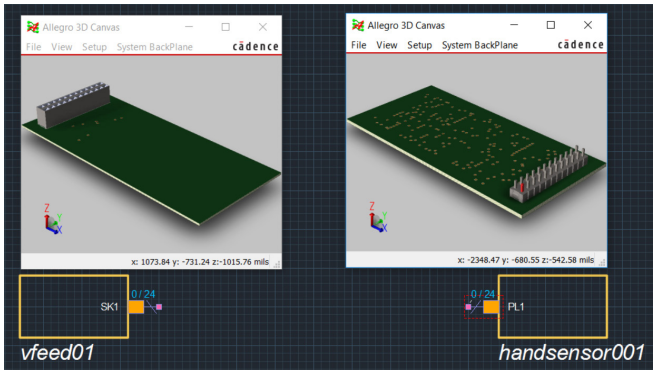

Figure 2: View connectors on bare boards earlier in the design cycle to ensure connector compatibility and correct orientations

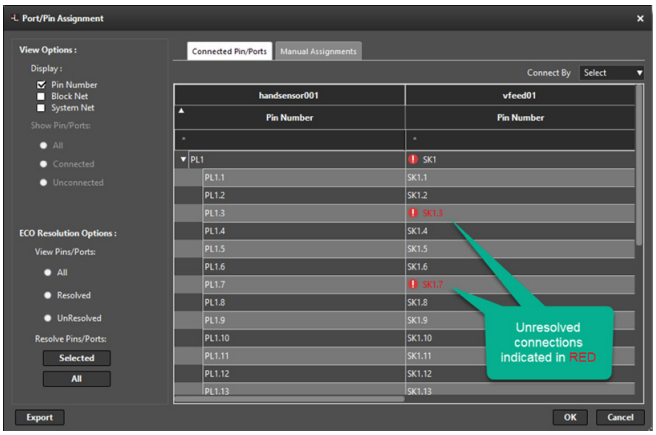

Figure 3: System connectivity mismatches identified and highlighted for users to resolve

Schematics for a Board

Allegro System Capture provides engineers with a modern, intuitive, easy-to-use environment to create detailed schematics for a board. With traditional schematic capture tools, engineers tend to spend a lot of time placing symbols and connecting pins. Allegro System Capture provides powerful connectivity modes that are 2X to 5X faster than traditional schematic creation tools. It also provides a way for engineers to place decoupling capacitor rails 10X faster on schematic pages near active components with only a few clicks. With online DRC and packaging on the fly, Allegro System Capture allows engineers to create schematics faster and to shorten the time to start the PCB layout process.

Schematic Validation

Allegro System Capture comes with a set of schematic checks to prevent common errors in creating schematics. These checks can be customized and new checks can be written for a company's design review needs.

Customers who have created custom rules in Allegro Design Entry HDL (DE-HDL) can reuse these checks with Allegro System Capture, preserving their investment.

Design Reuse

Most new schematics reuse some portion from previous designs. Allegro System Capture provides multiple means of reusing portions of previous designs—from simple copy and paste from a design to single- or multiple-page reuses to complete block reuses. Constraints specified on the design come across to the new design, ensuring that the complete design intent is reused, not just the graphics.

Allegro System Capture further allows you to create "reuse" blocks and place them in a library for use in other designs, just as with components. The connectivity, constraints, and layout from each block can also be reused. The same block can be used multiple times in the same design without renaming or copying.

Allegro System Capture also allows users to reuse portions of existing designs created in Allegro Design Entry HDL (DE-HDL) and Allegro Design Entry CIS (DE-CIS), preserving their investment. With Allegro System Capture, logical and physical design reuse is simpler, better, and faster.

Design Variants

Many designs in several market segments have design variants. With Allegro System Capture, you can conserve even more time and effort at the structural level. The design variants capability eliminates having to create slightly different versions of the same basic design—for example, offering graduated performance levels to different market segments, or addressing varying regional requirements. It enables you to derive variants of a single base design by assigning alternate sets of attributes to the components, wires, or other elements of the design. An engineering change order (ECO) applied to the base design automatically propagates to all its variants.

Allegro System Capture displays variant information on the schematics showing DNI components marked with "X", as well as display components in a different color if a property is modified for a variant of the design (10K versus 5K, for example). It also provides a variant table editor to enable manipulation—change value, cut and paste, etc.—of multiple entries of properties or status of components across multiple variants.

High-Speed Design

Constraints are critical to creating true design intent. Allegro System Capture provides a simple, easy-to-use docked constraint manager to specify electrical constraints on a selected set of nets as they are created on the schematic canvas.

Allegro System Capture also provides full access to Allegro Constraint Manager, which is used with Allegro PCB Editor for PCB layout and routing. Having a single constraint manager prevents misinterpretation of constraints between the front-end design creation process and back-end PCB layout and routing process. This ability to specify electrical constraints enables a constraint-driven PCB design flow that is proven to shorten the overall design cycle, and helps you get the design right the first time. Advanced features include the ability to automatically extract, use, and override constraints from blocks added to the design.

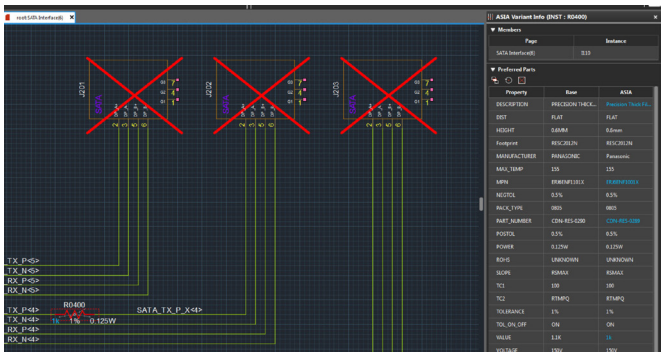

Figure 4: Variants shown on the schematics with DNI components and components, with value differences shown in different colors

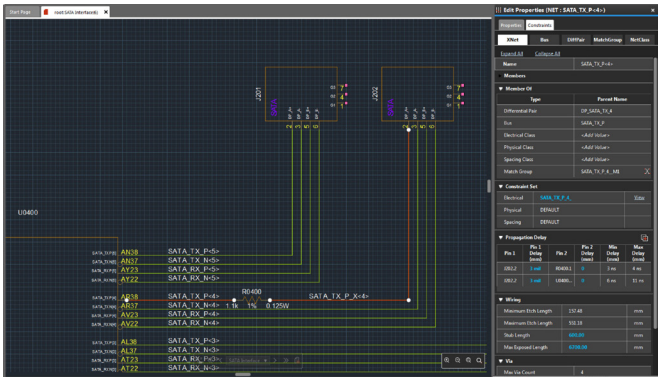

Figure 5: Docked constraint manager allows engineers to easily specify constraints on selected or recently created nets

Allegro Constraint Manager presents constraints through several separate worksheets for different types of electrical constraints. It allows you to capture, manage, and validate the different rules in a hierarchical fashion. Allegro Constraint Manager enables you to group all the high-speed constraints for a collection of signals to form an electrical constraint set (ECSet). This ECSet is then associated with all the nets in the group. As the rules are embedded in the design, the PCB layout designer can concentrate on optimizing the physical layout for size, routability, and manufacturability, while the software automatically communicates compliance with the engineer's performance requirements.

Concurrent Team Design

For many if not most companies, system design authoring is a team effort. Team system design authoring enables multiple design engineers to collaborate asynchronously in the hierarchical development of a system's definition. A schematic can be partitioned into user-defined levels of hierarchy and distributed to the defined members of the engineering team, providing them with an isolated "sandbox" for the development and verification of their partition(s).

Allegro System Capture provides team assignment and notification capability to assign engineers to specific blocks they are responsible for. It provides a dashboard view of the current status of each team member's block. This solution provides much-needed flexibility for large time-critical projects while accelerating the design creation process.

Schematic-Driven Placement

There are many instances where placement on the layout must be driven by the symbol placement in schematics. Allegro System Capture enables two-way cross-probing with Allegro PCB Editor to locate components in the schematics and vice versa. To help in the placement phase, you can place components in Allegro PCB Editor by

selecting the components in the Allegro System Capture canvas. You can also place all components on a schematic page in a single step in Allegro PCB Editor.

In addition, engineers can specify component association between an active device and associated decoupling capacitors, as well as maximum distance between the decoupling capacitors and the power/ground pins on the active component. This specification enables PCB designers to quickly place decoupling capacitor within the required distance. With this association, Allegro PCB Editor shows a circle from the pin being decoupled to place the capacitor, accelerating the overall layout process as discrete components in many instances make up over 66% of the components to be placed on a PCB.

Customization and Extensibility

Allegro System Capture enables customization and allows users to extend the capabilities provided out of the box through a TCL (an interpreted, general-purpose, high-level programming language) interface. Engineers can write TCL programs to customize Allegro System Capture and create custom commands. The custom programs can be used for querying and modifying the design data in the system. By placing these programs in a common area, it's possible for a team to share the efforts of all team members.

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
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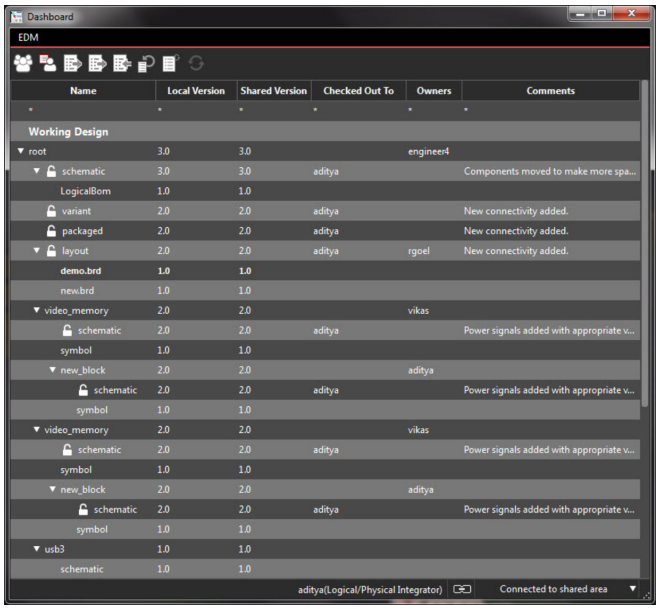

Figure 6: Team design dashboard provides status of every member's block of design

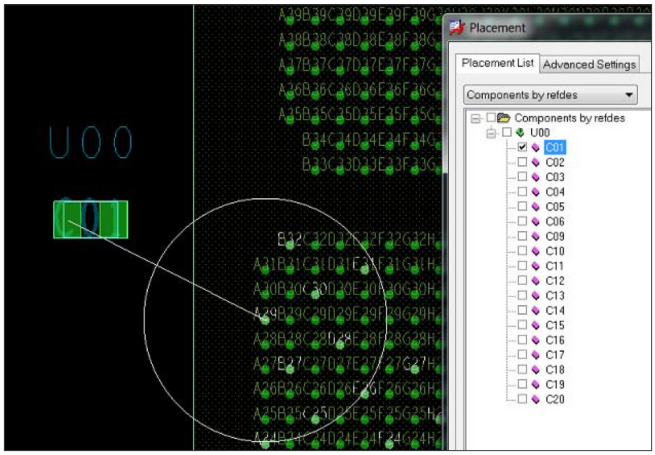

Figure 7: Component association and placement radius accelerate placement of discretes on the PCB

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