What’s New in PSpice 16.6
Learning PSpice

• Reduces the Time to get started with PSpice

• Content addresses the basic concepts of Electrical Engineering with Samples

• Infrastructure for Application Notes!!
Quick PSpice Parts Place Menu

- Allows quick place of commonly used PSpice Parts without any library setup requirements
- Implementation done through Menu XML/TCL
“What-If” Analysis

- Undo-Redo information is preserved on PSpice Netlist
- Enabled Quick “what-if” scenarios on schematic for PSpice simulations
- Overall reduction in time to finish designs
Engine Options

• Performance of Multi-Core enabled
  – Focused performance enhancements for large designs with complex model instances like MOSFETS, BJT

• I/O Performance
  – Significant performance for large DAT files
New PSpice Options – Speed

• THREADS
  – Maximum number of threads to be used for simulation
  – THREADS = 1 => Single-threaded simulation
  – THREADS = 0 => Use default calculation
  – By default, number of threads is calculated based on device count, number of cores in the machine, and PSpice license.
  – Default thread count is <= number of cores/2
  – Maximum 4 threads can be used for regular PSpice Licenses
Enhanced PSpice Engine Options

• Convergence Improvement Options
  – Advanced Biaspoint Convergence Homotopies
  – Integration method option
  – Node Value Limiting
  – Relative Tolerance

• Accuracy Improvement Options
  – Worst-case control independent of RELTOL
  – Behavioral sources TimeStep Control for sinusoidal functions
  – MinStep independent of TSTOP
  – 64-Bit Data accuracy
Biaspoint Convergence

- **PSEUDOTRAN**
  - Bias-point Convergence Enhancement
  - Used when all other methods (STEPGMIN, STEPSOURCES) have failed

- **ADVCONV**
  - Enables all convergence algorithms, viz. PseudoTran, StepGmin, and StepSources (ON by default)

- **GMINSRC**
  - Enables StepGmin from inside of StepSources

- **NOSTEPDEP**
  - Suppresses stepping of dependent sources during StepSources
Biaspoint Convergence

• PSEUDOTRAN
  – Bias-point Convergence Enhancement
  – Used when all other methods (STEGMIN, STEPSOURCES) have failed

• ADVCONV
  – Enables all convergence algorithms, viz. PseudoTran, StepGmin, and StepSources (ON by default)
  – Usability option to enable all convergence techniques in a single switch
Biaspoint Convergence

- **GMINSTEPS**
  - Maximum number of steps per iteration of StepGmin

- **ITL6**
  - Maximum number of steps per iteration of StepSources

- **PTRANSTEP**
  - Maximum number of steps per iteration of PseudoTran

These 3 are just to give additional control to Power users.
Transient Convergence

- **METHOD = [TRAPEZOIDAL|GEAR|DEFAULT]**
  - Integration method to be used during Transient analysis
  - Gear is more stable, so more often used in the default mode
  - Trapezoidal is more accurate

- **TRTOL**
  - Tolerance for integration error calculated during transient analysis
  - A higher value implies more tolerance, so bigger time steps and reduced accuracy
  - Can be useful to jump model discontinuities in case of fast-switching designs
  - Default = 7
New PSpice Options

• LIMIT
  – Absolute limit on data values calculated in PSpice engine during simulation
  – Can be used in case of overflow errors
  – Can also be useful for convergence failures in some simulations

• WCDEVIATION
  – Deviation to be used for Worst-case analysis
    • Default calculation for worst-case Delta is nominalValue * RELTOL
    • If WCDEVIATION is specified, it gets modified to nominalValue * WCDEVIATION
PSpice Options

Accuracy

• **PROBE64**
  – 64-bit Probe data
  – Increases resolution of probe
  – Very useful for differential probes

• **NOGMINI**
  – Suppress GMIN addition across current sources
  – Gives more accurate results for very low current values

• **BRKDEPSRC**
  – Sets automatic break-points for sinusoidal behavioral sources
  – Useful for long simulations when default Max Time Step is too big
Enhancement for behavioral sources

• VT Tables
  – Optional parameter for Table-driven behavioral sources
  – Tells simulator that x-axis of the Table represents Time
Run-time Convergence Settings

- Run-time settings support enabling Convergence Homotopies and configuration without simulation re-start.
Hands-On

- Node Value Limiting
- Runtime Settings
- Accuracy
- Psuedotran
PSpice IBIS Import

- Spice circuit generation for all IBIS versions
- Supports V-t curves
- Enables Analog simulation of XNets
  - Use Advanced Analysis tools for smoke analysis on bypass components
Securing PSpice Models

• AES Encryption added

• Key Length increase – 256-bit key used

• Multiple Modes of Encryption supported

• User-Defined Encryption supported

**ed Encryption:**

- Define variable CDN_PSPICE_ENCKEYS into a csv file which contains <filename>, <key> pairs

**-line usage of PSpiceEnc**

```
cept [-e/E | -i/I | -n/N | -p/P] [-mode <>] inputFilePath outputPath
```

- Use the old SPB 16.5 Encryption scheme.
- Special encryption available only in selected builds (for ST).
- Use DES Encryption with advanced data security (available)
- Use AES Encryption (default for SPB 16.6).

**cmds for each mode:**

- NENCSTART
- NENCSTART_CENC1
- NENCSTART_ADV2
- NENCSTART_ADV3

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## Expanding PSpice Library Models

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<thead>
<tr>
<th>Model Type</th>
<th>Library</th>
<th>Number of New Models</th>
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<tbody>
<tr>
<td>Schottky Diodes</td>
<td>Schottky.olb</td>
<td>105</td>
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<tr>
<td>Bridge rectifiers</td>
<td>diode_fullbridge.olb and</td>
<td>119</td>
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<td>dual_diode.olb</td>
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<tr>
<td>High Speed Diodes</td>
<td>Diode.olb</td>
<td>26</td>
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<tr>
<td>Zener Diodes</td>
<td>Zener.olb</td>
<td>11</td>
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<tr>
<td>New Ferrite material’s core models for Power application &amp; Signal</td>
<td>Magnetic.olb</td>
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<td>Controllers for Switching Regulators (Step Up, Step Down, LED Drivers</td>
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<tr>
<td>and Synchronous Controller)</td>
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<tr>
<td>Power Management: Special purpose IC's</td>
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<tr>
<td>IGBT Module</td>
<td>IGBT.OLB</td>
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