Virtuoso® Schematic Editor is the design composition environment for the Virtuoso custom design platform. From architectural definition using industry-standard language representations to final structural implementations done graphically, Virtuoso Schematic Editor helps you implement each stage of your design.

**VIRTUOSO CUSTOM DESIGN PLATFORM**

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. Virtuoso includes the industry's only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence® CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

*Figure 1: Virtuoso custom design platform*
VIRTUOSO SCHEMATIC EDITOR

Virtuoso Schematic Editor is the design composition environment for the Virtuoso custom design platform, delivering an extensive set of tools for custom IC design entry. From architectural definition using industry-standard language representations, such as Verilog®, VHDL, and C, to final structural implementations at the transistor level, Virtuoso Schematic Editor helps you implement each stage in your design.

BENEFITS

• Easy visualization of large, complex designs using the hierarchy editor
• Early detection of design problems with built-in design and language rule checking
• Rapid command execution with user-configurable bindkeys and menus
• 3x design entry speed via automatic wire routing
• 2x speed in schematic visualization, access, and control

FEATURES

FAST AND ACCURATE DESIGN ENTRY

Virtuoso Schematic Editor has many features that facilitate easy and fast design entry. These capabilities start with well defined component libraries that allow fast design at both the gate and transistor level. This is followed by sophisticated wire routing capabilities to assist in connecting devices. For larger and more complex designs, the tool supports both multisheet designs and the ability to design hierarchically, with no limit to the number of levels used. Hierarchical designs are easy to traverse using the hierarchy editor, and Virtuoso Schematic Editor ensures that all connections are maintained accurately throughout the design. For the more advanced user, commands can be quickly executed using programmable bindkeys and object-sensitive pop-up menus that display relevant operations for objects under the cursor, anticipate user requirements, and present only pertinent choices.

DESIGN WITH INDUSTRY-STANDARD LANGUAGES

Virtuoso Schematic Editor is well suited for entering mixed-level designs. It uses descriptions based on the industry’s two leading hardware description languages — VHDL and Verilog HDL — to facilitate the meet-in-the-middle design approach of the Virtuoso custom design platform. It also supports the ability to use the new mixed-signal languages — Verilog-AMS and VHDL-AMS — to provide a standard for entering designs, regardless of design type. In addition to entering the languages, the user has the ability to generate block representations from the HDL descriptions automatically, facilitating a system-level approach to IC design. This feature uses the text editor to define the pins and basic syntax to begin defining a block. It then uses error-checking features upon completion to check the syntax that you have entered.

EXTENSIVE DESIGN CHECKING CAPABILITIES

User-configurable rule checks identify drawing and electrical rule violations, such as overlapping components, open or shorted connections, unconnected inputs and outputs, object consistency, and illegal names to insure the accuracy of your design. The features of this tool allow the designer to check connections throughout the entire design hierarchy to make sure pin names are matched throughout and wire connections are completed. It can also check and make sure wire labeling has been done properly and there are no unmatched connections anywhere in the design. The user has the flexibility of checking individual pages of the design or checking the entire design hierarchy with one command.

TIGHT INTEGRATION INTO THE VIRTUOSO CUSTOM DESIGN PLATFORM

Virtuoso Schematic Editor is an integral part of the Virtuoso custom design platform. It is connected to all the other features of the platform thus a single environment to create, analyze, and implement multi-domain designs, including ASICs, programmable ICs, multichip modules, and digital, analog, and mixed-signal ICs. Virtuoso Schematic Editor supports both Cadence CDBA and the industry-standard OpenAccess databases. It also supports the Cadence SKILL programming language which facilitates customization of the environment and the encapsulation of proprietary design tools.
SPECIFICATIONS

DESIGN COMPOSITION

• Complete design hierarchy support
• Simplified automatic generation of an HDL template
• Support of multisheet schematics
• User-configurable command bindkeys and label display
• Dynamic highlighting for easy design correction
• Automated interactive connection router
• User-configurable selection with filtering
• Comprehensive symbol creation and editing features
• User configurable undo/redo levels
• Move, copy, stretch, rotate, and delete editing options
• Search and replace features
• Customizable tool environment using Cadence SKILL
• Online help using HTML formatted publications
• Support for bus syntax and bus tapping (see Figure 2)

DESIGN CHECKING

• Schematic or symbol cellviews checked individually
• Entire design hierarchy with one command
• Connectivity and consistency across pages and hierarchy
• Schematic rules checker (SRC) makes both logical and physical checks

DESIGN INPUTS

• EDIF 2 0 0 netlist
• Circuit design language (CDL)
• SPICE
• VHDL IEEE 1076-1993
• Verilog IEEE1364
• OpenAccess data objects

DESIGN OUTPUTS

• EDIF 2 0 0 netlist
• CDL
• SPICE
• Cadence CDBA database
• OpenAccess database

PLATFORM/OS

• Sun/Solaris
• HP-UX
• IBM AIX
• Linux

THIRD-PARTY SUPPORT

• All Process Design Kits supporting Virtuoso custom design platform contain the data needed by Virtuoso Schematic Editor. Please see the PDK datasheet for an explanation of available PDKs.

CADENCE SERVICES AND SUPPORT

• Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  – Collaborative approach and design infrastructure—virtual teaming
  – Proven methodology and flow tuned to your design environment
  – Design and EDA implementation expertise
• Product and flow training to fit your needs and preferred learning style
  – Over 80 instructor-led courses—certified instructors, real world experience
  – More than 25 Internet Learning Series (ILS) online courses
• Cadence customer support that keeps your design team productive
  – Cadence applications engineers provide technical assistance
  – SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

FOR MORE INFORMATION

Email us at info@cadence.com, or log on to www.cadence.com

Figure 2: Automated support of multibit bundles and wire tapping