SuperSpeed USB Certification: Know Before You Go…

With Intel’s release of USB 3.0 in the Ivy Bridge platform in 2012, the long awaited adoption of SuperSpeed technology has entered the mainstream. Microsoft’s release of Windows 8 added native support for USB 3.0 host controllers removing one of the last obstacles to seamless 5Gbps connectivity. In 2013, there has been a steady ramp of SuperSpeed products reaching the market as the USB-IF has recently announced that over 850 products have now passed the SuperSpeed USB certification program. The USB-IF’s compliance program has become a critical development milestone as it provides designers additional confidence that their products will interoperate with other compliant USB systems.

The USB-IF offers a comprehensive compliance certification program which is available to members at regular compliance workshops. In this technical article, we explore important advanced preparations necessary to achieve USB compliance and “time to market”.

USB 3.0 Technical Overview

USB aims to deliver a seamless connection between a host computer and peripheral devices. Navigating the path from idea to market delivery of new USB products often requires both special design skills and test equipment to validate multiple layers of USB technology.

USB 3.0 SuperSpeed is built upon a layered communication architecture. Key components of this architecture include the physical, link, and protocol layers. (Figure 1)

Unlike other serial interconnects that simply use faster bus speeds to increase performance, USB 3.0 creates a dual bus architecture, using a separate set of signals that support the 5 Gbps SuperSpeed signaling while maintaining the legacy 480 Mbps USB 2.0 interface for backward compatibility with older USB peripherals.

The SuperSpeed **Physical Layer** defines the physical connection of the bus between a host and a device. It consists of two differential pairs, one on the transmit side and the other on the receive side. USB 3.0 shares similar characteristics found in existing high-speed serial technologies such as PCI Express and SATA such as 8b/10b encoding, data scrambling, polarity inversion, and spread-spectrum clocking.

The **Link Layer** is defined to establish and maintain a reliable connection between a host and a device. SuperSpeed USB 3.0 introduces some key concepts including: link commands (used to ensure successful packet transfer); link flow control; and power management. The timers, state changes and handshaking are defined with the Link Training and Status State Machine (LTSSM). This diagram
identifies all the logical link states a device may enter when attached to a compliant USB 3.0 host system (see Figure 2).

Finally, the USB 3.0 **Protocol Layer** remains similar to its predecessor. Error detection mechanisms are included, including CRC fields added to all packets. USB 3.0 also adds power saving features at the link layer. SuperSpeed hosts no longer need to poll an endpoint before initiating a power-state transition. USB 3.0 allows endpoints to asynchronously notify the host when it has completed its tasks and is ready to enter lower power states.

**Preparing for Certification**

USB developers should actively consider pre-compliance testing using the same instruments found at USB-IF workshops and independent test labs. Selecting the same instruments can reduce unexpected problems that may arise due to differences in configuration, signal integrity or operator error. Investing in test instrumentation might initially be cost-prohibitive for screening a single OEM USB product. However, the same USB-specific test equipment can deliver significant value through faster “time to market” and fewer problems during USB-IF sponsored workshops.

It is quite conceivable for OEMs to achieve USB logo certification through USB-IF sponsored USB-IF workshops or using one of many independent labs. Both methods fall short in meeting the rapid “time to market” needs of USB OEMs. USB-IF workshops happen too infrequently for most OEM product development cycles. Using independent test labs as the primary method of achieving USB certification is often iterative in nature and thus can be quite costly. OEMs are strongly urged to perform extensive pre-screening of their devices prior to entering into one of the public USB compliance test programs.

The introduction of SuperSpeed USB has resulted in additional testing requirements imposed by USB-IF including new 5Gbps receiver testing as well as a rigorous new link layer test requirement. Test instrumentation manufacturers such Agilent, Teledyne LeCroy, Tektronix, etc. offer a large selection of compliance solutions specialized for the USB certification process. Of these vendors, Teledyne LeCroy is the only single company solution with complete coverage of both Electrical and Link Layer test requirements.
USB 3.0 Compliance Testing

The USB-IF has significantly expanded the requirements for USB 3.0 certification. USB 3.0 adds SuperSpeed USB while maintaining full backward compatibility with USB 2.0 through dual-bus architecture. All devices are required to meet previous USB 2.0 certification tests plus new tests introduced by SuperSpeed USB specification, expanding the overall certification process. Some of these new requirements include: Receiver Testing; Link Layer Testing; and a new Hub certification requirement covering Hub Silicon and End Hub devices.

Electrical Layer Testing

The USB 3.0 SuperSpeed Electrical Compliance Test Specification requires devices to be tested against five physical layer tests in addition to USB 2.0 compliance. These tests include:

- TD.1.1 Low Frequency Periodic Signaling (LFPS) TX test
- TD.1.2 Low Frequency Periodic Signaling (LFPS) RX test
- TD.1.3 Transmitted Eye Test
- TD.1.4 Transmitted SSC Profile Test
- TD.1.5 Receiver Jitter Tolerance Test

LFPS testing is performed on both the transmitter and receiver. The transmitter LFPS is intended to ensure that LFPS frequency and timing meet the requirements of USB 3.0 specification while the receiver can correctly recognize LFPS signaling against voltage swing and duty cycle variations.

Transmitter Testing

The transmitter compliance test is intended to determine whether the transmitter eye width, Random, Deterministic Jitter and Total Jitter meets those specified by the USB 3.0 Specification. The transmitter is also checked against the spread spectrum clocking (SSC) profile detailed in the specification.

USB-IF requires the transmitter be tested for the transmitted eye, LFPS timing and the transmitted SSC profile. For example, TD.1.3 verifies that the transmitter meets the eye width, deterministic jitter and random jitter requirements. A protocol aware bit-error-rate tester is used to place the DUT in compliance mode where it is required to send a
specific test pattern called CP0 pattern (scrambled logical idle). Here an oscilloscope can now be used to measure the eye width through the reference CTLE in order to provide an open data eye.

**Receiver Testing**

The Receiver jitter tolerance testing focuses on measuring the Receiver’s ability to properly receive and interpret the incoming data across multiple frequencies. This test also relies on a pattern generator that places the DUT in loopback mode and transmits compliance patterns with added jitter. The DUT loops the received data pattern back to the generator and any differences are counted as an error.

The Host and Device transmit data with embedded SKP symbols and by injecting and removing additional SKP symbols, each side can control and match the other side's clock speed. This challenges receiver testing because the addition and removal of SKP symbols in the data stream means that data sent out of the generator is always different from data received for bit-error-rate comparison. Thus the requirement for protocol awareness to filter the SKP symbols prior to comparing the received pattern is critical. The Teledyne LeCroy PeRT3 (Protocol Enabled Receiver Tester) is designed specifically to handle this requirement.

These tests significantly increase the complexity associated with USB 3.0 electrical layer compliance. It is highly recommended that developers verify their designs against these requirements before attempting physical layer compliance testing at the USB-IF workshops or independent compliance labs.

**Link Layer Testing**

The link layer’s critical role in establishing and maintaining the integrity of the connection between host and device has led to a comprehensive test requirement for the SuperSpeed link layer. Over 130 separate link layer assertions are tested across 40 unique test cases. The Teledyne LeCroy Voyager M3 platform is one of the approved Link Verification Systems (LVS). The Voyager M3 is the only solution that is based on an integrated analyzer / exerciser where all tests are script-based and users can view and modify all source code for debug or to create their own custom tests. Below are two example Link Layer tests.

**Link Layer Compliance TD7.5 - Header Packet Framing Robustness**, is intended to verify that the device under test (DUT) will not reject a packet having a single symbol error in the HPSTART framing. During this test a traffic generator/exerciser acting as the host or device is connected to DUT. Link initialization sequence is performed and the traffic generator transmits the required Link Management packet with errors in the first symbol of the HPSTART sequence. The test passes if the link initialization completes successfully. The link is reset and the test repeated with errors inserted in the second, third and fourth symbols of the HPSTART sequence respectively. To pass, the DUT should acknowledge the packet and stay in U0 for at least 50ms.

Similarly, **TD.7.7- RX Header Packet Retransmission Test**, validates that the device under test will reject packets where a single invalid character is received in the payload portion of the header packet. In this situation the specification requires that the DUT reject the packet by responding with the LBAD link command. The DUT should stay in U0 while the traffic generator then resends a valid LMP which should be acknowledged by the DUT. This test was expanded with 16 different iterations after it was discovered that some DUTs behaved differently based on the actual symbol that was inserted in the header. The image below shows a common fail condition
where the DUT enters recovery after an End of Packet (EPF) symbol appears in the middle of the header payload.

Summary
USB has a well-earned reputation as the world’s easiest to use and most reliable communications interconnect. The USB-IF’s compliance program has been the cornerstone of that user experience. Designed to ensure seamless device interoperability, participation in the SuperSpeed logo certification program is an essential part of delivering successful USB technology to the market.

The USB 3.0 certification program represents a substantial test effort from an OEM design perspective. The examples highlighted above reflect only some of the complexities that OEMs face when starting USB 3.0 certification. “Know before you go” highlights the importance of thoroughly pre-screening for USB compliance well ahead of a USB-IF workshops. As the next wave of USB industry adoption gets underway, well designed and tested products will be the key to success in SuperSpeed USB.

Author:
Mike Micheletti is a Product Manager with Teledyne LeCroy’s Protocol Solutions Group. For the last 10 years Mike has helped define and drive LeCroy’s digital layer test platforms for key emerging communications standards, including USB, Serial ATA, SAS, Fibre Channel, and DDR. Mike is a regular participant at the USB and DDR consortium meetings as well as compliance and certification working groups. © 2013, Extension Media