

HES-7 a ASIC and SoC Prototyping Board with backplane connector on top for daughter cards

FPGA-Board for Rapid ASIC and SoC Prototyping

The FPGA board HES-7™ provides a scalable FPGA-based ASIC prototyping solution for SOC/ASIC hardware verification and software validation teams. For complex ICs the production cost are extremely high, so there is a need to make these semiconductors right the first time. The common methodology is, to load the hardware description language in a FPGA prototyping board and verify it. The FPGA emulation does not run in real time, but it allows operating and testing the Chip before the expensive semiconductor production process starts.

HES-7 board is equipped with two Xilinx® Virtex®-7 2000T, has 4 million FPGA logic cells of capacity plus DSP and memory resources. The board is made of the core for verifying the ASIC code and the peripherals to connect and expand the board.

To communicate between the two onboard FPGAs there are 322 high-speed inter FPGA connections with matched length design rules and low tolerance impedance in the core of the board.

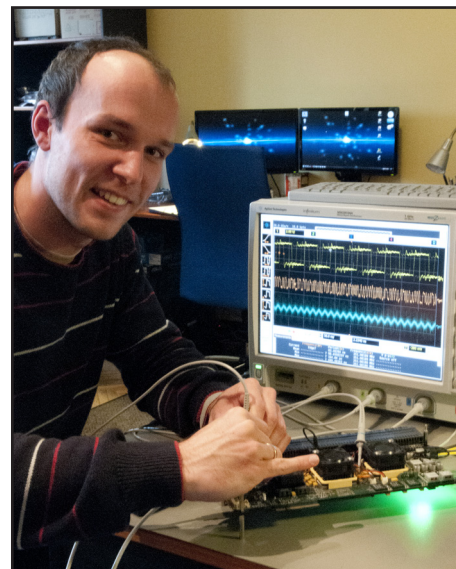
FPGA verification requires different types of memory to store code or data during the test. The board can be equipped with 16 GB

of DDR3 RAM supported with SO-DIMM sockets and additional 8GB of Flash memory. For data storage in a standalone configuration is a Micro SD Card socket implemented.

Using a backplane connector, HES-7 can include the expansion of daughter boards. This is made through a high-speed connector which allows having 60 differential global and local clock inputs from backplane to core of PCB. The total memory can also be expanded by connecting up to four HES-7 boards to each other with a resulting total memory of 64GB of DDR3 RAM. The expansion is made through 25 gigabit/s high-speed connectors.

The challenge is to be flexible for all kinds of possible ASIC code, which will be tested. So universal clocking is implemented with 5 customized, low skew, global clocks from the backplane. For clock setting user programmable PLLs (from 2 kHz to 1.4 GHz) are installed onboard. MMCX connectors enable external clock inputs (from 0 to 450 MHz).

Internal and external communication has to offer several standard interface protocols. For operating inside a personal computer a PCI-express finger connector allows the easy installation.



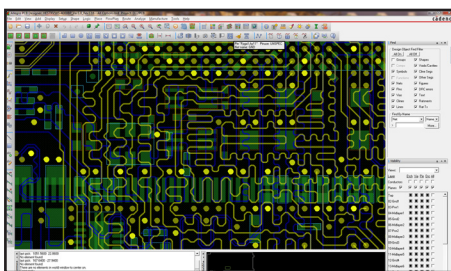
Michał Elias, Senior PCB Designer at Aldec

Design Challenges

"A design such as HES-7 requires a flawless constraint management system with fast on-line design rule checking. This was the main reason why we changed our PCB tool to the Allegro tool suite", said Zibi Zalewski, Hardware Division General Manager at Aldec, Inc.

"Another reason for the change were the features in interactive routing. With so many serial high-speed interfaces the delay tuning takes a vast amount of time to get all matched length for the netgroups right on more than 16 layers. The possibility to use Auto interactive Delay Tuning (AiDT) function enables us to prepare a rough routing by hand and use PCB Editor to perform a predictable delay tuning exactly where we want it to be."

This impedance controlled design with over 3000 components uses two FPGAs where the pin assignment needs to be optimized between the two major FPGAs but as well with the expansion connector and the PCI-Express PC-slot connector. A clean pin assignment of all the signals is the key to reduce the number of signal and reference layers to a minimum and allow to operate the interfaces between the two major Xilinx Virtex-7 2000T with a speed grade of 500 to 600 MHz.



HES-7 Design in Allegro PCB Editor

Fewer layers will offer more reliability and also lower production costs. Although the produced quantities are not huge, it still is one of the soft requirements to be achieved for every design.

Today's serial and memory interfaces like PCI-express and DDR3 have tight timing budgets on all lines so they require not only that all electrical design rules are matched but also the timing margins are balanced throughout the complete interface.

An efficient PCB Layout tool like Allegro PCB Editor environment enables the designer to complete all the challenges in a short time. Allegro PCB Editor also offers the interaction between tool and designer, so the design intent is implemented by using the right mix of automation by the tool and manual interaction based on specification and experience.

If HES-7 is operated outside a PC it can be connected through a PCI-express cable. So the constraints on the board have to consider the expansion cables as well if it is connected and the right termination if it is not connected.

Additionally there are 89 special purpose global lines to all FPGAs which can be used for programming, expanded debugging or customer specific signals. These general purpose tracks have to be all the same length and impedance, since it is not clear at the design phase, what signal speed will travel across which signal and how many of these signals will be grouped to an interface.

To give the user more flexibility with testing his ASIC and embedded software there are USB interfaces available for the virtual ASIC.

Both transmission speeds are implemented: USB 2.0 and USB 3.0 via external connectors.

For the initial bring up of the HES-7 and test in production a boundary scan chain was installed and is accessible as JTAG connector.

Two SATA connectors for connecting a Hard Disk memory can be used as device and host.

Tools used to design

Aldec uses Allegro PCB Editor for High-Speed signals, differential pairs and interactive PCB layout. The Constraint Manager contains all design rules of the board. Allegro FPGA System Planner straightens out pin assignment between the FPGAs and the connectors.

About Aldec

Aldec Inc., headquartered in Henderson, Nevada, is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, Design Rule Checking, IP Cores, DO-254 Functional Verification and Military/Aerospace solutions. Aldec's Hardware Design Center is located in Gdansk, Poland.
www.aldec.com

More information at:

FlowCAD

FlowCAD (Germany)
Mozartstrasse 2
D-85622 Feldkirchen bei München
+49 (89) 4563-7770
info@FlowCAD.de