

FloWare Modules – Enhancing Productivity

Version v64

FlowCAD Confidential 1



FloWare Features

- General purpose utilities
 - Functions not in standard tool yet
 - Not written for one specific customer
 - Everybody should benefit
- Easy installation
 - Also casual users must be able to install FloWare
 - No variables
 - Menus will be created automatically
 - Integrates perfectly into existing customizations
- Documentation
 - Full documentation is provided for every module



Table of Contents

• Categories

- PCB Layout

- OrCAD PCB Designer
- Allegro PCB Editor
- <u>Schematic Entry</u>
 - OrCAD Capture
 - Allegro Design Entry CIS
- <u>Contact Information</u>



FloWare Modules PCB Layout

OrCAD PCB Designer / Allegro PCB Editor



FloWare Modules PCB Editor

- Advanced Mirror
- <u>Advanced Testpoint Check</u>
- <u>Anti Tamper Mesh PCB</u>
- AOI Check
- <u>Assign Net to Via</u>
- Barcode Generator
- Batchplot
- <u>CAF-DRC</u>
- <u>Change Width</u>
- <u>Class Color</u>
- <u>Cleanliness Check</u>
- <u>Coil Designer</u>
- <u>Contour Place</u>
- <u>Cross Copy</u>
- <u>Cross Section Generator</u>
- <u>Custom Variables</u>
- Design Compare
- Digital Soldermask
- Drafting Utilities

- Drawing Designer (legacy)
- Drawing Size
- Drawing View Manager
- Edge Plating
- FPGA Utilities
- Highlight Dummy Pins
- IBIS Prototype Modeler
- Label Generator
- Label Tune
- Mask Generator
- <u>NC Panel Route</u>
- <u>Net Color View</u>
- Padstack Finder
- Padstack Usage
- Panelization
- PCB Library Plot
- Polar Grid Utilities
- Post Processing

- Push to Grid
- Quick Symbol Edit
- <u>Replace Via</u>
- Shape Utilities
- Shield Generator
- Shield Routing
- <u>Silkscreen</u>
- Snap Generator
- SVG Export
- <u>Synchronize Testprep</u>

Videos available on

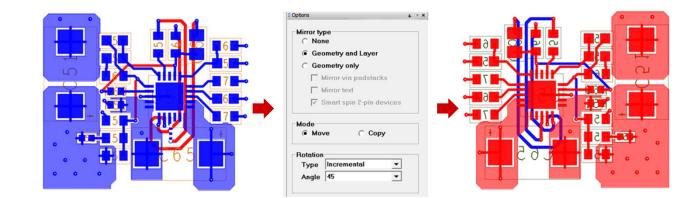
- Variant 3D
- Variant Assembly
- Variant BOM
- <u>Z-DRC</u>

YouTube



Advanced Mirror

- Enables mirror operations while moving or copying elements
 - Mirror across subclasses (Geometry and Layer)
 - Mirror on the same subclass (Geometry only)
- Including placement and routing
- Selection through window or single pick, dynamic preview
- Special handling for symbols, vias and text in Geometry only mode



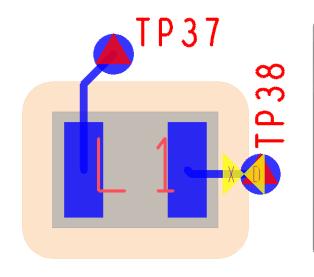


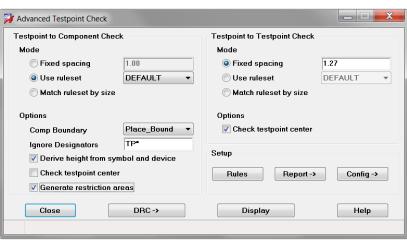
Advanced Testpoint Check

- Addresses various rules for testpoint checking
 - Testpoint to Testpoint check
 - Testpoint to Component check taking component height into account
 - Visualization of restriction areas
 - DRC marker generation

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- Constraints reuse through configuration files





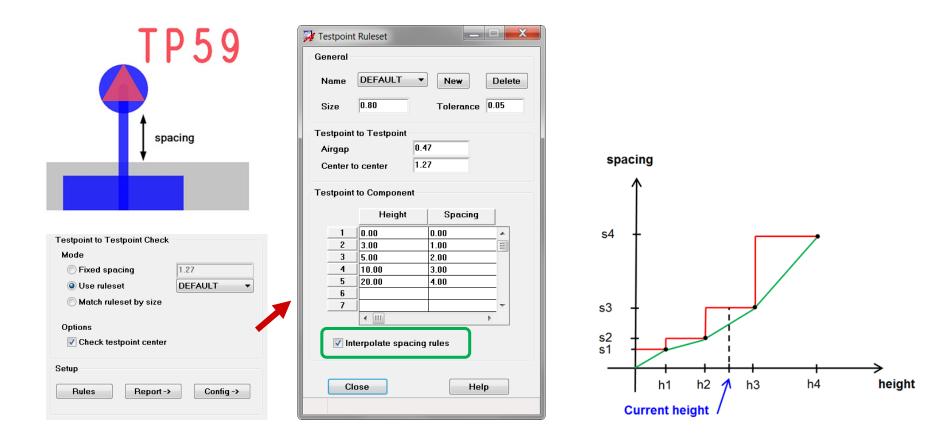


Advanced Testpoint Check

- Spacing rules may be specified
 - As fixed spacings

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- Using rulesets, which account for component height





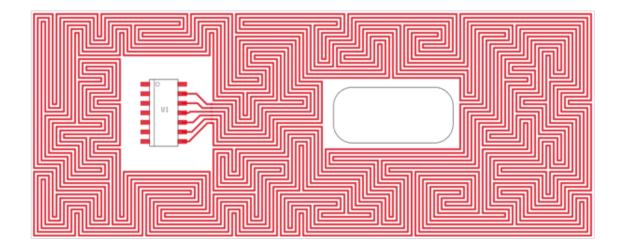
Anti Tamper Mesh PCB

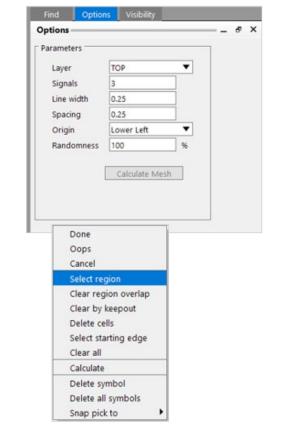
• Useful for Hardware Security Modules (HSM)

 In order to actively detect and respond to external attacks a convoluted maze of wires (mesh) can be used to monitor changes in resistance, capacitance, breaks, shorts etc.

• Features

- Number of signals, width, spacing, ...
- Region select, keepouts, destination layer, ...
- Randomness





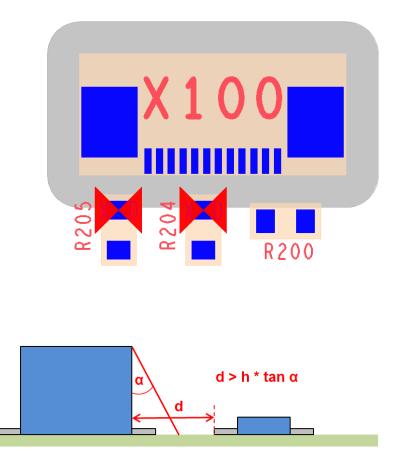


AOI Check

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- Helps users to check AOI related rules directly in PCB Editor
- Shadowing can cause serious issues in verification process

Parameters		Diagram
Camera angle	19.00	
Direction	All 👻	
Additional distance	0.00	1
		h 🚽 h
Seneral		Shadows
Comp boundary Pla	ice_Bound 🔻	Extend shadow by component pad
Derive height from symb	ol and device	🔽 Generate shadow areas
Calculate effective pad	area	✓ Attach shapes to symbol



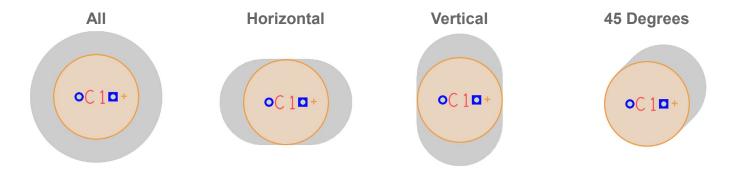
h



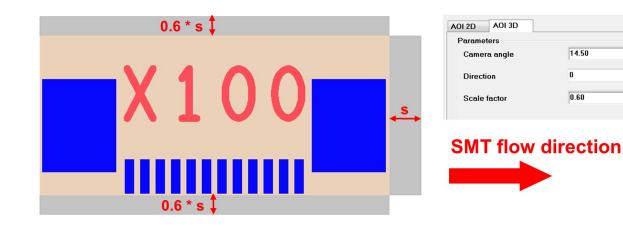
AOI Check

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 Shadows can be calculated in various directions based on specified camera angles taking component height into account



• Special rules apply to 3D inspection systems

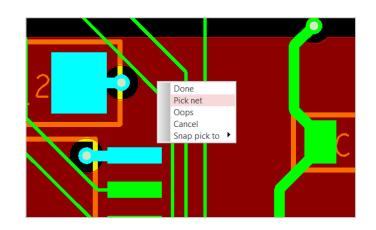


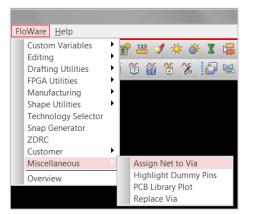


Assign Net to Via

- Enables users to change the net on existing vias
- No need to delete and route new ones
- Use model

- Select net from list (including wildcard support) or by context RMB > Pick Net
- Click on one or more vias
- Choose RMB > Done to confirm



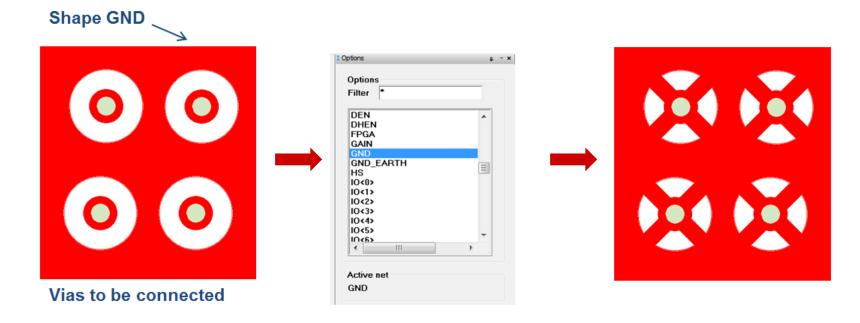






Assign Net to Via

Example





Barcode Generator

- Prints barcodes on a PCB layer as part of the manufacturing process
- Supporting definitions
 Code 39, Code 128, QR Code and Data Matrix
- Adjustable parameters corresponding to selected code
- Additional drawing options (e.g. show text, inverted display)
- Dynamic preview during parameter change
- Parameter preset through configuration file



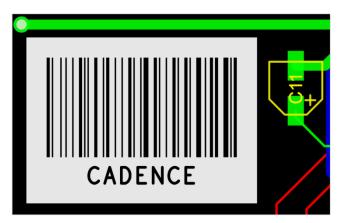


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		Setu Disp Edit Draf Shap Chec	lay t	> > > >	-	#			\$					P	123
		Man Sign Custo Misc	umentatic ufacture al Integrit om ellaneous view	► y ►		Barco Cross Custo Displ Draw Pads PCB SVG Varia	s Sector om V lay La ving I tack I Libra Expo	ariab abel 1 Desig Usage ry Plo rt	Text iner e ot	•	2	Cod QR (Data	Code	e	

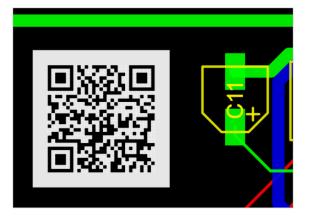




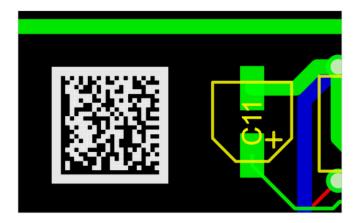
Barcode Generator



对 Barcode Gene	erator Code39/128 📃 🖂
General	
Text	CADENCE
Class	BOARD GEOMETRY
Subclass	ASSEMBLY_NOTES V
Cabbildos	
Specification	
Code 39	Code 128
Barcode Size	
Barcode hei	abt 10.000
Barcode wid	
Min bar widt	h 0.170 O Fix value
Margin Top/	Bot 2.000
Margin Left/	
	3
Misc	
🔽 Embed tex	t into barcode using block 4
📝 invert struc	ture
ОК	Place Help
UK	гасе пер



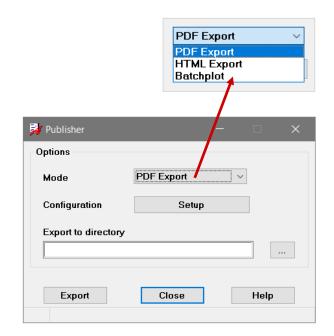
🕻 Barcode Generator QR-Code 📃 🖂
General
Enter text manually
http://www.cadence.com
Read from file
Class/Subclass
BOARD GEOMETRY
Encoding Version 3→ (29×29) ▼ Ecc level M ▼
Drawing Unit size 0.30 VInvert structure Merge shapes
Info Capacity: Numeric: 101 Alphanumeric: 61 Bytes: 42
Text status: Chars: 22 Type: byte
OK Status Place Help



General				
Enter text	manually			
http://ww	w.cadence.com	/welcome	e.html	
Read from	n file			
Class/Subcl	ass			
BOARD GE	OMETRY	- / AS	SEMBLY_NC	TES
Options				
Size	AUTO	-	Process	tilde
F	AUTO	_		
Encoding	AUTO			
Drawing				
Unit size	0.30		V Invert str	ucture
Margin	0.60		Merge sh	apes



- Creates documentation
 - Fully automated
 - Multipage or single page files
 - Visibility control based on views (color views as well as artwork views), similar to visibility panel
 - Order of view items can be changed by user
 - Plotsets allow grouping views into separate PDF files
 - Load and save configuration to disk
 - Three modes
 - PDF Export from Allegro / OrCAD PCB Editor
 - HTML Export
 - Batchplot (legacy)

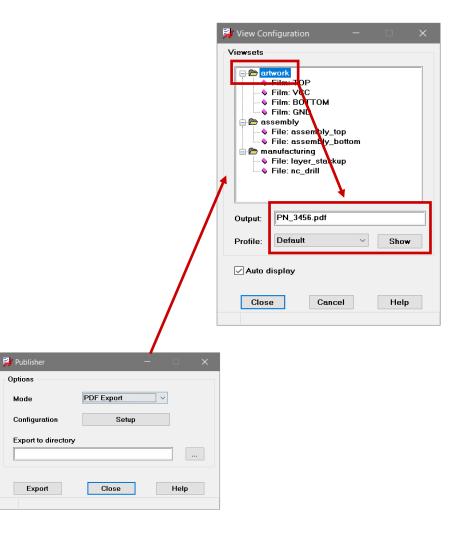




- Multiples viewsets can be defined
- A viewset may contain
 - Film records

- ...

- Color views (!!)
- Each viewset corresponds to one PDF file to be generated – Name of the PDF file can be specified (output)
- Each viewset may reference a profile to be used during PDF export
 - E.g. black white print only
 - With / without meta data
- Single push button to generate all data ...



Options

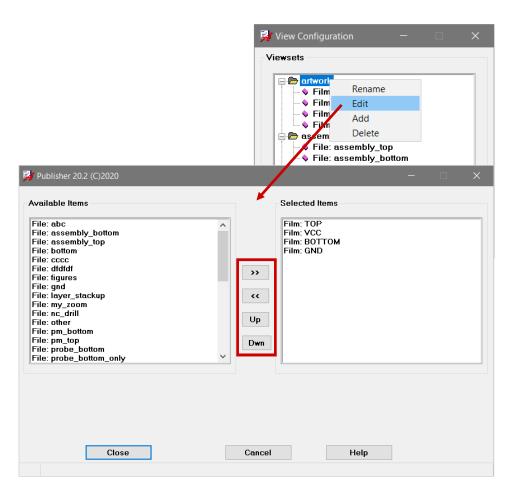
Mode



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Setup Viewsets for PDF Export

- Use context menu in tree view
 - Rename
 - Edit
 - $-\operatorname{\mathsf{Add}}$
 - Delete
- Edit views
 - Select film views
 - Select color views
 - Change order

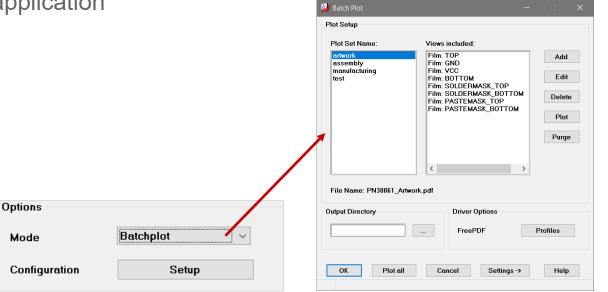


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Other Modes

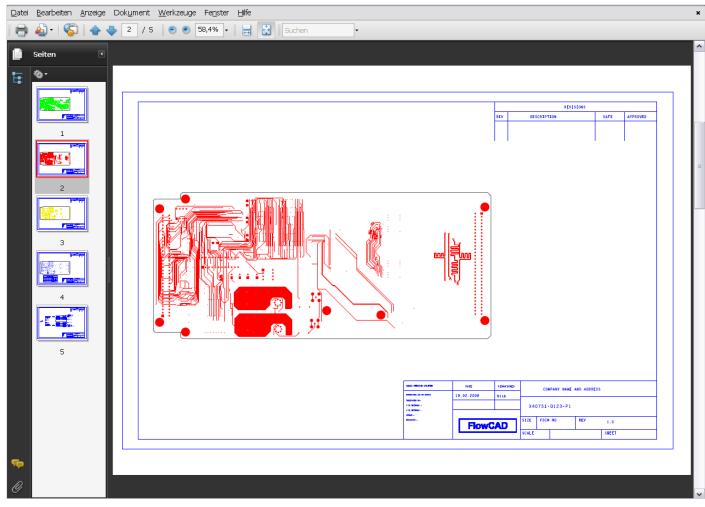
- HTML Export
 - Generates an HTML report including SVG graphics
 - Setup regarding viewsets and profiles similar to PDF Export
- Batchplot (legacy)
 - Selecting Setup will launch the existing / legacy application
 - Still available and supported

科 Publisher				×
Options				
Mode	PDF Export	×		
Configuration	PDF Export HTML Export Batchplot			
Export to director	у			_
Export	Close		Help	





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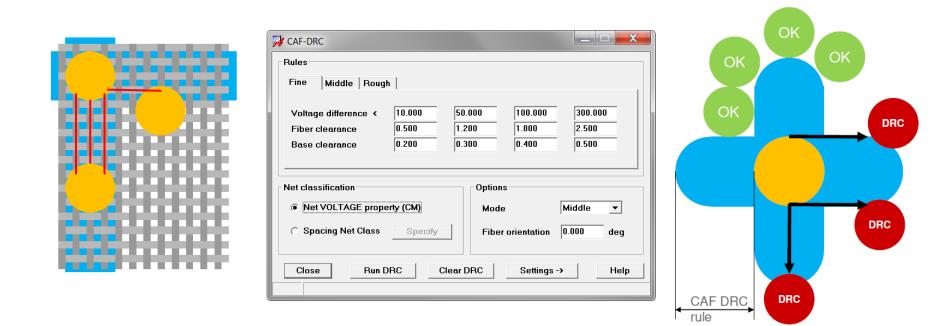


Final document opened with Acrobat Reader



CAF-DRC

- Special DRC for Conductive Anodic Filaments (CAF) on PCBs
- Performs Hole-to-Hole clearance checks along the fiber structure
- Based on voltage classification
- Adjustable fiber orientation





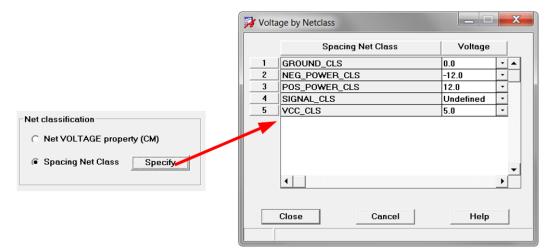
CAF-DRC

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• Use model

- Classify nets by voltage property or by spacing net class
- Launch application
- Specify rules and select mode to be used
- Export / import rules for reuse purposes
- Run DRC

👩 Allegro Constraint Manager	(connected to	Allegro PC	B Designer (was Performance L) 16.	6) [cafdrc_by_net_voltage] -
File Edit Objects Colum	nn <u>V</u> iew A <u>n</u> aly	ze <u>A</u> udit	<u>T</u> ools <u>W</u> indow <u>H</u> elp	cā
	ADD	RESS	💽 🕼 📜 ଓ 🗋 ଡ	🏝 🍕 🚓 🖦 🐀
* Worksheet selector	τ - ×	cafdr	c_by_net_voltage	
4 Electrical				
+ Physical			Objects	Voltage
Spacing		Туре	S Name	v
Same Net Spacin	g	*	*	*
Properties		Dsn	cafdrc_by_net_voltage	
E D Net		Net	P12V	12 V
T		Net	VCC	5 V
General Properties		Net	AGND	0 V
Ratsnest Bundle Pro	perties	Net	N12V	-12 V
🖻 🧁 Component		Net	UNNAMED_1_2N4339_66P_	s
E Component Proper	ties	Net	UNNAMED_1_2N4339_66P_	D
Pin Properties		Net	UNNAMED_1_2N2222_6P_E	
		Net	UNNAMED_1_2N2222_6P_0	:
		Net	UNNAMED_1_2N2222_6P_E	3
		Net	UNNAMED_1_1N4148_11P_	CAT
		Net	UNNAMED_1_1N4148_11P_	AN
		Net	UNNAMED 1 1N4148 9P 0	CAT



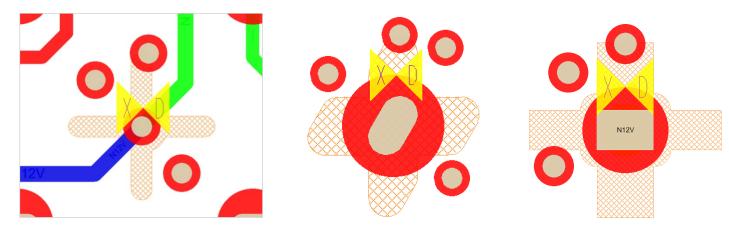


CAF-DRC

Results

- DRC markers in PCB Editor and Constraint Manager including cross probing
- Visualization of DRC polygons on DRAWING FORMAT subclasses CAFDRC_DV1, _DV2, DV3 and _DV4
- Handles all drill and slot types

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Norksheet selector 🛛 🖡 👻 🗙	cafdrc					
Flectrical	caluic	1				
Physical	Objects	Constraint Set	DRC Subclass	Values		
		Constraint Set	DRC Subclass	Required	Actual	
🦿 Spacing Same Net Spacing	Name	*	*	*	*	
Properties	cafdrc					
I DRC	Cafdrc					
BRC	(122.3205 87.5860)	Caf-drc	All	1.200000	FAIL	
	(124.3145 87.5742)	Caf-drc	All	1.200000	FAIL	
- Electrical	(130.6272 88.6275)	Caf-drc Caf-drc	All	1.200000	FAIL	
- Physical	(135.2550 85.2170)	Caf-drc	All	1.200000	FAIL	
	(135.5703 91.4987)	Caf-drc	All	1.200000	FAIL	
Same Net Spacing	(138.0020 62.3285)	Caf-drc	All	1.200000	FAIL	
Besign	(138.1352 61.6310)	Caf-drc	All	1.200000	FAIL	
	(138.3030 59.9186)	Caf-drc	All	1.200000	FAIL	
External	(156.0576 65.1256)	Caf-drc	All	1.000000	FAIL	
	(156.3692 82.5231)	Caf-drc	All	1.200000	FAIL	
	(156.6926 82.1690)	Caf-drc	All	1.200000	FAIL	
	(158.8545 79.4436)	Caf-drc	All	1.200000	FAIL	

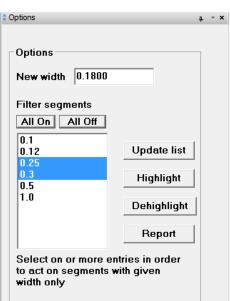




Change Width

- · Change the width of clines and clines segments
- Supporting a filter mechanism in that the changes are only applied to segments matching a given width
- Select by Pick, Window, Temp Group or Find By Name
- Highlight and report functionality including cross probing

-# 🗙 🔒 🗁	? Search:	Match word Match cas	3e
Width	Start	End	Layer
1.0	(144.5 26.8)	(144.5 27.875)	ETCH/TOP
1.0	(139.25 28.25)	(139.25 24.65)	ETCH/TOP
1.0	(137.7 26.8)	(137.7 28.3)	ETCH/TOP
1.0	(140.8 27.975)	(140.8 26.8)	ETCH/TOP
1.0	(137.45 19.2)	(136.152 19.2)	ETCH/TOP
1.0	(137.525 19.275)	(137.45 19.2)	ETCH/TOP
1.0	(130.4 26.9)	(130.4 28.075)	ETCH/TOP
1.0	(134.1 28.05)	(134.1 27.05)	ETCH/TOP
1.0	(135.8485 19.1)	(135.5 19.1)	ETCH/TOP
1.0	(135.8704 19.1146)	(135.8485 19.1)	ETCH/TOP
1.0	(136.007 19.1712)	(135.8704 19.1146)	ETCH/TOP
1.0	(136.152 19.2)	(136.007 19.1712)	ETCH/TOP
1.0	(132.1 19.2)	(133.6 19.2)	ETCH/TOP
1.0	(135.5 19.1)	(135.4 19.2)	ETCH/TOP
1.0	(133.6 19.2)	(133.6 17.9)	ETCH/TOP
1.0	(135.4 19.2)	(135.4 17.4)	ETCH/TOP
1.0	(87.3 27.5)	(88.8 27.5)	ETCH/TOP
1.0	(87.3 28.8)	(87.3 27.5)	ETCH/TOP
1.0	(90.5 19.8)	(90.5 18.625)	ETCH/TOP
1.0	(86.8 18.65)	(86.8 19.65)	ETCH/TOP
1.0	(85.5 27.5)	(83.4 27.5)	ETCH/TOP
1.0	(85.5 29.0)	(85.5 27.5)	ETCH/TOP



Enable On-Line DRC

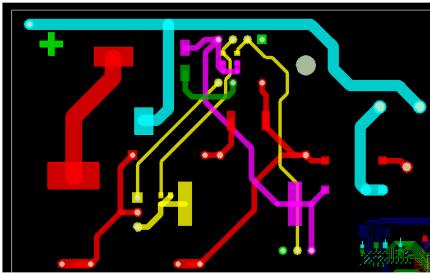


Class Color

- Enables users to color spacing net classes for review and documentation purposes
 - Color chooser
 - Legend support
 - Settings stored in database
 - Export / import settings

Legend Image: Constraint of the second se	ock 5
CLASS	COLOR
HIGH VOLTAGE	
PE	
POWER	
SECONDARY	
SWITCH	

	Spacing Net Class Color	
1	HIGH VOLTAGE	
2	PE	
3	POWER	
4	SECONDARY	 4
5	SWITCH	 -
Lege	ina	
_	end Generate/Update legend Text block 5	

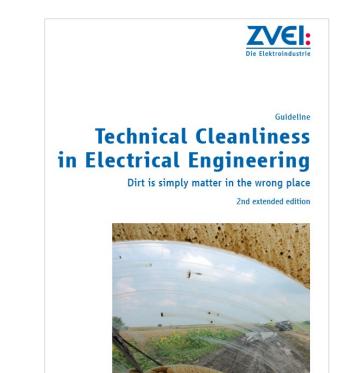


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Technical Cleanliness

- Technical Cleanliness refers to the performance of components, assemblies and systems related to particle contamination in automotive and other applications
- On PCB's such particles (e.g. conductive particle from aluminum cover) may cause short circuits
- The probability failure depends on
 - Particle size
 - Contact area size
 - Number of contact areas
- For more information refer to document ZVEI Guideline for Technical Cleanliness from <u>https://www.zvei.org/</u>

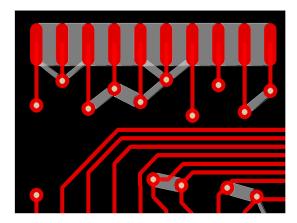




Technical Cleanliness

- Analyzes the PCB layout for contact areas caused by particles with a given size
- The contact area specifies the area in which a particle will cause a short, no matter how the particle is oriented
- Cleanliness Check calculates and visualizes contact areas using shapes and writes a report
- By sweeping the particle size the information from the output can be used to feed cleanliness assessment calculator from ZVEI

Cleanliness Check	- 🗆 X
General	
Particle size	1.0000
Side	Тор 🔻
Min shape aperture	0.0050
☑ Merge contact area shapes	
🗹 Enable data tiling	2.00
☑ Ignore small voids	20
Subtract open copper	
Create DRC	
Misc	
Clear 👻	Report
Close Run	Help 🔻
Range is 0.0000 to 1000.0000	

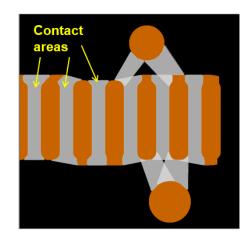




Technical Cleanliness

- Menu button Report
- Particle count per layer
- Short Area

- Sum of particle shape areas from layer CLNS_CONTACT_TOP (BOTTOM)
- Short Area
 - Shape area on merged layer CLNS_RESULT_TOP (BOTTOM)
- Design Area
 - Area from **DESIGN_OUTLINE** minus **CUTOUT**

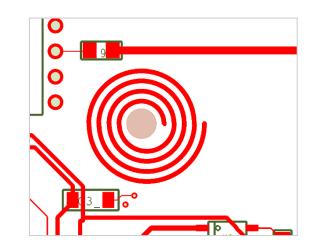


Cleanliness R	eport		
🔎 🗶 🖻	🖬 🖨 🥥 Search:		🔾 💭 🕅 Match word 🕅 Match
	ess Report:		
Desigr	1: board04.brd May 21 13:39:56	2019	
Units:	MM		
Units:	MM ParticleCount	ShortArea (sq mm)	ShortAreaMerge (sq mm)
Units: TOP	ParticleCount	ShortArea (sq mm) 69.748	ShortAreaMerge (sq mm) 68.980
	ParticleCount 295		



- Includes useful functions when designing planar spiral inductors on a PCB
- Support for different spiral pattern
 - $-\operatorname{Round}$
 - Rectangle
 - Octagon
 - Hexagon
- Features
 - Parameterized input in terms of width, spacing, number of turns, etc.
 - Support for rotation, flipping and scaling
 - Dynamic preview during parameter change

Round Recta	ngle Oc	ctagon Hexagon			
Parameters			Diagram		
Width 1.	.000	Spacing 1.000			
Diam X 6.	.000	Rotation 0.00			
Turns 3				Spacing Wieth +	
Scale 1.	.000	Clockwise	Diem X		
Calculated Exte	ents: 18	3.000 × 17.000			
	ents: 18	3.000 × 17.000	Miscellaneous		
General		8.000 × 17.000 TOP •	Miscellaneous Add pad at start	AIV	*
General	bclass [ТОР •		VIA VIA	*
General Create coil on sul Add route kee	bclass [🔲 Add pad at start	VIA	
General Create coil on sul Add route kee Su	bclass pout bclass	ТОР •	Add pad at start	VIA	
General Create coil on sul Add route kee Su	bclass pout bclass	TOP •	Add pad at start Add pad at end Convert structure to	VIA	



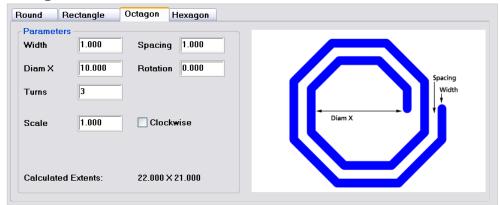
Basic spiral patterns

Round

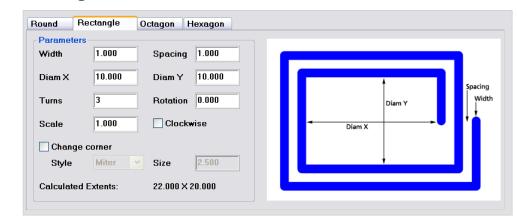
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Parameters	tangle C	spacing 1.000]	
Diam X	6.000	Rotation 0.000		Spacing
Turns	4			Width
Scale	1.000	Clockwise))
Calculated Ex	tents:	22.000 × 21.000		

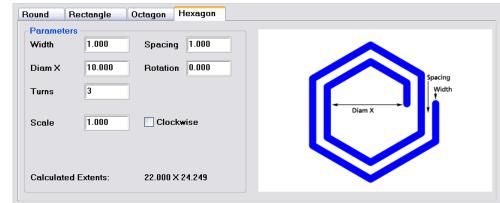
Octagon



Rectangle



Hexagon



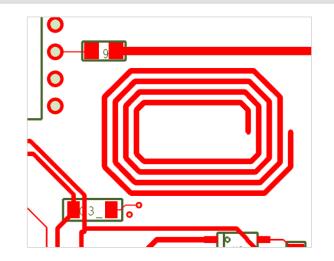


Rectangle spiral with corner modifications

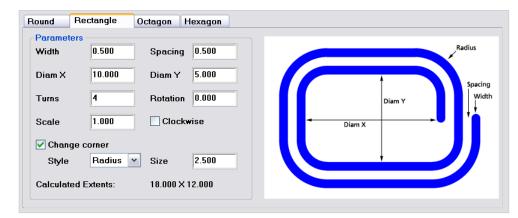
Mitered corners

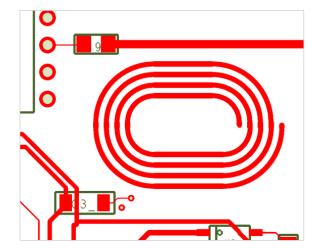
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Round Rectangle Octagon	Hexagon	
Parameters		1
Width 0.500 Spacin	ng 0.500	Miter
Diam X 10.000 Diam Y	Y 5.000	Spacing
Turns 4 Rotati	on 0.000	Diam Y Width
Scale 1.000 Clo	ckwise	Diam X
Change corner		
Style Miter 💌 Size	1.000	
Calculated Extents: 18.000) X 12.000	



Rounded corners







• Other features

- Realization as a combination of cline segments or one single shape
- Addition of padstacks to the start / end points
- Automatic generation of route keepouts in the inner area

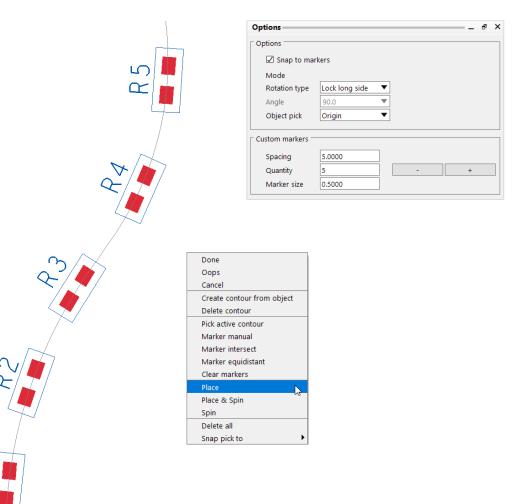




Contour Place

 \bigcirc

- Interactive placement along contour
 - Automatic snap to contour path
 - Place, Place & Spin, Spin
- Various alignment options
 - $\mbox{ Lock long side}$
 - Lock short side
 - Relative
 - Absolute
- Custom snap marker
 - For accurate control
 - Manual markers
 - Markers by intersection
 - Equidistant markers

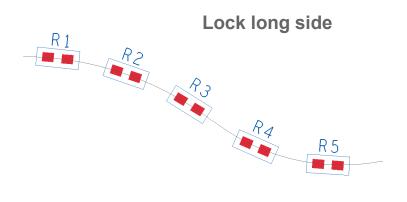


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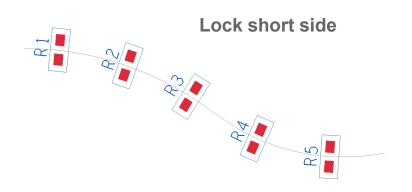


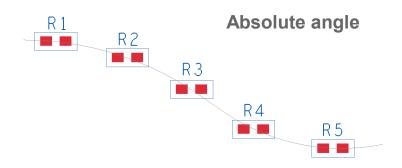
Contour Place

• Alignment options



Options		Ð	×
Options			
Snap to mark	kers		
Mode			
Rotation type	Absolute 🔻		
Angle	Lock long side		
-	Lock short side		
Object pick	Relative 😼		
	Absolute		
Custom markers —			
Spacing	5.0000		
Quantity	5 - +		
Marker size	0.5000		







Cross Copy

• Problem

 $(\)$

- Customer needs to move objects from one class / subclass to another
- Command Edit > Copy does not support a destination layer
- Customer gets error messages, e.g. E Changing shape to a different class is not supported
- Customer has to find workarounds (e.g. export subdrawing, text edit clipboard file, import subdrawing)
- Solution
 - Cross Copy closes the gap
 - Can move or copy objects to any destination layer for various purposes
 - In contrast to Create Detail, objects are not destroyed (e.g. text will stay text!)

General:
Destination class/subclass:
Board Geometry 🔹
Assembly_Notes -
Delete original objects
Processing options
Shapes:
Type Filled Shape 🔹
Voids Include 🔹
Clines/lines:
Convert to shape
Endcap style Round 🔻
Pins/vias:
Mode Pads only ?
Figures (stand-alone):
Mode Filled Shape 🔻
Advanced:
🔲 Merge all
Merge by net
Toggle Layers



Cross Copy

- Advanced features
 - Shape processing
 - Include / exclude voids
 - Fill or decompose with / out voids
 - Unfill shape
 - Clines / lines processing
 - Can be converted to shape
 - Various endcap types
 - Padstack processing (pins and vias)
 - Drawn as shape on destination layer
 - All visible layers are merged
 - Resulting pad shape can be voided by drill hole information
 - Merging support
 - Selected data (find filter settings) is merged







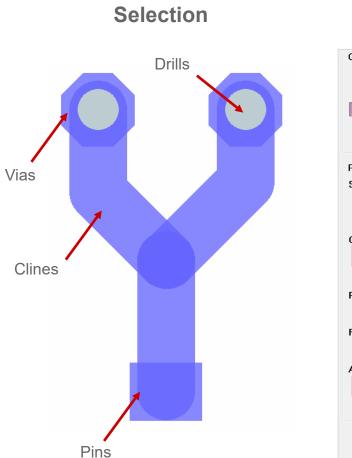




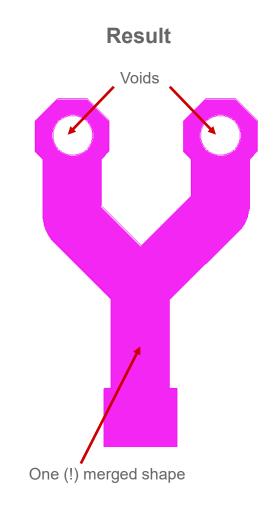
Cross Copy

 \bigcirc

Example: Merging data to soldermask shape



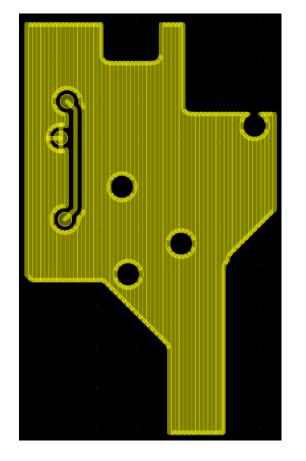




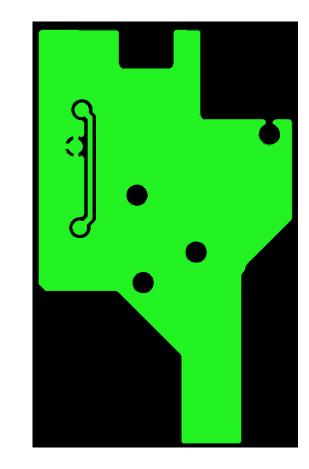


Cross Copy

Example: Converting pseudo shapes (stroked lines) to real shapes



General:								
Destination class/subclass:								
Etch •								
Top								
Delete original objects								
Processing options								
Shapes:								
Type Filled Shape 🔹								
Voids Include 🔹								
Clines/lines:								
Convert to shape								
Endcap style Round -								
Pins/vias:								
Mode Pads only								
Figures (stand-alone):								
Mode Filled Shape 🔹								
Advanced:								
Merge all								
Merge by net								
Toggle Layers								



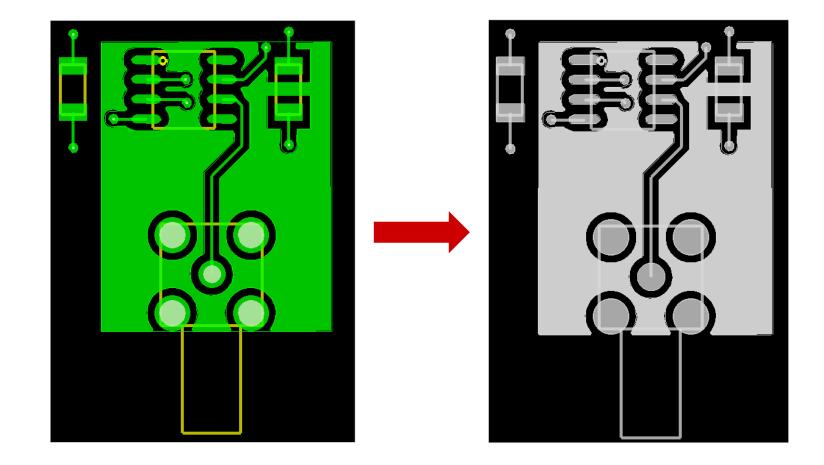
Note: Typical situation after importing third party Gerber data into Allegro – copper needs to be reanimated!!!



Cross Copy

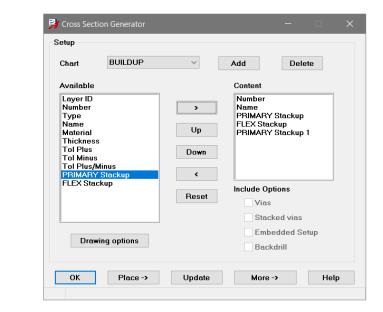
 \bigcirc

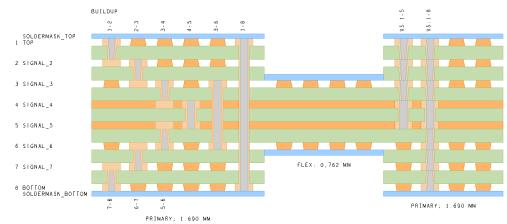
Example: Backup data on Board Geometry / Assembly_Notes for documentation purposes





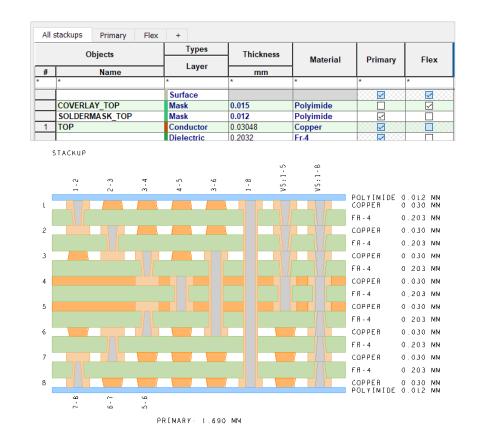
- Enhanced support for rigid-flex applications
- Customizable content
 - Custom charts with more meaningful visualization
 - Layer attributes, order, ...
 - Colors, fill styles, \ldots
 - Vias, stacked vias, backdrill and embedded status support
- SVG export
 - Export graphics for documentation purposes
- Configuration stored in db
- Automatic update

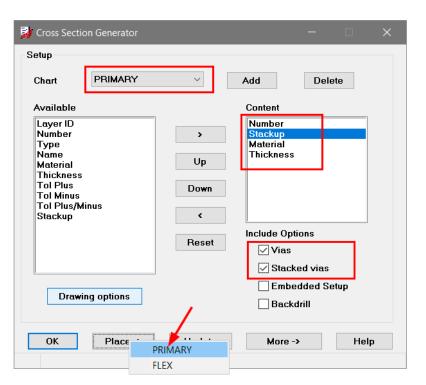






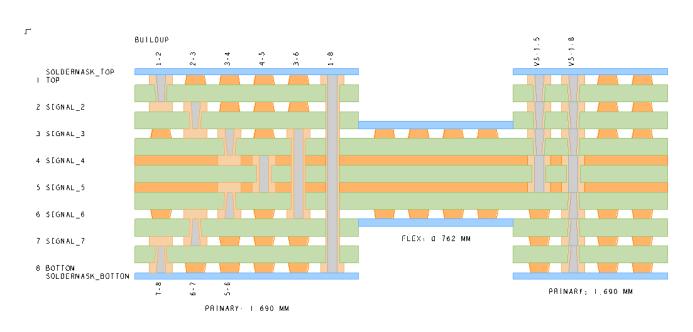
- Content can be defined for each stackup from cross section individually
- Also symbols can be placed individually

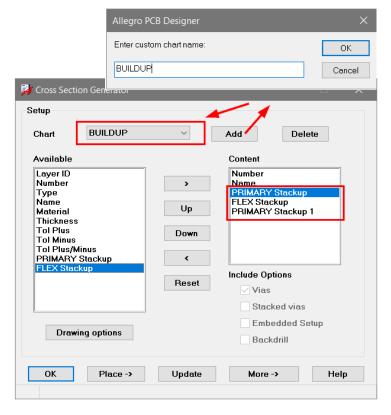






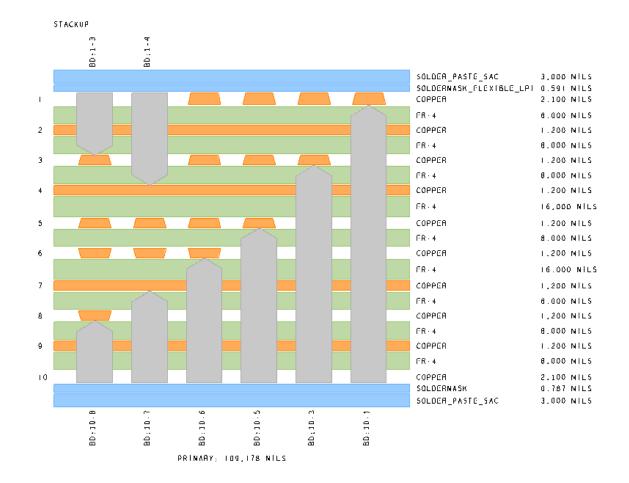
- A custom chart let's you combine stackups in an arbitrary order
- Feature many customer were asking for ...
- Additional information (vias, stacked vias, etc., can be applied to each stackup item individually)

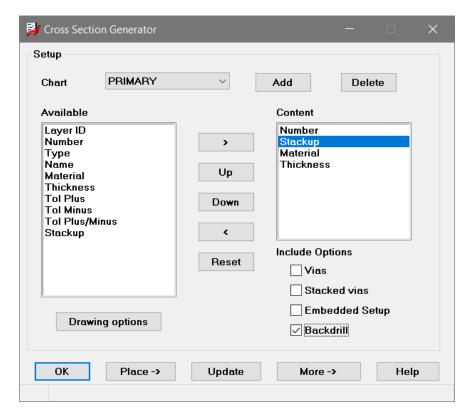






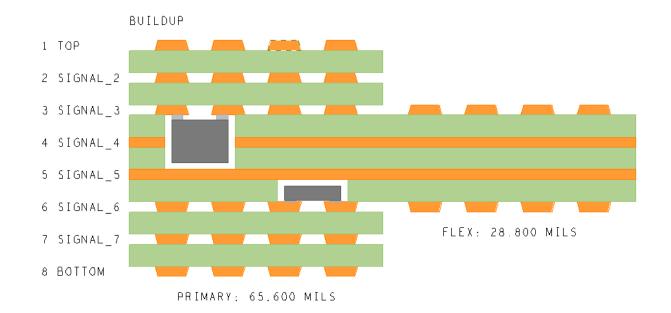
• Backdrill support

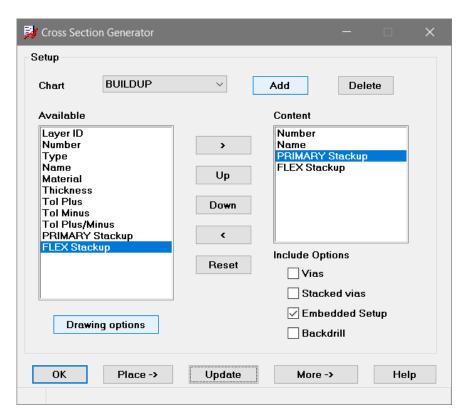






• Embedded component support







• Various drawing options

				Style	
) Design	○ SVG Export
				Conductor	\sim
🙀 Cross Section Generator		:	×	Conductor Dielectric Mask	
Symbol	Style			Via	
Symbol width 2000.000) Design	⊖ SVG Export		Drill span Backdrill Embedded Embedded	
Row spacing 0.000	Conductor	~		Text	
Column spacing 80.000	Color			Spacing	1
Text block 4	Shape	Fill		Fix height	80.000
Text block title 4	Width	4.000			
Proportional thickness	Spacing	20.000			
Type Log5 ~ Min height 80.000	Fix height	80.000			Fill V
				Width	Unfill Fill Hatch both
ОК		Help			Hatch pos Hatch neg
					·



• Export SVG

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- Mainly for documentation purp
- Separate color profile can be c

Style

🔿 Design

Mask

Color

Shape

		C	Gene	rated	by PCB E	ditor	×	+									_			\times
ion pu	rposes	\leftarrow	\rightarrow	C	0 0	atei D):/Develo	opment/	Projec	ts/XS	ectior	n/PRIM	1ary.	.svg			Q	☆	θ	:
	defined		Apps	լիհ	Chapter	26. Datan	na 🚸	FRITZ!B	ox 🧃) Sha	aring Li	ink Valio	dat	W	Dokumenttype	lefini				>>
can be	e defined		STACKUP				-													
			1.2		2-3	3.4	4-5	3.6		1-8	VS:1-5	-	VS:1-8							
		1													POLYIMIDE COPPER	0.012 N 0.030 N				
	Heln			[-7	Γ			FR-4	0.203 N				
More ->	Save settings	2													COPPER	0.030 N	им			
	Load settings														FR-4	0.203 N	им			
	Export SVG	3													COPPER	0.030 N	им			
															FR-4	0.203 N	м			
		4													COPPER	0.030 N	м			
tyle															FR-4	0.203 N	м			
-		5													COPPER	0.030 N	им			
🔿 Design	SVG Export														FR-4	0.203 N	м			
Mask	~	6													COPPER	0.030 N	м			
musk															FR-4	0.203 N	им			
Color		7													COPPER	0.030 N	M			
OL	Fill ~														FR-4	0.203 N	IM			
Shape	1 m •	8													COPPER	0.030 N				
Width	4.000	 	7-8		6-7	ê.									POLYIMIDE	0.012 N	n M			
	20.000				-															
Spacing	20.000						PRIMA	RY: 1.690 M	IM											



Custom Variables

- User defined variables in PCB Editor, useful for title blocks, etch texts etc.
- Similar to Design Entry HDL
- Automatic update of variables across all subclasses
- Variant support

- History capabilities
- Variable values can be sourced from external control file or even cpm-file

	variables Edit cont	ext USA 💌	Add Limit View	- 1
	Cult Cont			-
	Туре	Name	Value	1
1	С	DOC_NO	W30861-Q6789-MFG	
2	С	PROJECT	PN-5916-X-3	
3	С	TITLE	Control Unit	
4	С	VARIANT_NAME	USA Version	
	•			
Options		Specify	Filter display	• •
		Specify		
	Mapping	Specify Show All Hide All		

Title Co	ntrol Unit						
Project PN-5916-X-3							
Doc No. W30861-Q6789-MFG							
Variant USA Version							
- Size A3	Scale 1:1 Page 1 of 4						
7	8						



Custom Variables

Define Placeholders

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Parameters							
Variable name:							
PART_NUMBER							
Display value:							
<part_number></part_number>							
Destination layer							
Drawing Format 🔹							
□ Title_Block							
Attributes							
Block 3 Rot 0.0000							
Align Left v Mirror No v							
Advanced							
Type Standard 🔻							
History None							
Mode							
Add placeholder							
O Modify placeholder							
🔘 Delete placeholder							

Update Example

Cadence Design Sys	stems T	Title Control Unit						
B.4 RTM 1	0/31/15 RNICK							
A.2 Outline modification 0.	2/18/15 BWILKE	Project PN-4815-X-1						
A.1 Initial Release 0	D1/12/14 DTASIC C)oc No. W30861-Q1234-MFG						
	\	Variant Core Design						
Rev Descriptio		Poge 1 of 4						
Custom variables		8						
Edit conte	ext BASE 💌	Add Toggle Display						
Туре	Name	Value						
1 C	DATE	10/31/15						
2 C	DESCRIPTION	RTM						
3 C	DOC_NO	W30861-Q1234-MFG						
4 C	PROJECT	PN-4815-X-1						
5 C	REVISION	B.4						
6 C	TITLE	Control Unit						
7 C USER RNICK 8 C VARIANT_NAME Core Design 4 * Options Filter display Layer Mapping Specify Name Value OK Update history ->								



Design Compare

- Compares two databases and identifies the differences
- Useful when tracking changes in the product lifecycle
- Two modes

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- Standard Compare

Generates an HTML report with differences that apply to netlist, placement, BOM, testpoints, etc.

- Graphical Compare

Based on IPC-2581 all or individual layers can be compared graphically, differences will be highlighted, markers can be generated

对 Design Co	ompare							
Compare Designs								
First:	D:/design_projects/amplifier_v1.brd							
Second:	D:/design_projects/amplifier_v2.brd							
Options	Options							
C Stand	lard Compare (Netlist, Placement, BOM, Testpoints)							
Graph	nical Compare (based on IPC2581)							
□ u	Ise data from previous session (skip IPC export/import)							
V 🗸	create new database (Recommended): ipc_compare.brd							
🔽 U	lse default film definitions							
Ove	rride undefined width: Lines: 0.050 Texts: 0.050							
Units	Millimeters v							
	Start Cancel Help							



Design Compare

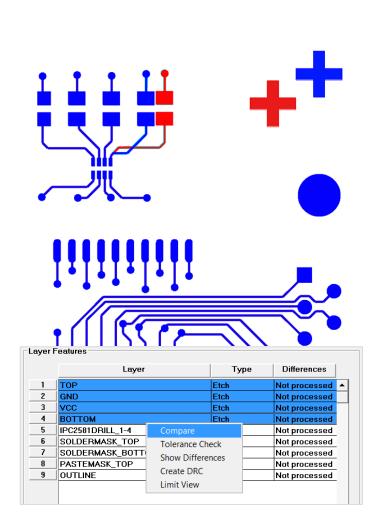
Standard Compare

- HTML based report
- Expand / collapse functionality facilitates navigation

	Design Compare Re × +								
🛞 file:	///D:/design_projects/design_c	com C Q Suchen	☆ 自 ♥	^	Ø 🖗	• • •			
collapse details									
						۵			
c <mark>a</mark> d e n c e°									
B E	ditor Design	Compare Re	eport						
Gene	eral								
Datal	base Info								
Stacl	kup								
oluoi	ica p								
Netli	st								
Components									
Com	ponents								
	-								
Sumi	mary								
Sumi	-								
Sumi	mary ement Changes	Design V2 (xy side angle)	Note]					
Sumi Place	mary ement Changes	Design V2 (xy side angle) (85.5800 82.1600)	Note]					
Sumi Place	mary ement Changes Design V1 (xy side angle)	(xy side angle)	Note Placement change						
Sumi Place Refdes	mary ement Changes Design V1 (xy side angle) (83.9900 82.1200)	(xy side angle) (85.5800 82.1600)		-					
Sumi Place Refdes	mary ement Changes Design V1 (xy side angle) (83.9900 82.1200) TOP	(xy side angle) (85.5800 82.1600) TOP		-					
Sumi Place Refdes	mary ment Changes Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000	(xy side angle) (85.5800 82.1600) TOP 90.0000							
Sumi Place Refdes	mary ement Changes Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200)	(xy ide angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100)	Placement change	-					
Sumi Place Refdes	Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP	(xy ide angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM	Placement change						
Sumi Place Refdes	Design V1 (xy side angle) (83.9900 82.1200) TOP 90.0000 (56.9900 35.1200) TOP 270.0000	(xy ide angle) (85.5800 82.1600) TOP 90.0000 (56.1000 34.3100) BOTTOM 180.0000	Placement change						

Design Compare

Graphical Compare



yer	Features				
	Lay	yer	Туре	Differences	
1	тор		Etch	7	
2	GND		Etch	11	
3	VCC		Etch	1	_
4	воттом		Etch	4	-
5	IPC2581DRILL_1-4		Drill	4	-
6	SOLDERMASK_TO		Mask	9	-
7 8	SOLDERMASK_BO PASTEMASK_TOP		Mask Mask	4	-
0 9	OUTLINE		Misc	0	-
	•				•
	n Compare	V1 :	Control (Selected on On/Off	Rais	e
	n			_	e
	n Compare	V1: V2:	On/Off On/Off On/Off	Rais	e
	n Compare Folerance Check Create DRC	V1: V2: Diff: Miscelle	On/Off On/Off On/Off	Rais Rais	e e
	n Compare Folerance Check Create DRC Show ->	V1: V2: Diff: Miscelle	On/Off On/Off On/Off aneous nit Check to outline o	Rais Rais Rais Rais extents only Min Area 0.02	e e



Digital Soldermask

- Additional features accounting for new technologies
- Developed together with Würth Elektronik
- Various modes
 - Pad ring / box
 - Trace mode
 - Component mode
 - By region
- Parameters
 - Bridge width
 - Pin, via gap
 - Length offset

- ...

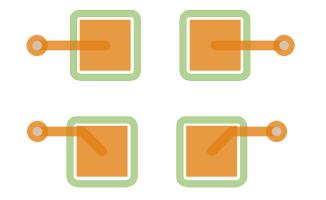
General			Diagram	
Region	DESIGN	 Create 	1	
Technology	Spray Coat	▼		Bridge width
Mode	Pad Box	•		t
Layer(s)	ТОР	▼		Length
Output	DIGITAL_SOLDER_1	▼ New		offset
Options				ŧ
Bridge width	0.12			Pin mask gap
Length Offset	0.10			r in mask gap
Pin mask gap	0.05			
Via mask gap	0.05	🗹 Use via hole		
Advanced				
Comp boundary	PLACE_BOUND	▼		a mask gap
Pad margin	0.15			
Min aperture	0.07			



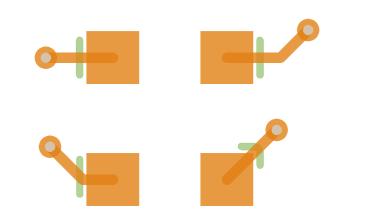
Digital Soldermask

Pad box

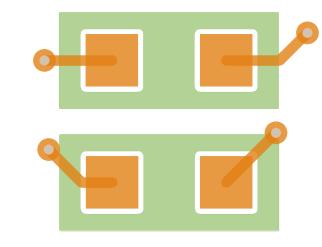
 \bigcirc



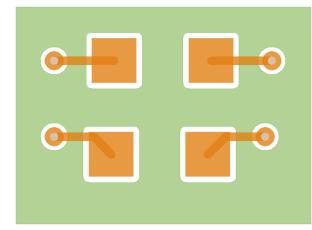
Trace mode



Component boundary



Soldermask region

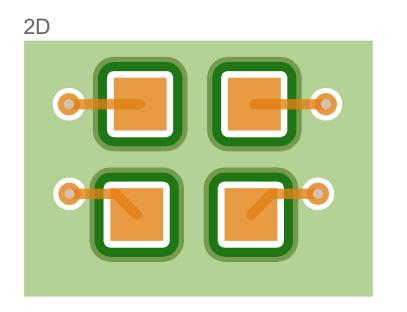




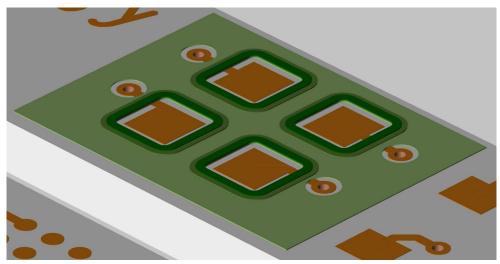
Digital Soldermask

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 Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness and thickness requirements



3D canvas



- In example above:
 - Solder mask region on Digital_Soldermask_1_TOP
 - Pad box on Digital_Soldermask_2_TOP
 - Pad box on Digital_Soldermask_3_TOP



- Includes useful functions for drafting purposes
- Functions support dynamic preview before changes are committed
- Several functions
 - Modify line

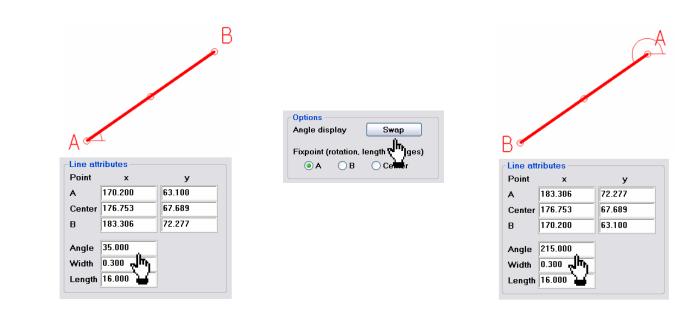
- Modify arc / circle
- Copy array line
- Copy array arc / circle
- Trim objects
- Cut objects
- Arc2Vector
- Ellipse

<u>T</u> ools	Flo	<u>W</u> are <u>H</u> elp		_
Q		Setup Display Edit	* * *	✓ # ■ # # # ₩
		Draft	•	Modify line
		Shapes	•	Modify arc/circle
		Check/Review	•	Copy array line
		Documentation	•	Copy array arc/circle
		Manufacture	•	Trim objects
		Signal Integrity	•	Cut objects
		Custom	•	Arc2Vector
		Miscellaneous	•	Ellipse
		Overview		Snap Generator



Modify line

- Change line attributes on a parameter basis: Coordinates as well as angle, width and length
- Angle display can be swapped
- Fix point for rotation and length changes can be chosen
- Fine-tuning capabilities for angle, width and length



Options		д • х	
		FlowCAD	
License	ed for:		
FlowCA	D, Internal Us	se Only	
CLine att	ributes		
Point	x	У	
Α	170.200	63.100	
Center	176.753	67.689	
в	183.306	72.277	
	05.000	7	
Angle	35.000	_	
Width	0.300		
Length	16.000		
)	
Options		Europ	
Angle d	lispiay	Swap	
Fixpoin	t (rotation, ler	ngth changes)	
() A	● A ● B ● Center		
Tuning			
Parameter Angle 🖌			
Increment 5.000 + -			



Modify arc / circle

- Change arc or circle attributes on a parameter basis:
 Center coordinate as well as radius, start angle, sector angle and width
- Fine-tuning capabilities

		>		×
~Arc/circle attribu	tes	-AI	rc/circle attribut	tes
Center X	127.000		Center X	124.000
Center Y	63.000		Center Y	65.000
Radius	10.000		Radius	4.319
Start angle	45.000		Start angle	
Sector angle	90.000		Sector angle	
Width	0.200		Width	0.300

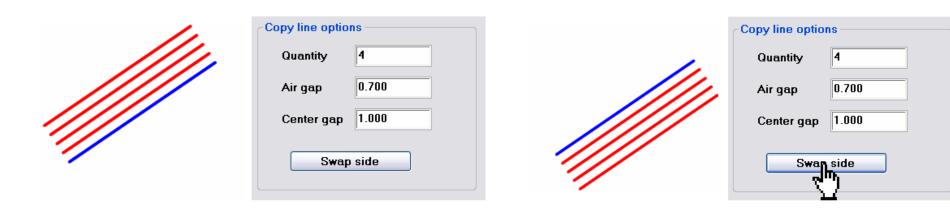
Options	μ ≁ ×
	FlowCAD
CLicensed for:	
FlowCAD, Interna	al Use Only
~Arc/circle attribu	Ites
Center X	127.000
Center Y	63.000
Radius	10.000
Start angle	45.000
Sector angle	90.000
	0.200
Width	0.200
T	
Tuning	
Parameter Ra	idius 👻
Increment 0.0	
Increment 0.0	



Copy array line

- Copies lines in parallel to a selected object
- Number of copies can be specified as well as air gap (or center gap respectively)
- Swap side

Options	τ * ×
	FlowCAD
CLicensed for:	
FlowCAD, Intern	nal Use Only
Copy line optio	ns
Quantity	4
Air gap	0.700
Center gap	1.000
Swap) side

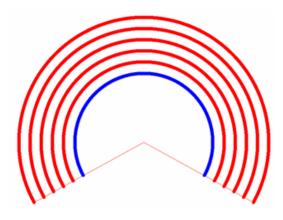




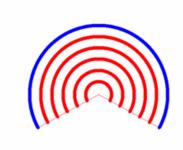
Copy array arc / circle

- Copies arcs in a concentric way to a selected object
- Number of copies can be specified as well as air gap (or center gap respectively)
- Direction can be chosen

Options	
	FlowCAD
Licensed for:	
FlowCAD, Intern	nal Use Only
Copy arc/circle	options
Copy out:	side
🔵 Copy insi	de
Quantity	5
-	
Air gap	0.700
Center gap	1.000



Copy arc/circle options		
Copy outside		
O Copy inside		
Quantity	5	
Air gap	0.700	
Center gap	1.000	



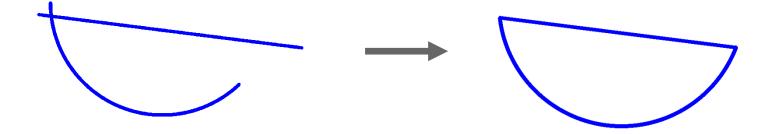
Copy arc/circle options		
○ Copy outside		
🖲 Copy insi	de	
Quantity	5	
Air gap	0.700	
Center gap	1.000	



Trim objects

- Trims object endpoints to calculated intersections
- Works with arcs and line objects
- Single point mode when two intersections are found (in case of arcs), ability to swap
- Trim vertex for both objects, first only or second only

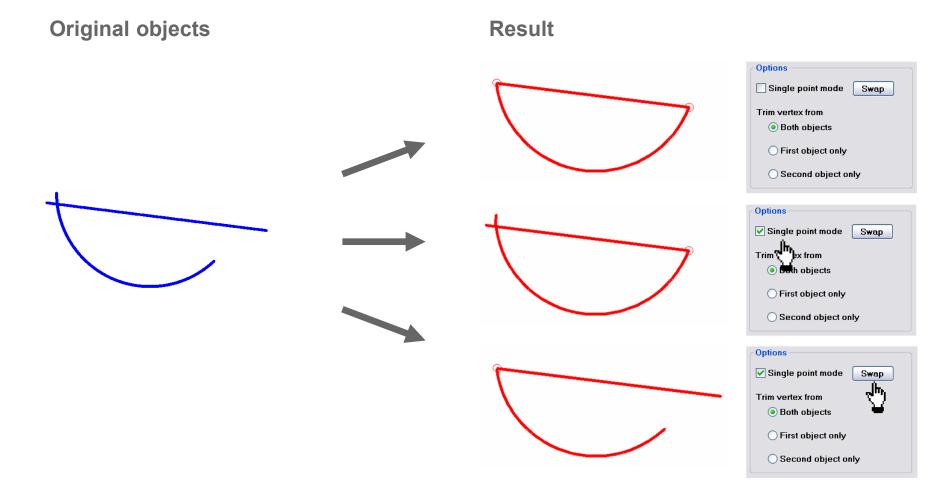
🔋 Options 🛛 🖡 👻 🗙
FlowCAD
Licensed for:
FlowCAD, Internal Use Only
Options
Single point mode Swap
Trim vertex from
Both objects
◯ First object only
O Second object only





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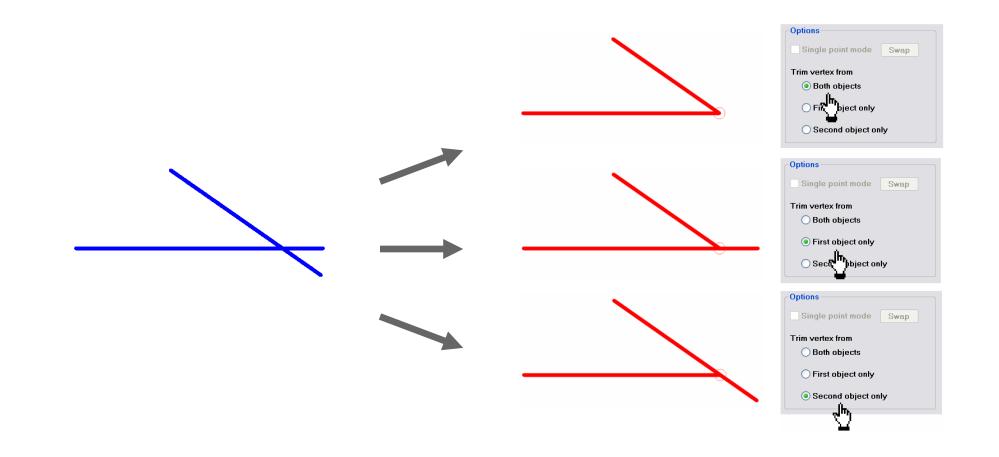
Trim objects: Single point mode





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Trim objects: Trim vertex from ...

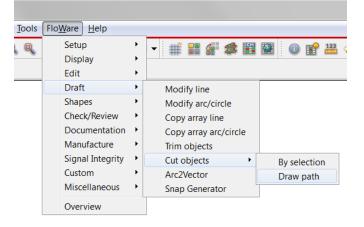


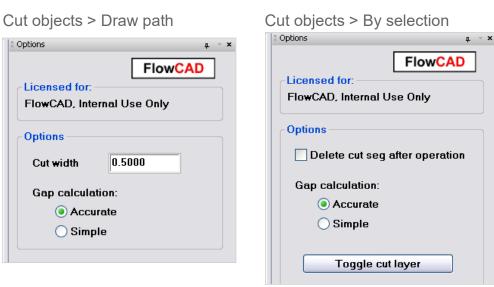


Cut objects

 \bigcirc

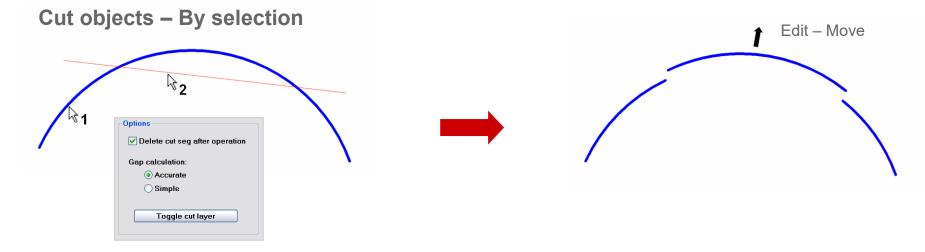
- Enables users to cut line, arc or circle objects for various purposes
- Two commands
 - Cut objects > By selection
 - Cut objects > Draw path
- Useful when layout portions need to be isolated before moving them to a new location



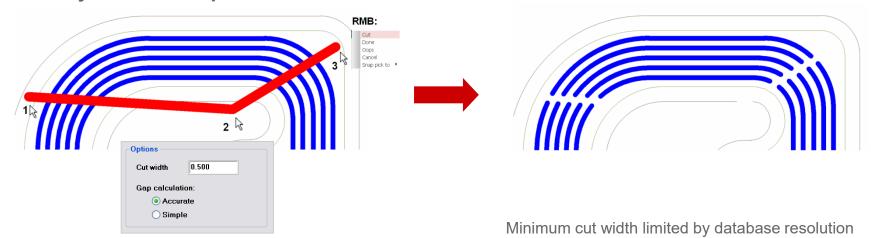


63





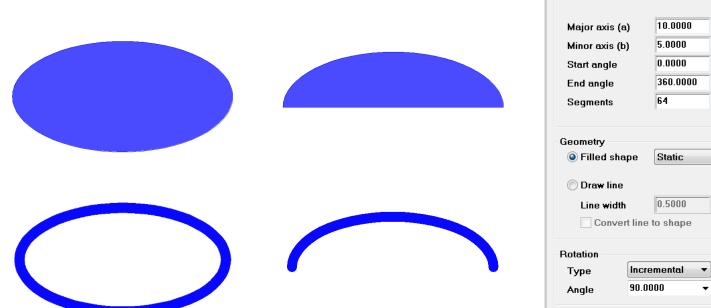
Cut objects – Draw path

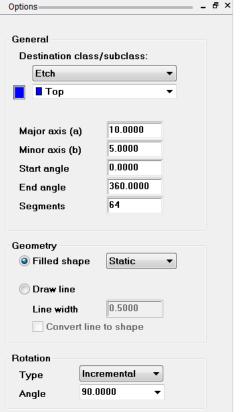




Ellipse

- Useful for pad shapes and RF applications
- Axis parameter **a** and **b**
- Geometry
 - Full
 - Partial (specify start, end angle)
- Type
 - Solid filled shape
 - Draw line path
- Number of segments



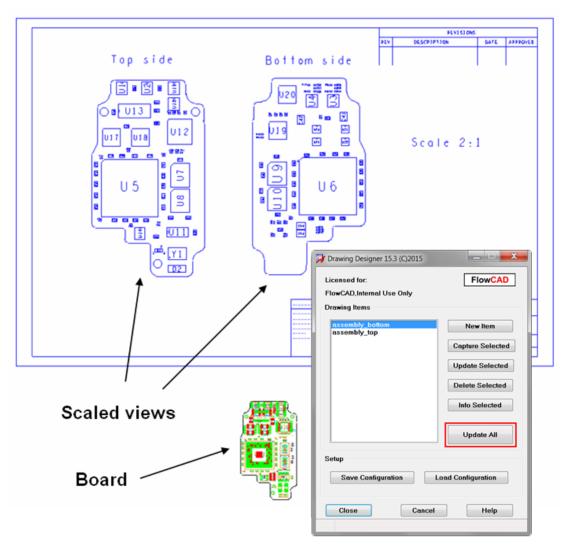




Drawing Designer

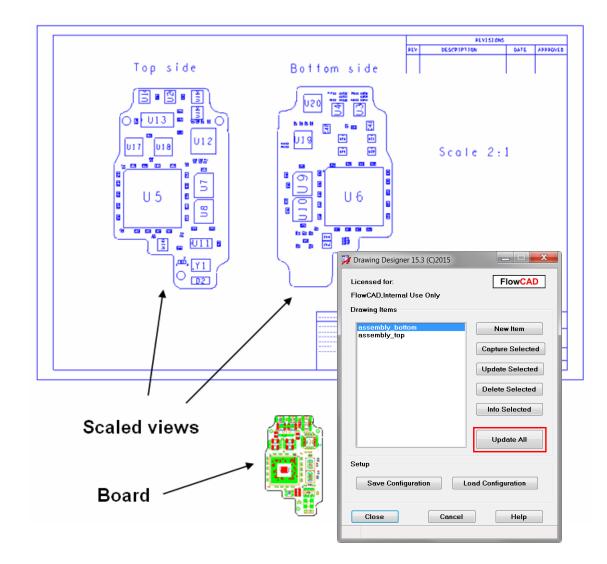
- Useful when creating manufacturing drawings
- Records the creation of scaled views (including mirroring and rotation)
- Automatic updates

- Configuration stored in database
- Configuration export and import





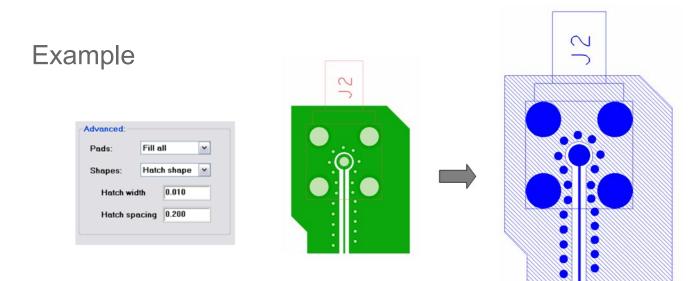
Drawing Designer



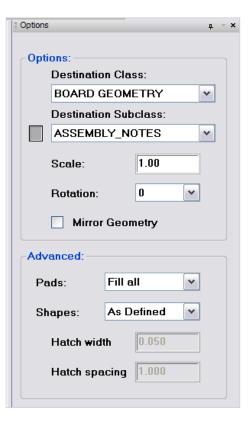


Drawing Designer

- Ministatus panel offers various options when creating new drawing items
 - Destination layer where data is written to
 - Scale, rotation, mirror of the item
 - Pad style: filled, unfilled
 - Shape: As defined, unfill all, hatched



Note: Hatch option only applies to solid filled shapes

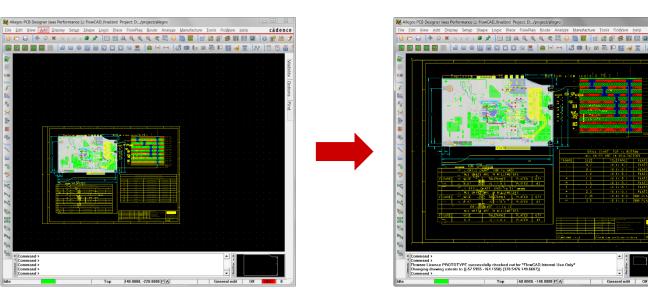




Drawing Size

- Let's you change the design extents in a quick and easy way
- Useful if you want to reduce design extents to minimum values
- Settings can be applied to all or individual sides

材 Drawing Size		
Mode		
Expand Contract	🔘 Minimum extents	Drag window
Options		
Offset 100.000	Side All sides	
Close Apply Help		

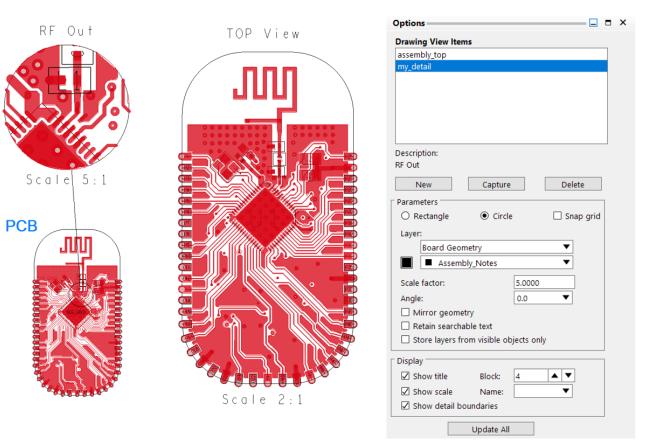




Drawing View Manager

- Facilitates creation of manufacturing drawings
- Features

- Capture named drawing view items interactively
- Clipping capabilities using rectangular or circular boundaries
- Scale, mirror, rotate
- Retain object colors
- Automatic update
- Template support

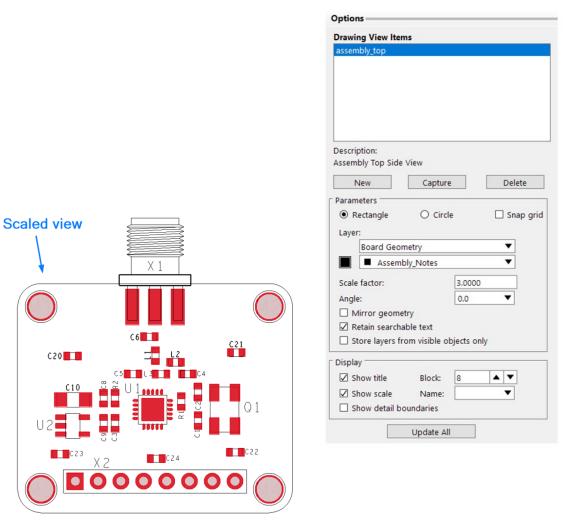




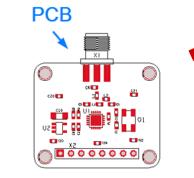
Drawing View Manager

• Simple use model

- Press **New** and enter a name
- Select item from the list
- Press Capture
- Adjust layer visibility and find filter ...
- Adjust mirror, scale, rotation ...
- Place item
- Use Update All once PCB was modified







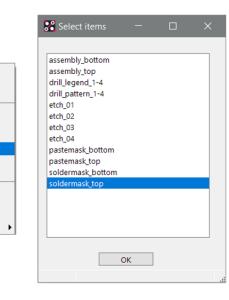


Drawing View Manager

• Template support

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- Significantly shortens setup time
- Eliminates the need to create drawing view items each time from scratch in a new project
- Information about visible layers, objects, source area, destination layer, scaling etc. is already pre-defined
- Default templates located in share/pcb/toolbox/config/drawingview
- SITE and pcbenv customizable
- Use model
 - RMB Choose Template and select an item
 - If necessary adjust scale etc.
 - Place item



Done

Oops

Cancel

Capture

Update

Delete

Info Selected

Snap pick to

PCB

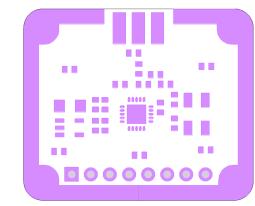
Update All Delete All

Add/Edit Description

Choose Template

New



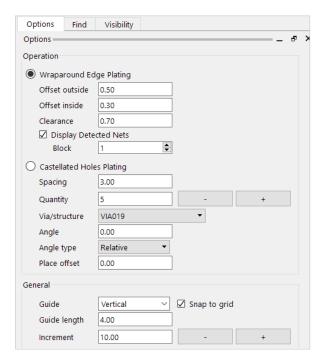


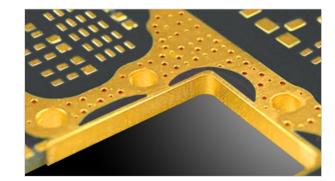
Scale 2:1



Edge Plating

- Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed
- This plated conductive material may be used for many functions
 - Improve current carrying across multiple layer of a PCB
 - Edge connection protection
 - Board to case grounding
 - EMC signal integrity
 - Heat management
- Two forms of Edge Plating
 - Wraparound (Side) Plating
 - Castellated Holes



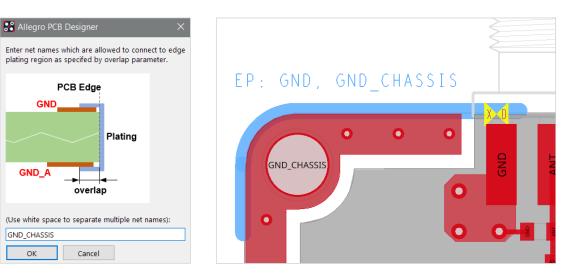




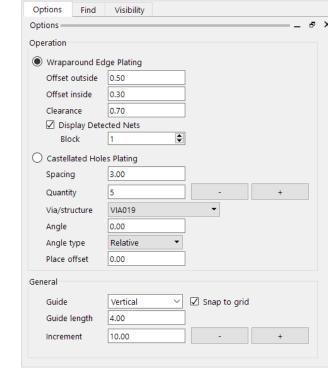


Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support



GND_CHASSIS





Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
 - Spacing

- Quantity
- Objects supported
 - Vias
 - Via structures
 - Symbols
 - Electrical components
- Placement parameters
 - Alignment with outline (relative, absolute)
 - Offset from outline

	Options Find Visibility
	Options e >
	Operation
	O Wraparound Edge Plating
	Offset outside 0.5000
	Offset inside 0.3000
	Clearance 0.7000
	Display Detected Nets
	Block 1
	Castellated Holes Plating
	Spacing 3.0000
	Quantity 5 - +
	Via/structure VIA_C500_D200
	Angle 0.0000
	Angle type Relative 👻
	Place offset 0.0000
	General
	Guide Vertical 🗸 🗹 Snap to grid
	Guide length 4.0000
	Increment 10.0000 - +
ノ) ― 〜 X	



FPGA Utilities

- Check and report any pin swapping which has been done in a PCB layout
- Export pin constraints to csv and vendor specific formats
 Altera, Xilinx, Actel, Lattice
- Works in both flows
 - Allegro Design Entry HDL
 - OrCAD Capture
- Various options

🐉 FPGA Utilities 16.4 (C)2016		
Licensed for FlowCAD,Inte	rnal Use Only	FlowCAD
General	indi oco only	
	IC1	
Reference Designator:		
Vendor Format:	Altera Quartus	•
Parameters		
Use pin name as FPG	A IO-Name	
🔘 Use net name as FPG	A IO-Name	
Create unique names		
ECO Mode (LVL-Chec	k)	
Original Connectivity	Report:	
Filter Output		
Exclude pins connecte	ed to DC-Nets (Volta	ige Property)
Exclude pins with pinu	se Power or Ground	
Exclude unconnected	pins	
Exclude pins which die		e only)
Output Format		
Sort by pin number	🔘 Sort by IO	-Name
Generate	Close	Help

FPGA Utilities

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		🔀 Pin Constraints file, Vendor format	
		🔎 🗱 🗁 🖬 🖨 🎱 Search:	🚱 🕘 🗌 Match word 🗌 Match case
	tera Quartus	<pre># Pin Constraints for Xilinx XDC # # Design: D:/demo/placed.brd </pre>	^
	Pin Constraints file, Vendor format	Apr 05 15:41:47 2018	
Differences Report #= # Pin Swap Report: Text Format	Pin Constraints for Altera Quartus	Y PACKAGE_PIN P14 Y PACKAGE_PIN R16 Y PACKAGE_PIN N16 Y PACKAGE_PIN N13	[get_ports {AD[0]}] [get_ports {AD[1]}] [get_ports {AD[2]}]
9 🗙 🖻 🖬 🖨 🥥 Search:	Match word Match case 15:43:23 2018	Y PACKAGE_PIN L15 Y PACKAGE_PIN N15 Y PACKAGE_PIN P15	[get_ports {AD[3]}] [get_ports {AD[4]}] [get_ports {AD[5]}] [get_ports {AD[6]}]
<pre># Pin Swap Report # # Design: D:/demo/placed.brd # compared with # File: D:/demo/initial.txt</pre>	gnment PIN_P14 gnment PIN_R16	-to AD[0] y PACKAGE_PIN M15 -to AD[1] y PACKAGE_PIN M13 -to AD[2] y PACKAGE_PIN K14	[get_ports {AD[7]}] [get_ports {AD[8]}] [get_ports {AD[9]}] [get_ports {AD[10]}] [get ports {AD[11]}]
# # Date: Apr 05 15:40:22 2018 # # Ref PinName Slot OldPin NewPin OldType NewType #	oldNet NewNet gnment PIN_L15 gnment PIN_N15	-to AD[3]	[get_ports {AD[12]}] +
U101 AD[8] G1 M14 L16 BI BI U101 AD[10] G1 M15 M13 BI BI U101 AD[15] G1 L16 M14 BI BI U101 AD[15] G1 L16 M14 BI BI U101 AD[7] G1 M13 M15 BI BI U101 GPIO[1] G1 P7 N6 BI BI	A9A4gnment PIN_P15BD14A8gnment PIN_M15A7A10gnment PIN_L16A8BD14gnment PIN_N14A10A7gnment PIN_N14BD0BD1gnment PIN_M13A4A9gnment PIN_K14	-to AD[6] -to AD[7] -to AD[8] -to AD[9] -to AD[10] -to AD[11]	
U101 AD[2] G1 P15 N16 BI BI U101 GPI0[2] G1 P6 P5 BI BI U101 GPI0[4] G1 P5 P6 BI BI U101 KB_KSOP_0[5] G1 N6 P7 BI BI	A6 A2 BD4 BD2 BD2 BD4 BD1 BD0 A2 A6		

Xilinx XDC



Highlight Dummy Pins

- Assigns a color to all pins in a design which are not connected to any net
- Including report and cross probe functionality
- Useful for review purposes

 \bigcirc

💽 Dummy Pin Report	🙀 Highlight Dummy Pins 📃 🗖 💌	
<u>File</u> <u>C</u> lose <u>H</u> elp	Options	
U1.13 (65.405 69.215) U1.16 (69.215 69.215) U1.17 (69.215 78.74)	✓ Dummy nets	
U101.1 (73.66 69.215) U101.12 (87.63 69.215) U101.13 (88.9 69.215)	✓ Single node nets	
U101.16 (92.71 69.215) U101.17 (92.71 78.74) U102.1 (73.66 82.55)	Highlight Clear	
0102.12 (87.63 82.55) 0102.13 (88.9 82.55) 0102.14 (92.71 82.55)	C Report Only	
U102.17 (92.71 92.075) U17.7 (28.575 50.8) U18.6 (-1.905 96.52)	Close Apply Help	
019.13 (26.289 46.66) 019.15 (23.749 46.66) 019.17 (21.209 46.66)		
019.19 (18.669 46.66) 02.1 (50.165 82.55) 02.12 (64.135 82.55)	Assign Color	
U2.13 (65.405 82.55) U2.16 (69.215 82.55)		
U2.17 (69.215 92.075) U22.1 (60.833 48.768) U22.3 (60.833 43.688)		
U22.5 (68.453 41.148) U22.6 (68.453 43.688) U26.13 (166.405 86.438)	Next>> Cancel	

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IBIS Prototype Modeler

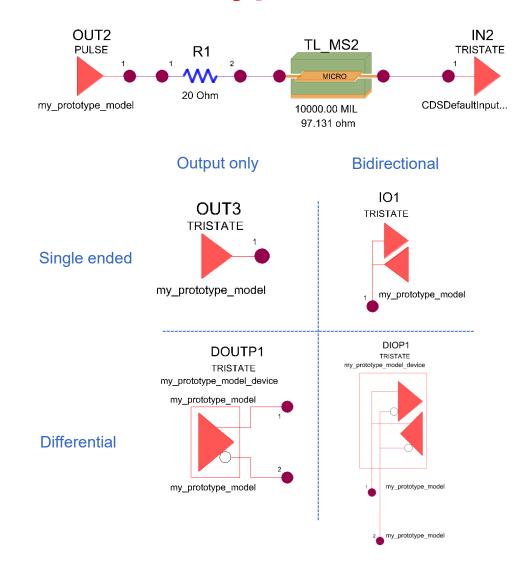
- Creates scalable IBIS models for early stage signal integrity analysis
- Features include

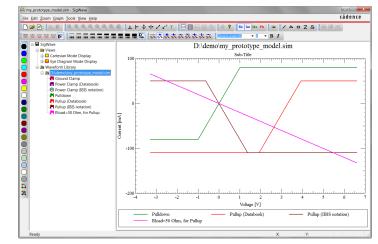
- Ability to create Push / Pull, Open-Sink and Open-Source buffers
- Adjustable voltage levels
- Adjustable internal resistance including a calculator
- Adjustable slew rate dV / dt
- Ability to include saturation and clamping effects
- Support for single-ended as well as differential outputs
- Support for output only and bidirectional models
- Ability to view curves in Sigwave
- Generate DML models as well as native IBIS models

Licensed for Model type –	FlowCA),Interna	l Use Only	/				FlowCAD
Operation (1998)	Pull driv	er	🔘 Ор	en sink	driver		Open so	urce driver
General		_			_			
Voltage leve	ls: Vo	H 3.	300 V	v	oL 0.	000 V	Vra	nge 3.300 V
Driver streng	th: Rs	lope 1	2.500 O	hm	Cal	culate		
Slew rate:	Tr	ise O.	.250 n:	s @	0 / 9	0% 🔻		
Options								
🗸 Include se	turation							
Pullup ci	irve:	lpu min	-110.000	mA	lpu max	55.000	mA	Set limits
Pulldowr	curve:	lpd min	-80.000	mA	lpd max	80.000	mA	Set limits
🔽 Include cla	amping							
Power cl	amp:	Vpcl	4.100	v	Rpcl	0.500	Ohm	
Ground o	amp:	Vgcl	-0.800	v	Rgcl	0.500	Ohm	
Model as	differenti	al outpu	t					
Model as	I/O (type	bidirect	ional)					
Output								
Model nam	e: my_p	orototype	e_model					
				Write D		Write		Help

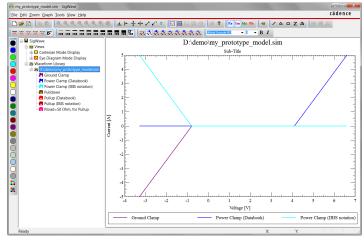
IBIS Prototype Modeler

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Pullup, Pulldown and Rload curves



Power, Ground clamp



Label Generator

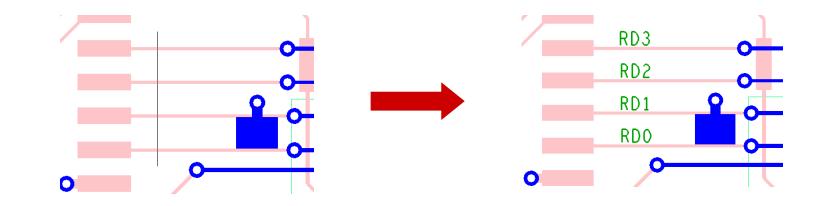
- Creates signal name and pin labels for documentation purposes
- Selectable label content (e.g. signal same + pin number)
- Individual label origin (e.g. pin, or via origin, but also cursor intersecting cline)
- Aligned text rotation mode (text angle value follow cursor gesture)
- Supports three different object types (pin, via, cline)
- User defined text size, justification and rotation

Options	Find	Visibility
options		
		FlowCAD
Licensed	l for: –	TIOWORD
FlowCAE),Intern	al Use Only
Display	Conten	it:
NET_N	IAME	•
Manufac	turing s	subclass:
FLW_L	ABEL_	NOTE 🔻
Object Fi	ilter:	
Pin	C	Cline 💿 Via
Text Filte	er:	
Text Blo	r.k.	1
Text Rot		
Text Jus		LEFT V
Text Offs		0.0000
Text Offs		0.0000
Text Mirr		
T BALIMIT	01.	
ſ	01-	ar All



Label Generator

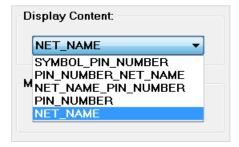
Procedure

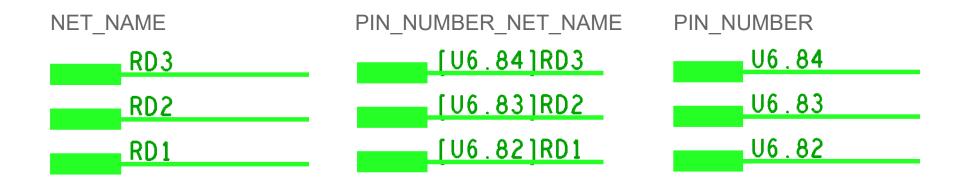




Label Generator

Label Content







Label Tune

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- Adjusting component labels automatically
 - Better readability
 - Saves a lot of time when creating assembly drawings

• Features

- Label can be chosen (e.g. Refdes, Value, Part Number, …)
- Automatic rotate, center, fit
- Automatic mirroring
- Visibility control
- Various options
 - Max block size, max height
 - Boundary clearance

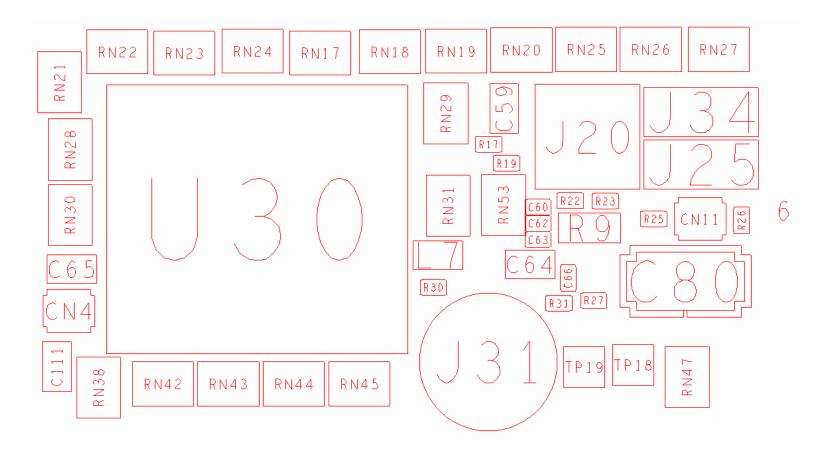
abel Tune			对 Label Tune	
ain Advanced		1	Main Advanced	
Objects			Text rotation	
Label name	Refdes	-	Congest side	
1 - b - l l	Assembly		TOP horizontal:	0 🔻 deg
Label layer	Assembly		TOP vertical:	90 🔻 deg
Outline data	Assembly	-	BOTTOM horizontal:	0 🔻 deg
			BOTTOM vertical:	270 💌 deg
Visibility control	Top On/Off		C Fixed angle	0 🔻 deg
Limit layers	Top On/Off		 Relative angle from syn 	nbol definition
	Bottom On/Off			
			Text center	
Components on bott	om side		Offset correction:	0.00
Label mirrored			⊤Text fit	
			 Specify by height 	
Mode				
Rotate text			Min 0.50 M	ax 15.00
			O Specify by block	
Center text			Blocks 1-35	
Dx 0.	00 Dy 0.00		BIOCKS 1-55	
Fit text			Clearance to boundary:	0.000
				1
Close	Cancel Hel	p	Close Cancel	Help



Label Tune

 \bigcirc

Typical situation in PCB Editor



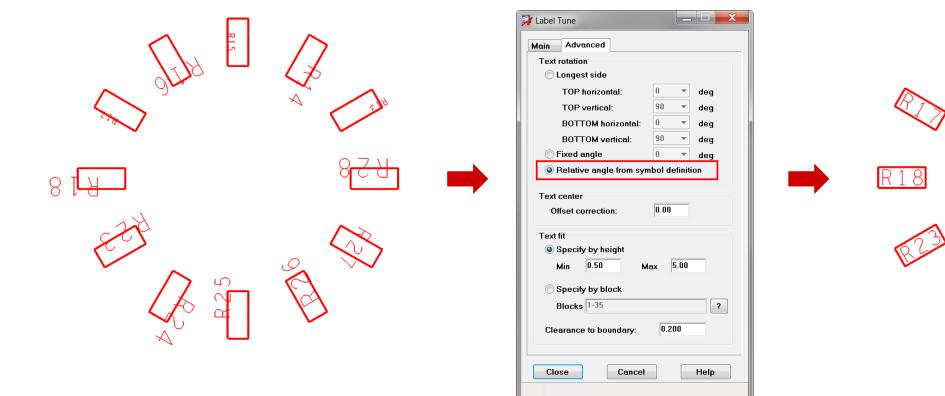
Result after running Label Tune

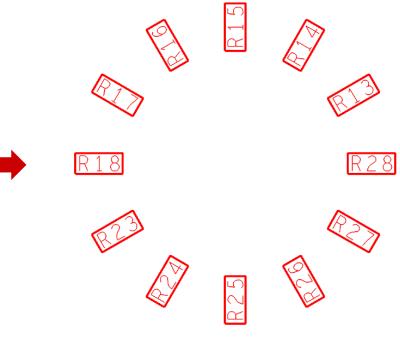
Animation

Label Tune

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Another example







Mask Generator

- In some cases customers may want to oversize mask data (soldermask, pastemask) due to manufacturing requirements
- Data will be generated on manufacturing subclass. The original padstacks won't be touched
- Input parameters
 - Source data ("What to oversize") can be specified separately for vias and pins
 - Oversize values (positive and negative)
 - Side to process
 - Manufacturing subclass where data will be written to

🙀 Mask Generat	or			
Pin objects			Via objects	
Source	Etch pad	-	Source	Drill hole 💌
Oversize	0.010		Oversize	0.010
Options				
Process side	e	Both	•	
Manufacturin	g subclass	MSK_C	V10U ▼	New
	Ж	Ge	enerate	Help

Pin objects	
Source	Etch pad 🔹
Oversize	Soldermask Pastemask Etch pad





Mask Generator

Pins and vias on TOP

Manufacturing subclass MSK_OV30U_TOP

Mask Generator Pin objects Source Etch pad Oversize 0.030 Options Process side Manufacturing subclass	Via objects Source Oversize	Etch pad V 0.030	
ОК	Generate	Help	



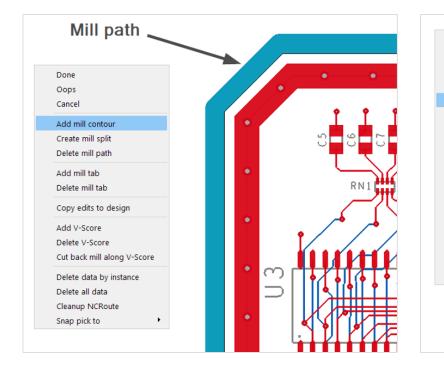
- Toolset supporting various techniques for PCBs in a panel to be easily separated after they are manufactured and assembled
- Mill tab panels

- Add mill contour
- Split & Cut mill
- Add mill tabs with or without perforation drills
- V-Score panels





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Add mill contour along the edge of the board

Create splits interactively

Markers

1

2

•

Done Oops

Cancel

Add mill contour

Create mill split

Delete mill path

Add mill tab

Delete mill tab

Add V-Score

Delete V-Score

Delete all data

Snap pick to

Cleanup NCRoute

Copy edits to design

Cut back mill along V-Score

Delete data by instance

Delete splits

Done

Oops

Cancel

Add mill contour

Create mill split

Delete mill path

Add mill tab

RN

Guide

 \sim

Delete mill tab

Add V-Score

Delete V-Score

Delete all data

Snap pick to

Cleanup NCRoute

Copy edits to design

Cut back mill along V-Score

Delete data by instance

1

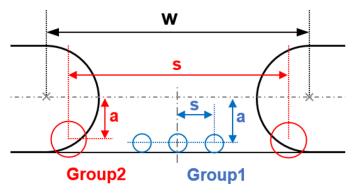
٠

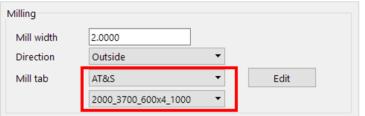
 \sim

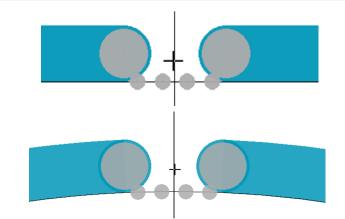


- Mill tabs can be specified with respect to

 Tab size
 - Number of holes, diameter spacing and offset
- Application provides libraries from PCB fabricators – AT&S
 - Fineline
 - Alba PCB Group / Q-print electronic
- Interactive placement
 - Can be placed on any contour



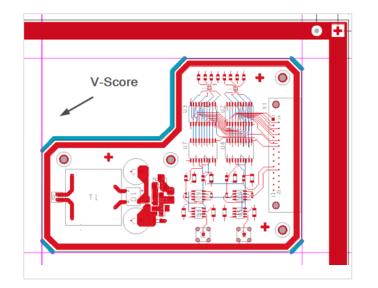


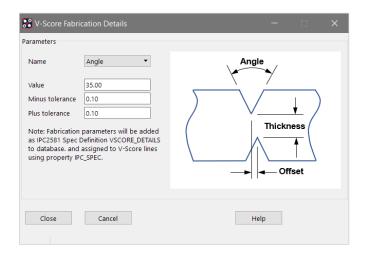


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- V-Score lines can be defined in horizontal or vertical directions by selection an appropriate side of the board
- Existing milling can be cut back
- V-Score fabrication details can be specified which creates an IPC-2581 Spec Definition entry in the database

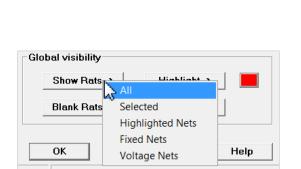


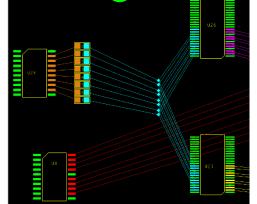




Net Color View

- Allows saving and restoring net color and rat visibility settings
- Useful for floor planning and route feasibility studies
- Global visibility commands
 - Useful hands-on for configuring a view (display / blank rats and assign net colors)
 - Find By Name support
 - No need for jumping and travelling to standard commands from PCB Editor





View name io	_interface 💌
Save	Restore Misc ->
Save options	Restore options
✓ Visible rats	Complete
Colored nets	C Toggle
Global visibility	
Show Rats ->	Highlight ->
Blank Rats ->	Dehighlight ->

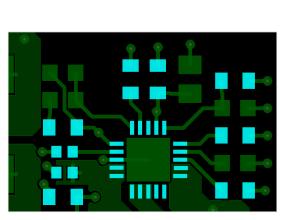


Padstack Finder

- Enables users to search and navigate for padstacks in the current design
 - Filter capabilities
 - Distinguish between pins and vias
 - Padstack name
 - Drill size

- Wildcard support
- Highlight and cross probe
- Color by group

<u>File Close H</u> elp			
Name	Location	DrillSize	Start<->End
SMD0 75X0 65R	(164.3 81.0)	0.0	TOP<->TOP
SHD0 75X0 65R	(164.3 79.7)	0.0	TOP<->TOP
SHD0 75X0 65R	(164.3 52.0)	0.0	TOP(-)TOP
SHD0_75X0_65R	(164.3 50.7)	0.0	TOP<->TOP
SHD0 75X0 65R	(163.3 81.0)	0.0	TOP<->TOP
SHD0 75X0 65R	(163.3 79.7)	0.0	TOP<->TOP
SHDO 75X0 65R	(163.3 52.0)	0.0	TOP<->TOP
SHD0_75X0_65R	(163.3 50.7)	0.0	TOP<->TOP
SMD0_75X0_65R	(130.6 19.0)	0.0	TOP<->TOP
SMD0_75X0_65R	(130.6 20.0)	0.0	TOP<->TOP
SMD0_75X0_65R	(90.3 26.7)	0.0	TOP<->TOP
SMD0_75X0_65R	(90.3 27.7)	0.0	TOP<->TOP
SMD0_75X0_65R	(48.0 47.5)	0.0	TOP<->TOP
SMD0_75X0_65R	(49.0 47.5)	0.0	TOP<->TOP
SMD0_75X0_65R	(49.0 46.2)	0.0	TOP<->TOP
SMD0_75X0_65R	(48.0 46.2)	0.0	TOP<->TOP
SMD1_0X0_8R	(175.25 85.4)	0.0	TOP<->TOP
SHD1_0X0_8R	(175.25 82.0)	0.0	TOP<->TOP
SHD1_0X0_8R	(175.25 78.6)	0.0	TOP<->TOP
SHD1_0X0_8R	(175.25 56.4)	0.0	TOP<->TOP
SHD1_0X0_8R	(175.25 53.0)	0.0	TOP<->TOP
SMD1_0X0_8R	(175.25 49.6)	0.0	TOP<->TOP
SMD1_0X0_8R	(173.55 85.4)	0.0	TOP<->TOP
SMD1_0X0_8R	(173.55 82.0)	0.0	TOP<->TOP
SMD1_0X0_8R	(173.55 78.6)	0.0	TOP<->TOP





Filter Objects:	Show pins	Show v	vias
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SMD1_1X			_
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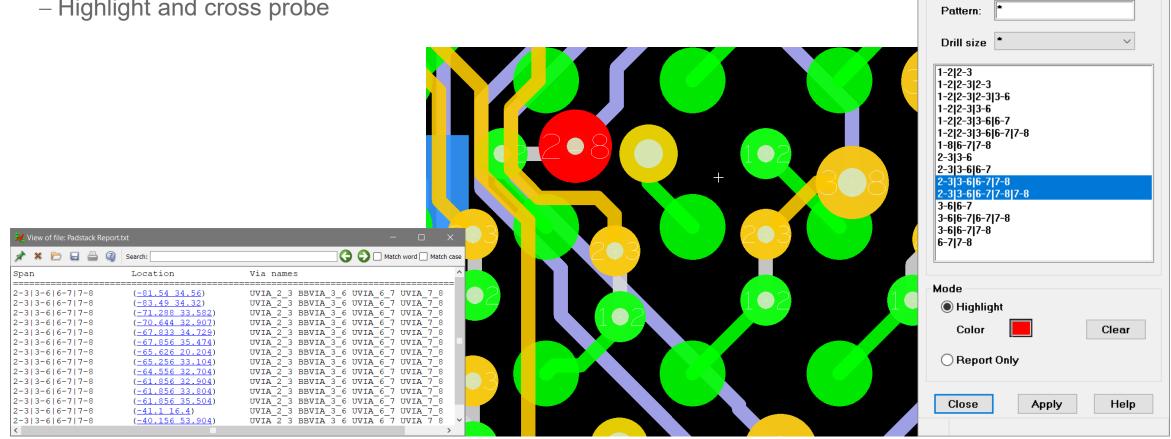
Padstack Finder

Objects: Stacked Vias

Filter

Padstack Finder

- Now supporting Vias Stacks
 - Display label formed by individual drill spans
 - Highlight and cross probe





Padstack Usage

- Generate padstack reports by extracting data from PCB Editor symbol libraries (*.dra). Different reports are available:
- Report types

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- Where-Used
 Lists all footprints that use a given padstack
- Padstack Standard
 Lists the padstack definitions for a given footprint
- Padstack Detailed

Lists detailed information for a given footprint. This information includes number of pins, vias and mechanical pins, pin numbers, xy coordinates, etc.

- Report format
 - -HTML
 - -Excel
 - Text

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Padstack Usage

Report examples

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		lcc44			-	smd30_55			Pi	_	cir60_37d	2.540	0.000				
nd30_96	1	lcc52		lcc28	2	smd30_55 smd30_94			Pi	n 3	cir60_37d	5.080	0.000				
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 18

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6	smd25_94	1	lcc48			
7	smd2_25x1_8r	1	ind_ihlp-1616			
8	smd2_45x2_35r	1	ind_s4924			
9	smd30_115	1	lcc24			
10	smd30_55	4	lcc20			
11			lcc24			
12			lcc28			
13			lcc44			
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15			lcc68			
	smd30_94	3	lcc20			
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	smd30_96	1	lcc52			
	smd4_0x3_0r	1	ind_ssm063 header30			
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22						



- Simplifies panel documentation process
- Boards can be stepped individually or by array
- Boards can be rotated and / or mirrored individually
- Automatic update
- Automatic notification if boards have been modified
- Based on proven mdd-Technology (Design Reuse, Place Replicate)
- Supports standard panels as well as family panels
- Configuration stored in database

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- Setting up a new panel
 - Open a new database or panel template
 - Launch FloWare > Panelization
 - Link your boards
 - Create modules
 - Place a single instance or an array of your board
 - Done
- Updating an existing panel (e.g. original layouts have been modified)
 - Open the panel database
 - Launch FloWare > Panelization
 - Choose Update panel
 - Done
 - Create manufacturing data as usual ...

🎸 Paneliza Main	setup		
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OK	Update	panel Status	Cleanup Help





- Interactive placement
 - Place single instances or array
 - Dynamic preview attached to cursor (board size, orientation, rotation, mirror)
 - Display design bounding box or actual outline
 - Snap to grid option

	2
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P P P	2

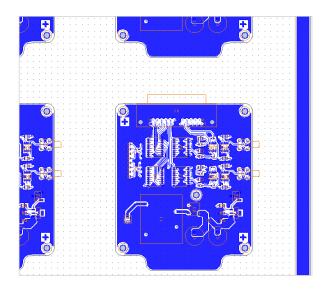
Display bounding box

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Mode Place single instance Place instance array	Options Display actual outline Display module extents Snap to grid
Close	Help

Display actual outline

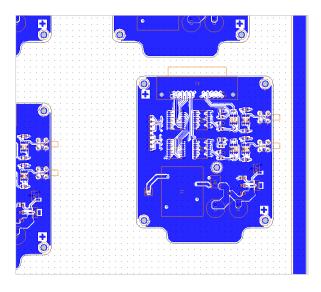


- Panel modifications
 - Change parameters (e.g. x, y) of instance to be changed
 - Fields become yellow
 - Choose context menu Update changes to confirm



	ld	Design		x		Y	
1	P1	AMPLIFIER		76.000		220.000	
2	P2	AMPLIFIER		76.000		82.000	
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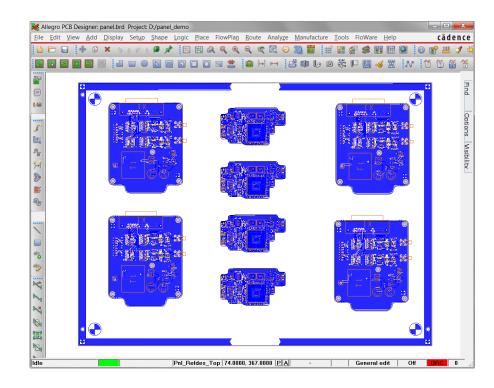
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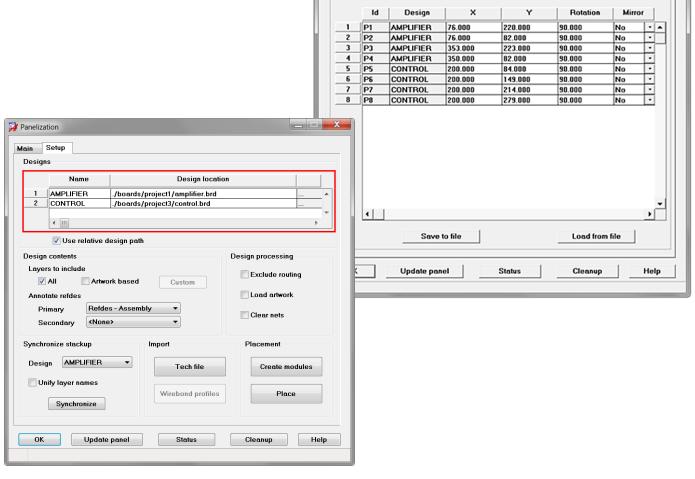
Panelization

• Family panels

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- Contain more than one board layout
- Simply link the board databases
- Make your placement





Panelization

Main Setup

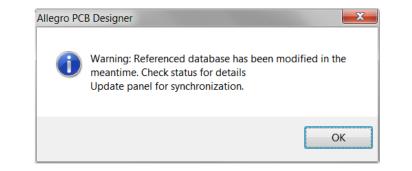
Panel list



• Panel status

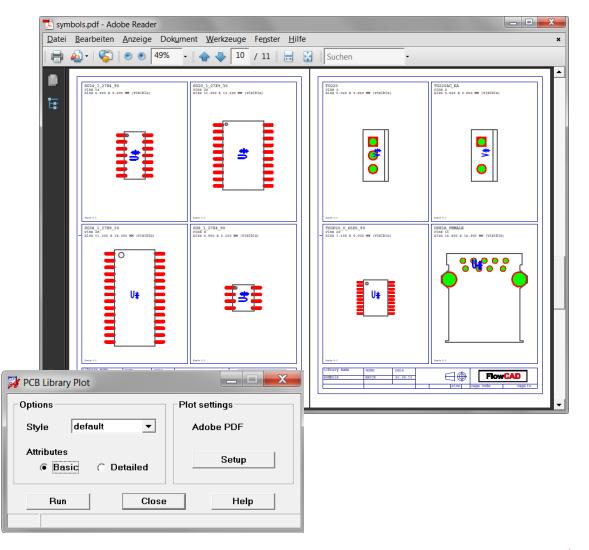
- Automatic notification when board databases have been modified
- Status report gives details about time stamps

		Design	1 14	1 1	I Deterior	1		
	Id	Design	×	Y	Rotation	Mirr	10	
1	P1	AMPLIFIER	76.000	220.000	90.000	No		٠
2	P2	AMPLIFIER	76.000	82.000	90.000	No		
3	P3	AMPLIFIER	353.000	223.000	90.000	No		
4	P4	AMPLIFIER	350.000	82.000	90.000	No		
5	P5	CONTROL	200.000	84.000	90.000	No		
6	P6	CONTROL	200.000	149.000	90.000	No		
7	P7	CONTROL	200.000	214.000	90.000	No		
8	P8	CONTROL	200.000	279.000	90.000	No	•	
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P2	AMPLIFIER		11:27:55 2012		
P3	AMPLIFIER		11.27.55 2012		
P4	AMPLIFIER	000 10	11.27.55 2012		
P5	CONTROL	Oct 12	11:27:55 2012		
P6	CONTROL	Oct 12	11:27:55 2012		
P7	CONTROL	Oct 12	11:27:55 2012		
P8	CONTROL	Oct 12	11:27:55 2012		
Design	Last Modifie	d	Path		
AMPLIFIER CONTROL	Oct 12 11:45 Oct 12 11:23			ards/project1/amp ards/project3/com	

- Documentation of PCB footprints within a selected library
 - Includes graphical representation of footprint graphics
 - Graphics will be scaled into dedicated areas for better readability
 - Additional attributes (size, pitch, padstacks used etc.) are automatically extracted and written to the document
 - Frame templates are provided
 - Customizable contents and drawing styles including drill holes
 - One single PDF document for all footprints





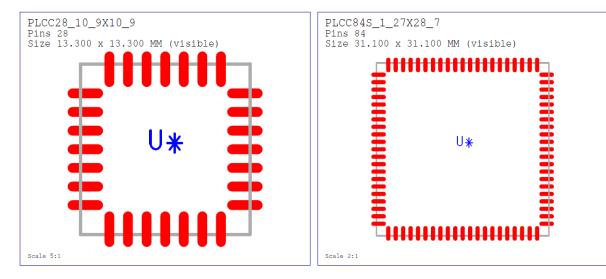
Default Mode

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- Basic information
- More footprints per page

Detailed Mode

- Additional information
- Less footprints
 per page



PLCC28_10_9X10_9

Scale 5:1

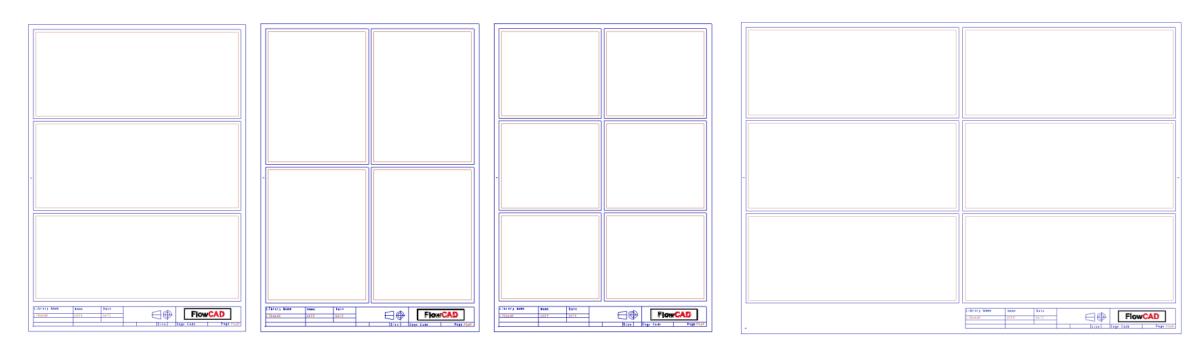
	Attributes:				
	Size				(visible)
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• Templates

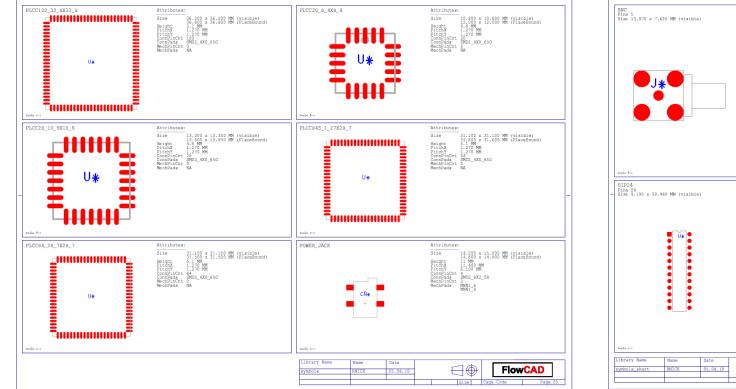
- Define the areas to be used for plotting which correlates to the number of footprints per page
- Metadata support for title blocks (page number, date, user, library name)
- Default templates provided
- Customer can define his own templates





Examples

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6 footprints on A3

Detailed attributes

7 DIP8 Pins 8 Size 9.195 x 10.160 MM (visible) $\exists \oplus$ FlowCAD

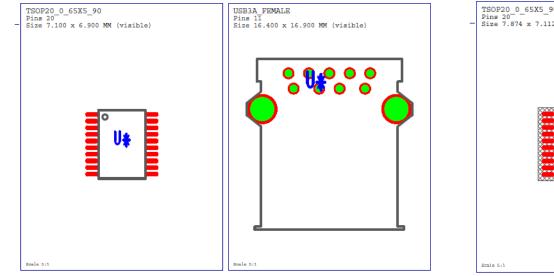
DIN64 Pins 64 Size 19.050 x 93.980 MM (visible)

4 footprints on A4 Basic attributes

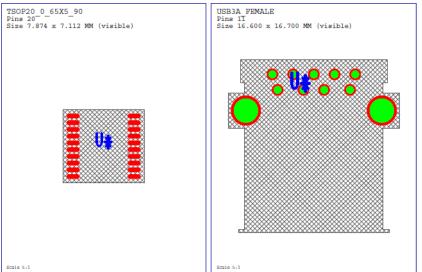


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Customizable content including drill holes and various drawing styles



Assembly TOP including etch and drill holes



Placebound as hatch shape including etch and drill holes

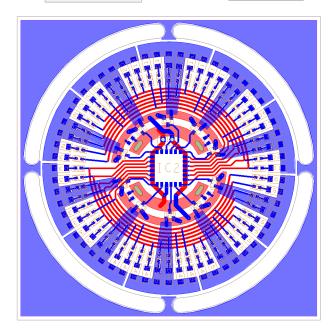
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- Useful for boards where circular placement and routing is required
- Providing a set of functions
 - Defining and editing a polar grid
 - Polar placement
 - Polar routing

- Polar shape editing including voids
- Snap control
 - Coarse and fine grid
 - System grid
- Polar grid can be also used in conjunction with standard PCB Editor commands using
 RMB > Snap pick to > Intersection

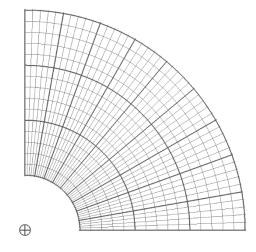
Tools	Flo <u>W</u> are <u>H</u> elp			
l Q	Setup Display))	- # # # \$ \$	🖺 🎦 💿 😭 🏭
	Edit Draft Shapes Check/Review Documentation	>	Advanced Mirror Change Width Coil Designer Cross Copy Label Tune	
	Manufacture		Polar Grid	Setup Grid
	Signal Integrity Custom Miscellaneous	Push to Grid Replace Via Shield Generator	Place Route Shape	
	Overview	Ļ	Shield Routing	Shape Void

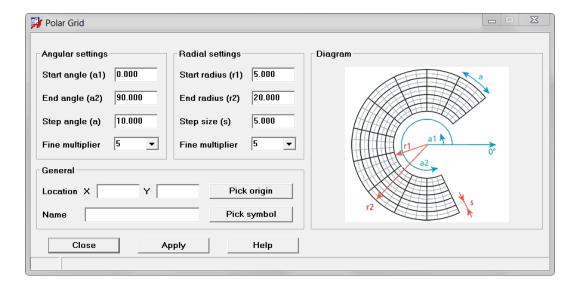


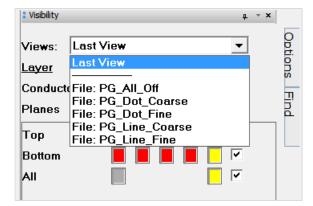


Polar Grid Setup

- Define a new grid
- Edit an existing grid
- Fully parameterized
- Coarse and fine grid settings
- Line and dot style support
- Stored as format symbol in database
- Visibility control

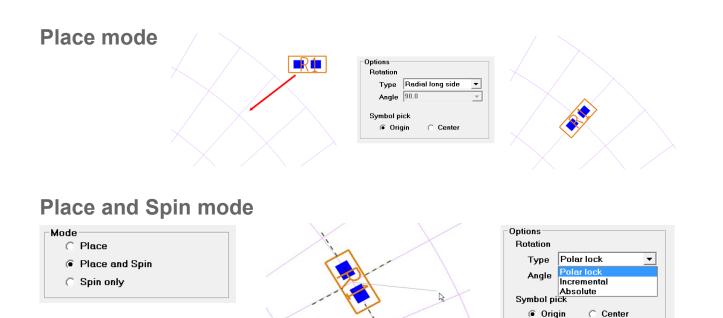








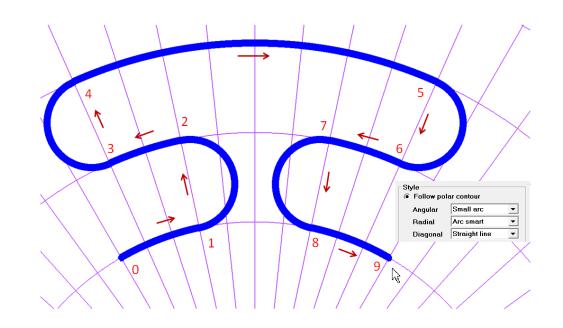
- Polar placement
 - Special mode for placing component in circular or radial fashion
 - Snap to fine or coarse grid
 - Various alignment and rotation capabilities
 - Spinning on polar grid basis (e.g. Polar lock)



Mode			
Place			
O Place	and Spin		
🔿 Spin o	•		
Snap options			
🔽 Coarse	Show	Lines 🔻	
🔽 Fine	Show	Dots 💌]
System	Show		
Options			
Rotation			
Туре 🛛	Radial lor	ıg side 🛛 💌]
Angle 🤅	30.0	-	
Symbol pic	k		
Origin	n O	Center	



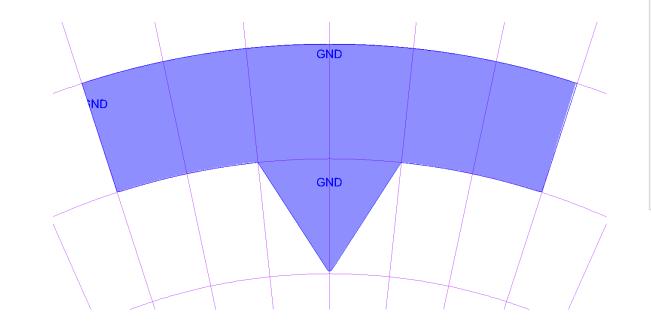
- Polar routing
 - Special mode for drafting or routing in a circular or radial fashion
 - Snap to fine or coarse grid
 - Ability to follow radial and angular contour
 - Alternate path options (e.g. **Arc smart**)



otions		
General		
Etch		-
📘 📘 Тор		-
Line width	.200	
Add connect	options (e	etch only)
🔲 Snap to	o connect	point
Via VIA		•
Snap options		
 Coarse 	Show	Lines 🔻
Fine	Show	Lines 🔻
Custom	Show	
System	Snow	
	SNOW	
Style Style		Jr
Style		
Style Follow po	lar contou	urc 💌
Style Follow po Angular	lar contou Small a	t line
Style Follow po Angular Radial	lar contou Small a Straigh	t line
Style Follow po Angular Radial Diagonal	lar contou Small a Straigh	t line



- Polar shape and void editing
 - Special mode for creating shapes and voids in a polar grid
 - Snap to fine or coarse grid
 - Ability to follow radial and angular contour
 - Alternate path options (e.g. **Arc smart**)



Options			р - ×			
General Etch Constant Net		▼ ▼				
Type Dynamic copper 💌						
Snap options Coarse Fine System	Show Show Show	Lines 💌 Lines 💌				
Draw style						
Angular	Small a	arc 🔻				
Radial	Straigh	t line 🔻				
Diagonal	Straigh	t line 💌				
Pen width	0.100					



Post Processing

- Central cockpit from which manufacturing output can be configured and generated
- Hit Button solution many users are asking for
- Tasks can be enabled / disabled, added and removed individually
 - Standard functions from PCB Editor
 - Skill procedures (e.g. FloWare)
 - User defined scripts
- Jobs can be defined which contain a collection of tasks
- Configuration stored in database
- Import and Export capabilities for the purpose of standardization

Post Proces	ssing		_
Tasks Co	nfiguration		
Job:	default	Add new	Delete
	Update Shapes Cross Section Clean Data: ./mfg/* Standard BOM Variant BOM: core Variant Assembly: NC Drill Legend NC Drill Data NC Route Data Artwork Data Standard Plot Batch Plot: all Mfg Collector Zip Data: output.zip	core	
All C	Dn All Off	Save	Load
Ru	n Ci	ose	Help



Post Processing

- Context menu provides task editing – Info
 - Tasks can be added (appended or inserted)
 - User tasks
 - Predefined tasks including arguments
 - Tasks can be removed if not needed at all

🙀 New Task			
New task			
Add use	er task		
Name	dxfout	Title MyDXF Out	put
Script	C:\Cadence\:	scripts\dxfout.scr	
Predefi	ned task		
		▼ Arg	
Info			
0	ĸ	Cancel	Help

b:	default 👻	Add new Delete	5	🧚 New	/ Task					
				New	task					
🗹 🔷	Update shapes									
🗆 💊	Custom variables (*)			\bigcirc	Add use	r task				
🗆 💊	Cross section (*)				Name	dxfout	Title	MyDXF Outpu	ıt	
🗆 🔶	Clean data: ./mfq/*.*				, tunio		indo [, ,		
🗹 📏	Standard BOM			:	Script	C:\Cadence\scr	ipts\dxfou	t.scr		
🗋 💊	Variant BOM: core (*)									
🔾 💊	Variant Assembly: co	re (*)		۲	Predefin	ied task				
🔾 💊	Drawing designer (*)			1	Undate	Shapes 🔻	Ara	all_variants		-
	NC drill legend	Info			Artwork	•	nig	an_rananto		
	NC drill data	Insert task			Batch P					
🔽 💊	Artwork data	Append task			Clean D Cross S					
🔽 💊	Standard plot					Variables				
	Batch plot: all (*)	Delete task			Mfg Col					
	Rename files				NC Drill	Data Legend				
□ •	i tendine mes				NC Rou					
					Standar					
					Standar	d Plot Shapes	Cancel		Help	
						Assembly				
					Variant	BOM				

Zip Data

Job:



Post Processing

• Additional built-in functions

- Clean Data

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Performs file delete operations based on arguments provided including wildcards

– Standard BOM

Generates standard BOM in text and csv format

- Standard Plot

Plots all artwork film control records into one PDF file artwork.pdf

– Rename Files

Provides powerful automated file renaming mechanism (wildcards, variables and pattern tags) for PLM purposes

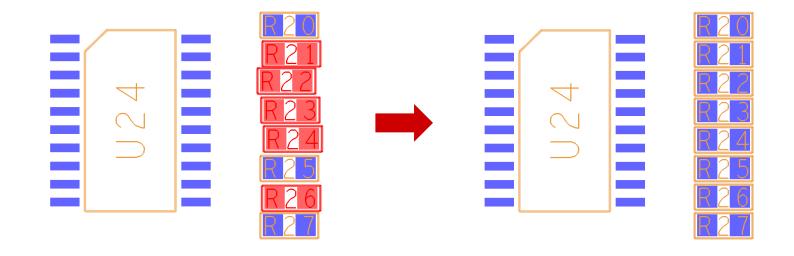
۲	Predefined task			
	Clean data	~	Arg	./mfg/*.*
"mfg curr	g/*.art" or "./*.log". U ent working directory	lse rela are no	ative pa t accep	ed in wildcard format, e.g. "mfg/*", athes only. Directories outside the oted. When deleting files in the specify an extention. (e.g. "./*.log")

Dir	Ext.	1 1	Match	1	F	Rename	to	Move t	0
mfg	art	*		(Dr	oject_no>_<	filos ab	,	fab	_
mfg	drl	routed-*			oject_no>_<			fab	_
plot	pdf	±	-		e>_assembl			fab	
piot	csv	*BOM*		-	e>_assenibi e>.bom	7. pui		fab	-
			Add Row Delete Row						
•									•
▲	:d		Delete Row	ort/l	Import				•



Push to Grid

- Placement application featuring
 - Highlight off grid symbols
 - Option to move / push symbols to the nearest grid point
 - Regular placement mode for standard placement operations
 - Single and multiple selected symbols
 - Including mirror and spin support



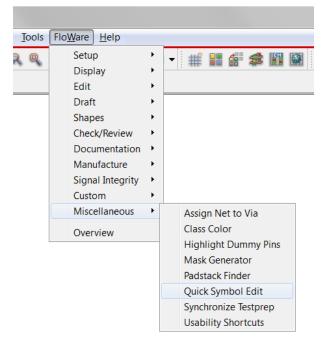
Options	₽ ~ X
General	
All grids 1.0	
Mode	
Highlight only	
Move to grid	
Place regular	
Options Exclude mechanical symbols Exclude fixed symbols Rotation increment 45	
Display Highlight color	
Dehighlight ->	



Quick Symbol Edit

- Opens symbol editor out of a layout database for viewing or editing purposes
- Three modes

- Edit same session
 - Acts similar to Tools > Modify Design Padstack (next slide)
- Edit new session
 - Launches a new session and open the symbol dra file
- Export only
 - Only exports symbol data (dra, psm, pad, etc.) for the selected symbol to a specified directory





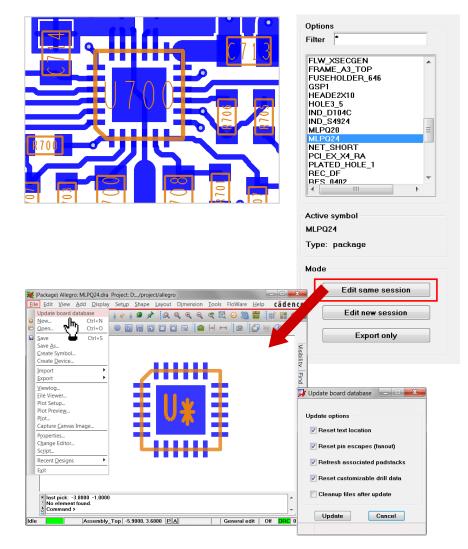
Quick Symbol Edit

- Edit same session
 - Seamless edit and update of a symbol definition in board context
 - Acts like Tools > Modify Design Padstack

- Steps:

(

- 1. Launch Quick Symbol Edit in layout context
- 2. Select a symbol
- 3. Current database closes, symbol dra file will be opened
- 4. Make your modifications
- 5. Finally choose File > Update board database
- 6. Specify update settings
- 7. The layout database from which the command was launched opens again and the footprints will be updated





Replace Via

- More flexibility while replacing vias in the design
 - Specify padstack names
 - Restrict replacement to selection area
 - Include and exclude vias from the specified area through interactive commands
 - Additional filter options, e.g. distinguish between
 - Vias with or without testpoint status
 - Mirrored or unmirrored vias
 - Processing options
 - Allow DRC
 - Ignore Fixed
 - Retain Mirror Status

3 Replace Via 17.2 (C)2017	
Licensed for FlowCAD,Internal Use Only	FlowCAD
Via Filter	Filter Options
Old: VIA0_2C0_5C •	✓ Test Status Testpoint ▼
New: VIA0_3C0_7C	✓ Mirror Status
Selection	Processing
Include vias	Allow DRC
	Ignore Fixed
Vias selected: 0 Clear	Retain Mirror Status
Close Replace	Report Help



Shape Utilities

- Includes useful functions when editing shapes
 - Boolean operations
 - Size operations (Expand, Contract, Size)
 - Rectangular shapes with rounded corners
 - Advanced boundary edit functions
 - Stretch
 - Cut

- Round off vertices
- Change round off radius
- Modify individual arc parameters
- Modify shape priorities
- Check status

<u>T</u> ools	Flo <u></u>	<u>W</u> are <u>H</u> elp		
Q		Setup Display Edit Draft)))	
		Shapes Check/Review Documentation Manufacture Signal Integrity Custom Miscellaneous Overview		Boolean Size Rounded Rectangle Advanced Boundary Edit Change Priority Check Status

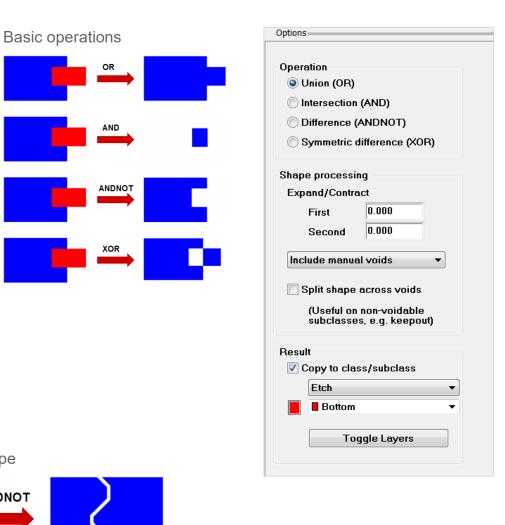


Shape Utilities – Boolean Operations

- Features
 - OR, AND, ANDNOT, XOR
 - Supports shape-shape operations as well as shape-line and shape-text operations
 - Shape attributes (shape type, fill style, net name etc.) are retained and applied to the resulting shape
 - Ability to split shapes across voids
 - Expand / contract capabilities
 - Useful for general editing and basic RF-applications

Cutting a dynamic shape

ANDNOT



Etching negative texts into copper



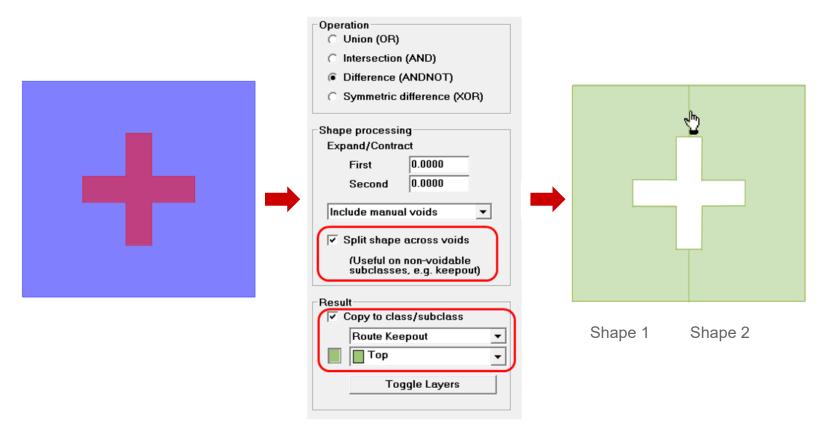


Shape Utilities – Boolean Operations

• Let's you also split shapes across voids

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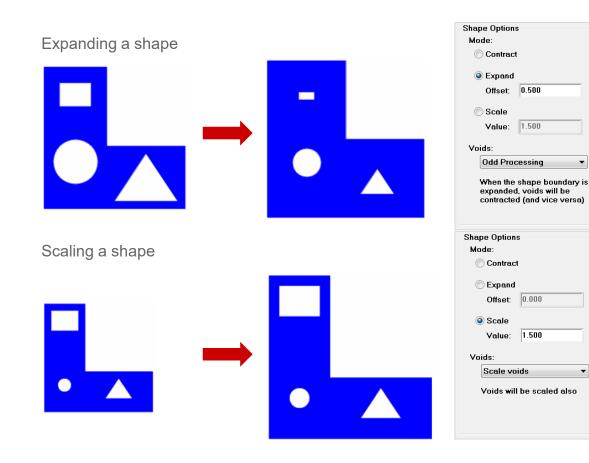
• Useful when working on non-voidable layers such as KEEPOUT, NO_PROBE etc.





Shape Utilities – Size Operations

 Expand / Contract similar to Edit > ZCopy but directly acts on selected shape. No copies remain. Additional options for void handling



Options	
Shape Options Mode: © Contract	
Expand Offset: 0.000	
Scale Value: 1.000	
Voids:	
Ignore voids 🔹 🔻	



Shape Utilities – Rounded Rectangular Shapes

- Useful when defining pad shapes
- Size can be specified exactly

 \bigcirc

• Reference point can be chosen by using negative values for width and height

	Parameters	
	Shape width: 20.00	
Basic operation	Shape height: 5.00	Options
	Corner radius: 1.00	Destination layer
	Center to pick	Etch •
	Shape width: 20.00 Shape height: 5.00	Bottom -
		Parameters
	Shape width: 20.00 Shape width: 20.00	Shape width: 1.00
Specify shape origin	Shape height: -5.00 Shape height: 5.00	Shape height: 1.00
	Shape width: 20.00	Corner radius: 0.00
	Shape height: 5.00	Center to pick
	Center to pick	

- Supports several modes
 - Stretching of shapes
 - Cutting of shapes

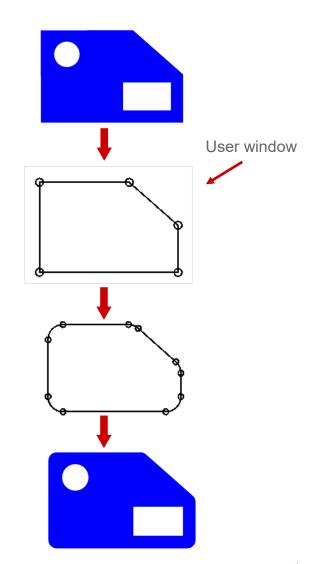
- Rounding off vertices
- Changing existing round off radius
- Modifying individual arc segments of a shape
- All modes within one command
 Including Oops support
- Additional features
 - Can also edit voids (Find Filter)
 - Supports single pick as well as window selection (several vertices)
 - Snap to grid, Trim to selection window
 - Display control (e.g. handle size)

	FlowCAD
Licensed for:	
FlowCAD, Inter	rnal Use Only
Stretch/Cut mo	nde
Stretch bou	
-	2
Cut bounds	-
Snap to	grid
Trim to	selection window
Bound Off mo	de
Round off y	
~	
Change rou	
Radius	1.000
0	ode
unange arc m	
Change arc m Mofify indiv	
Change arc m Mofify indiv Cent X	
Mofify indiv Cent X	vidual arc - 1.000 +
Mofify indiv Cent X Cent Y	vidual arc - 1.000 + - 1.000 +
Mofify indiv Cent X	vidual arc - 1.000 +
Mofify indiv Cent X Cent Y	vidual arc - 1.000 + - 1.000 + - 1.000 +
Mofify indiv Cent X Cent Y Radius	vidual arc - 1.000 + - 1.000 + + - 1.000 +



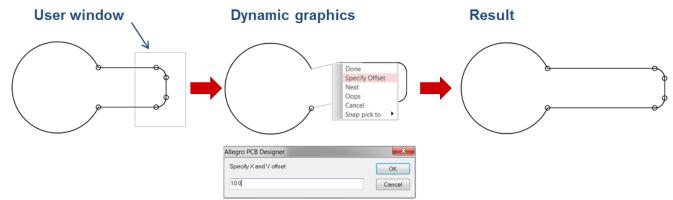
- Use model
 - 1. Select the shape or void to be modified
 - 2. Select an action, e.g. Round off vertex
 - 3. Pick a vertex or drag a window to select the vertices
 - 4. Switch to other modes if necessary and continue
 - 5. RMB > Done



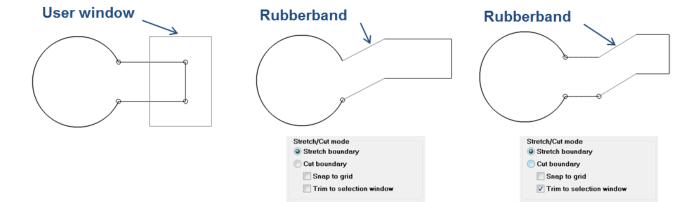




- Stretching of shapes
 - Specify offset if accurate stretch distance is needed

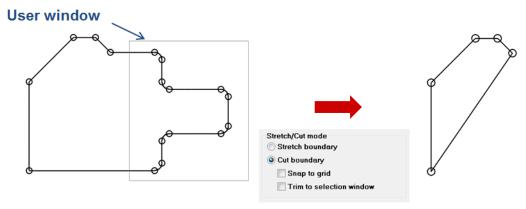


- Trim to selection window let's vou control stretch point origin

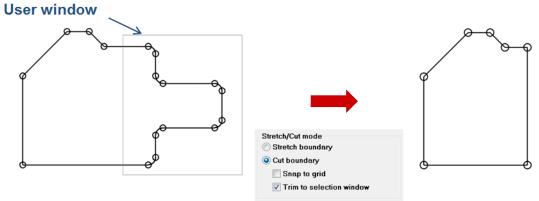




- Cutting of shapes
 - Adjacent segments of selected vertices will be deleted

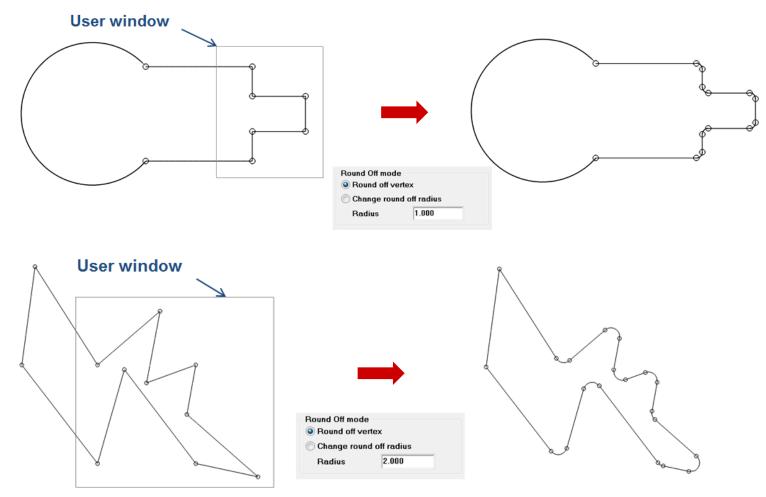


- Trim to selection window simply cuts at the window boundary



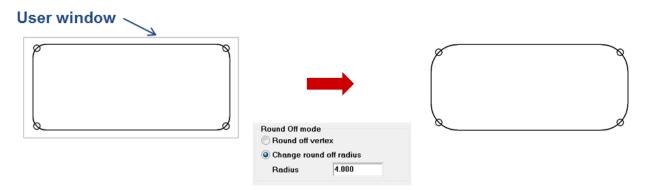


• Round off vertex

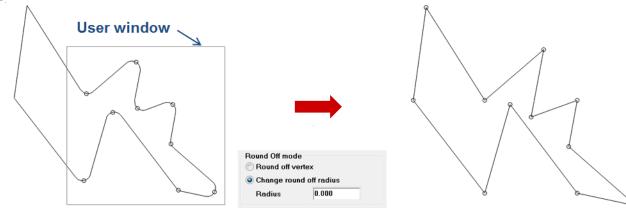




- Change round off radius
 - Let's you change existing rounded off corners

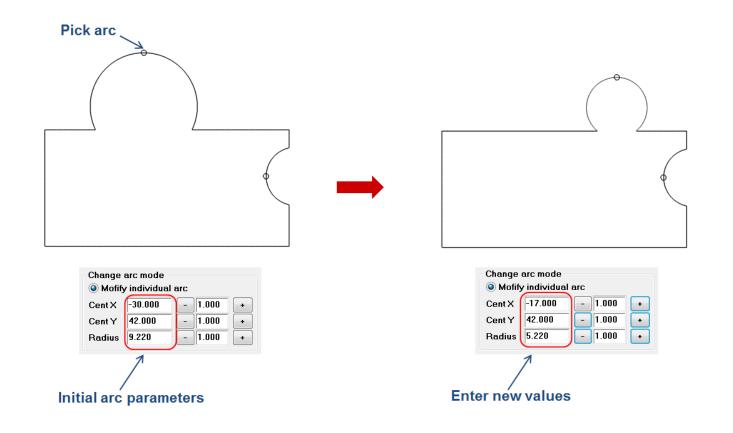


- Can also restore original vertices by specifying a radius of 0.0



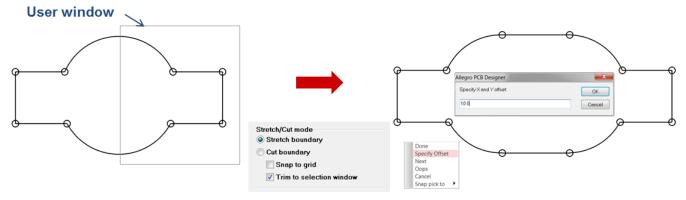


- Change arc mode
 - Parameters of existing arcs can be changed in Options panel. End points of adjacent segments will be adjusted automatically. Tuning possible by using +/- buttons

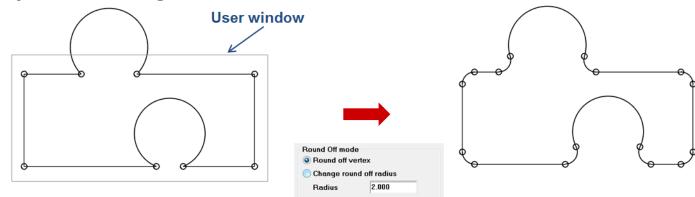




- Other highlights
 - Stretch / Cut on arc segments in conjunction with Trim option



- Round Off with adjacent arc segments





Shape Utilities – Priority

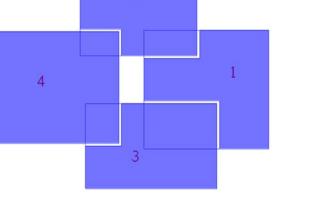
- Interactive application to modify the priority of a dynamic shape
- Use model

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- Select shapes by subsequent picks
- Choose RMB > Complete selection to enter priority edit mode
- Use one of the options and select a shape to modify the priority
 - Highest
 - Increase one level
 - Decrease one level
 - Lowest
- Priority numbers are displayed dynamically

Options
Change priority
O Highest
O Increase one level
O Decrease one level
🔘 Lowest
Display control
Text block 2
Compact view
Update dynamic shapes

Ontions



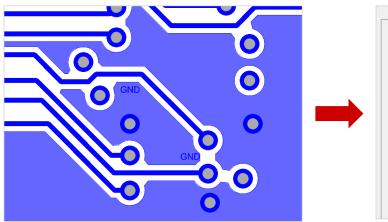


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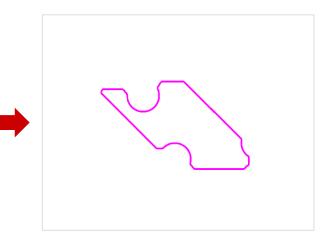
Shape Utilities – Check Status

- Utility to check and highlight island and dangling shapes
 - Islands: 0 connections
 - Dangling shapes: Only 1 connection
- Such shapes can act as antennas and cause EMI issues

Options	
Layer	
П Тор	•
Island shapes	
Island shapes	
Dangling shapes	
📃 Limit vie w	









Shield Generator

- Facilitates the generation of shape and via pattern for shielding purposes
- Includes shield rings along board outline (e.g. for ESD protection) as well as the generation of shield boxes for RF circuits

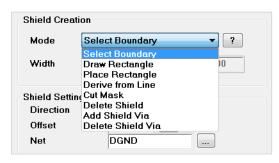
Shield Generator Shield Creation Mode Select Boundary ? Width 50.0000 Height 50.0000 Shield Settings Direction Inside ? Offset 2.5400 ? Net DGND ? Create Shapes Width 2.0000 Type Static ? Layers Specify ? Create Vias Via Gap 2.5400 ? Layers Specify ? Create Vias Via Gap 2.5400 ? Initial Offset 0.0000 ? Padstack Via0_3C0_7C
Create Mask

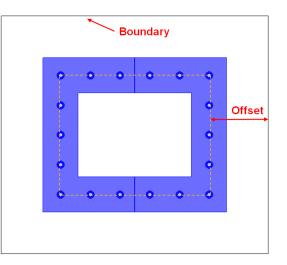


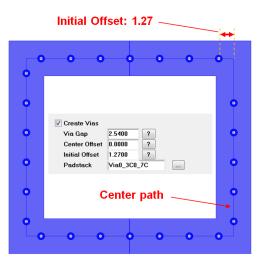
Shield Generator

- Different modes for shield generation
 - Select Boundary
 - Draw Rectangle
 - Place Rectangle
 - Derive from Line
 - ...

- Shape parameters
 - Direction, offset, width, layers, ...
- Via parameters
 - Via gap, offset inside ring, initial offset, ...
- Mask generation and cutting capabilities for solder mask and paste mask
- Ability to create groups or symbols









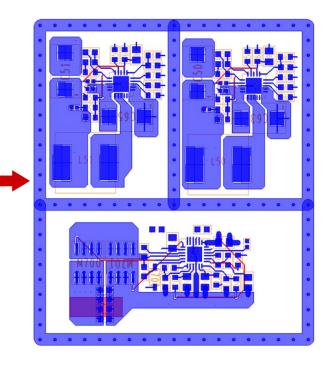
Shield Generator

• Derive from Line

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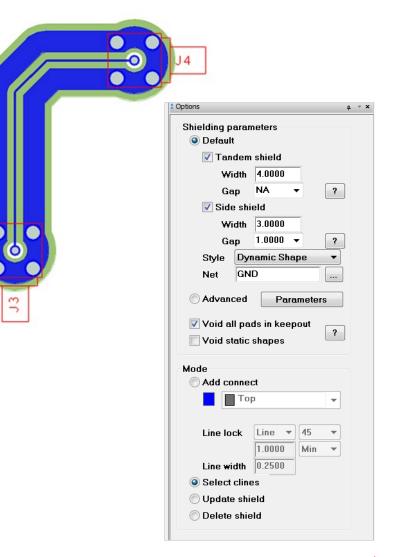
 This mode allows you to use construction lines as template and derive shield structure. Useful if shield box has partitions with arbitrary segmentations

Mode Der	ive from Line 🔹 ?
Width 50.0	000 Height 50.0000
Shield Settings	
Direction	Inside
Offset	2.5400 ?
Net	DGND
🔽 Create Shape	95
Width	2.0000
Туре	Static -
Layers	Specify
🗸 Create Vias	
Via Gap	2.5400 ?
Center Offset	0.0000 ?
Initial Offset	0.0000 ?
Padstack	Via0_3C0_7C
Create Mask	
Side	Top 🔻
Misc	_
Create Symb	
📃 Snap Grid	2.540





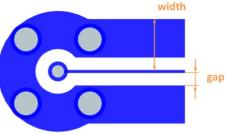
- Creates shield for critical signals in a semiautomatic way
 - Through interactive routing including dynamic preview
 - By selecting existing clines
- Support for side and tandem shields including parameters for gap and width and net name
- Support for dynamic or static shapes as well
 as route keepouts
- Advanced parameters can be used to control layers
 individually
- Parameters stored in database for each shield structure separately
 - Existing shields can be updated at any time without reentering information

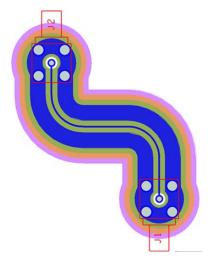




- Default shield parameters
 - For regular applications
 - Side shielding (width and gap)
 - Tandem shielding (width) on adjacent layers only
 - Shape style and net name
- Advanced parameters
 - Can be used to define parameters for several layers individually
 - Export / Import settings for reuse purposes

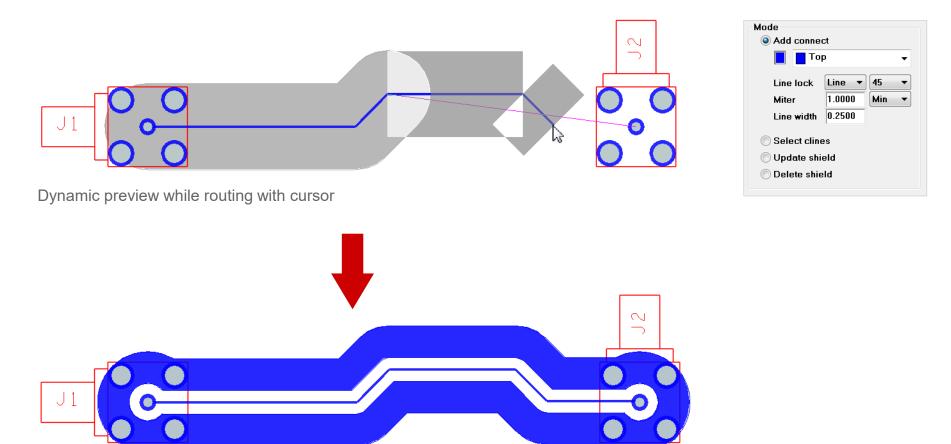
	D	ing parameters efault Tandem shield Width 5.0000 Gap NA • Side shield Width 4.0000 Gap 1.0000 • tyle Dynamic Shap et GND dvanced Param	neters							
Side shi	elding te side sh		Global Net name	GI	ND				×	
Fandem	shielding		Enable D	DR			same net		?	
	Enable	Layer	Style	DR	Wid		Gap	1		
1	Enable	Layer SOLDERMASK_TOP	Style Static Shape		Wid 2.000		Gap	- -		
	Enable	Layer	Style		Wid 2.000 2.000		Gap			
1 2 3 4	Enable	Layer SOLDERMASK_TOP TOP L2 L3	Style Static Shape Dynamic Shape	•	Wid 2.000 2.000 4.000 5.000		Gap NA NA	•		
1 2 3 4 5	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape	× × ×	Wid 2.000 2.000 4.000 5.000 6.000		Gap NA NA NA NA NA	• • •		
1 2 3 4 5 6	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L5	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape	× × ×	Wid 2.000 2.000 4.000 5.000 6.000 2.000		Gap NA NA NA NA NA NA	• • • •		
1 2 3 4 5 6 7	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L5 BOTTOM	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape	× × ×	Wid 2.000 4.000 5.000 6.000 2.000 2.000		Gap NA NA NA NA NA NA NA	• • • •		
1 2 3 4 5 6	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L5	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape	× × ×	Wid 2.000 2.000 4.000 5.000 6.000 2.000		Gap NA NA NA NA NA NA	• • • •		
1 2 3 4 5 6 7 8	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L5 BOTTOM	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape	• • • • • •	Wid 2.000 2.000 5.000 5.000 2.000 2.000 2.000 2.000 2.000		Gap NA NA NA NA NA NA NA O	· · · ·		
1 2 3 4 5 6 7 8	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L4 L4 L5 BOTTOM SOLDERMASK_BOTTO	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Natatic Shape Paran Add Ring (Del Via vi Up Initial	• • • • • • • • • • •	Wid 2.000 2.000 5.000 5.000 2.000 2.000 2.000 2.000 2.000 set set	1.000	Gap NA NA NA NA NA NA NA O	· · · ·		
1 2 3 4 5 6 7 8	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L4 L4 L5 BOTTOM SOLDERMASK_BOTTO	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Nape Static Shape Add Ring of Del Via vi Up Initial Down Via st	• • • • • • • • • • • •	Wid 2.000 2.000 5.000 2.0000 2.000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.00000 2.00000000	1.000 1.000	Gap NA NA NA NA NA NA NA O O	· · · ·	*	
1 2 3 4 5 6 7 8	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L4 L4 L5 BOTTOM SOLDERMASK_BOTTO	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Natic Shape Attic Shape Add Paran Paran Paran Paran Paran Paran Paran Add Add Jup Initial Down Via st Alignr	• • • • • • • • • • • • • • • • • • •	Wid 2.000 2.000 5.000 2.0000 2.000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.00000 2.00000000	1.000 1.000 0.000	Gap NA NA NA NA NA NA O 0 0	· · · ·	??	
1 2 3 4 5 6 7 8	Enable	Layer SOLDERMASK_TOP TOP L2 L3 L4 L4 L4 L5 BOTTOM SOLDERMASK_BOTTO	Style Static Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Dynamic Shape Nape Static Shape Add Ring of Del Via vi Up Initial Down Via st	• • • • • • • • • • • • • • • • • • •	Wid 2.000 2.000 5.000 2.0000 2.000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.0000 2.00000 2.00000000	1.000 1.000	Gap NA NA NA NA NA NA O 0 0	· · · ·	*	







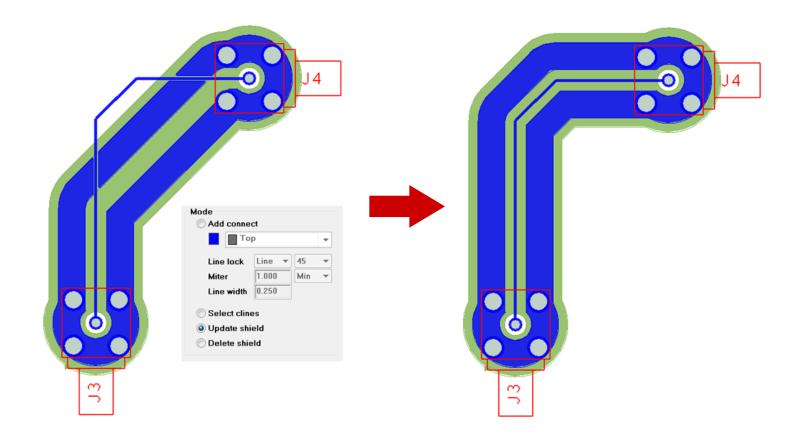
• Routing shields interactively



Final structure once snapping to pin or via



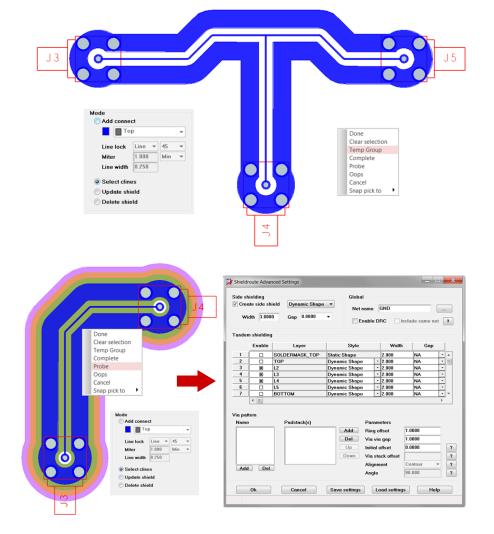
- Updating existing shield structures due to routing modifications
 - Seamless update since parameters are stored in the database for each shield structure





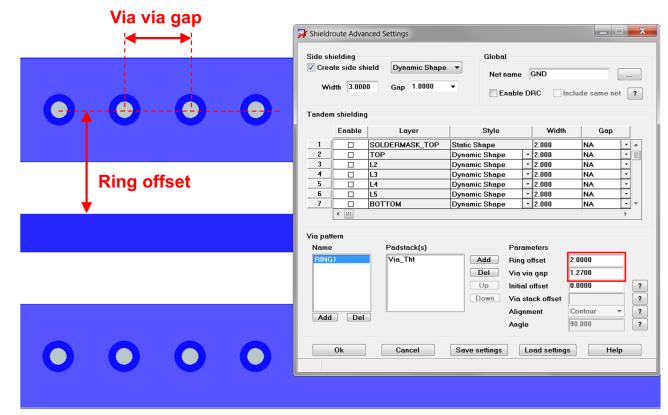
- Creating combined shields for several contiguous clines
 - Through Temp Group command

- Parameter probe
 - Simply copy parameters from one structure to another
 - Parameters will be extracted and can be applied to other clines





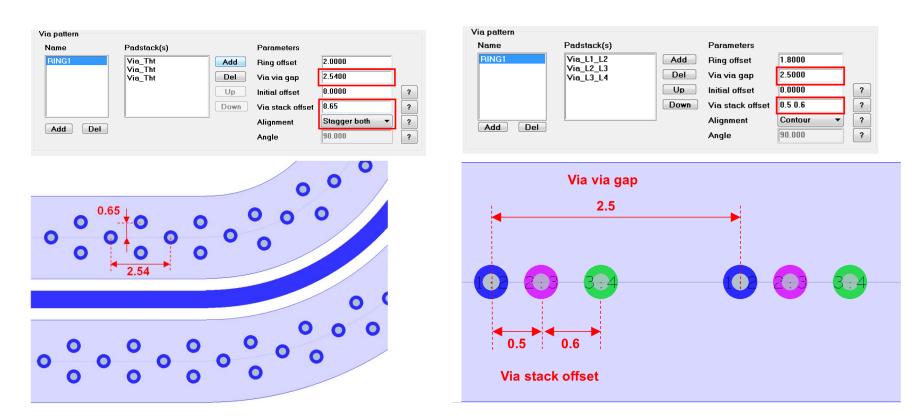
- Via pattern generation
 - Use Advanced Parameters form to specify
 - Multiple rings can be specified
 - Settings which apply to padstacks, offsets, alignment, angles, etc.





Shield Routing

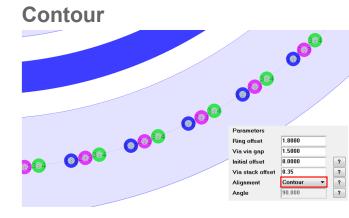
- Advanced via pattern settings
 - Multiple padstacks (e.g. microvias)
 - Parameter for main stitching gap and gaps within in the stack
 - Staggering option



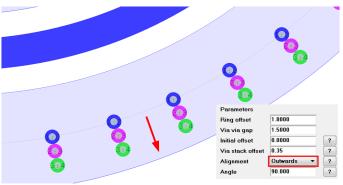


Shield Routing

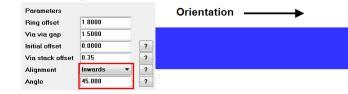
• Microvia stacking within ring

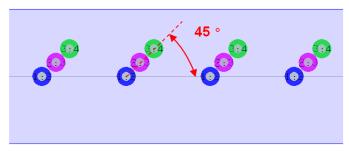


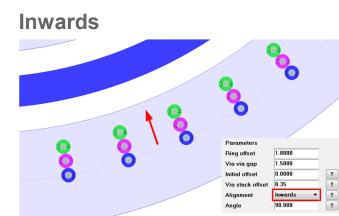




45 deg inwards









Silkscreen

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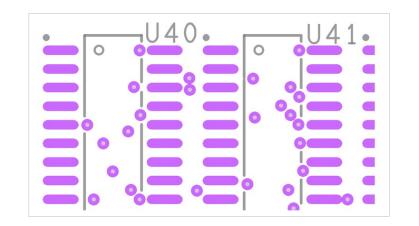
- Powerful silkscreen utility
- Configuration

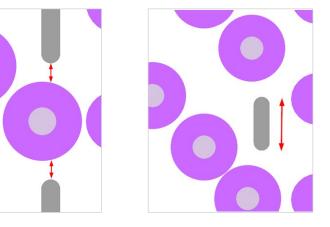
Objects to silk e.g. lines and labels can be configured as well as obstacles which require silk objects to be cut e.g. soldermask, keepout areas

Rules

Clearances and minimum segment length can be defined

<table-of-contents></table-of-contents>	
General Elements: V Text V Lines Source Specify Obstacles Specify Side Top V	ParametersMinimum line length0.25Min clearance0.10Undefined line width0.10Ignore text blocks?
Miscellaneous DRC -> Configuration -> Clear all data	Display control Global All off Limit ? Source T B Obstacle T B Drc Result T B
ОК	Run Help





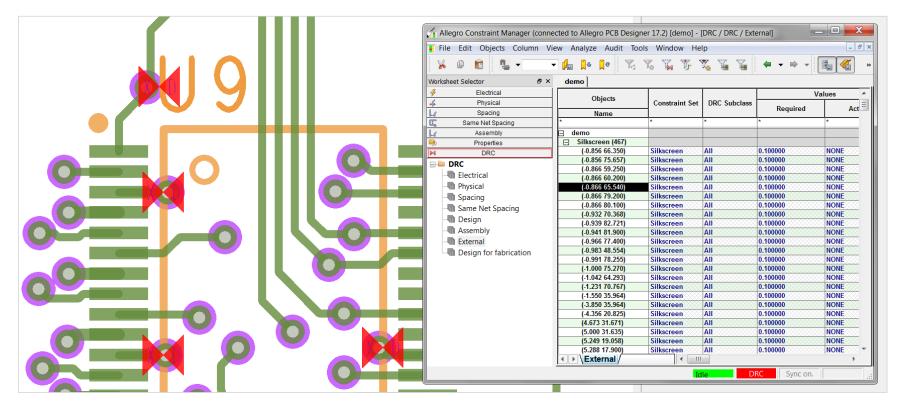


Silkscreen

• DRC

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Before generating silkscreen data, a DRC check can be performed, indicating all violations helping users to identify problems and fix them before actual data is generated





Snap Generator

- Creates snap points for standard PCB Editor commands
- Graphical entity in PCB Editor
- Snap point types

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- Intersection, extended intersection
- Endpoints, center points, origins
- Subdivision points (e.g. divide circle by 5)
- Stored in database
- Many options

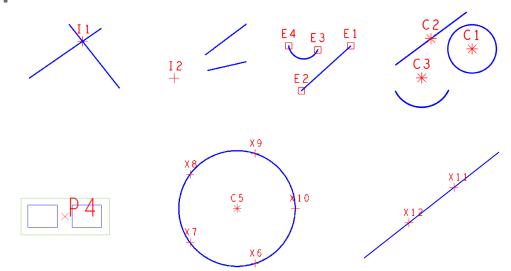
Basic	Arc	Line	Param		Snap Poir	nt List			
- Filte	r:				I E	СР	м	x	All
0	Intersect	ion (l)			· ·	v .		V	V
0		e Extend	ed Point		11 (1.27				
6	Endpoint				12 (7.62	144.78)			
	Center (.,			I3 (8.255 E1 (31.7				
					E2 (22.8	6 1 42.24	4)		
۲	Origin (F	1			E3 (36.8 E4 (43.8	15 141.0	605)		
Meth	odology				C1 (27.3 C2 (40.1				
	Incremer	ıtal			P1 (50.8	118.11))		
v	Inside Bo	ox only			P2 (46.9	9 1 1 8.1	"		
Mode				_					
	dle (PCB l	Editor)							
_	dd Snap	,							
_)elete Sna	an			XY:				Add
0		-12			AL.				Auu

Runs also when working on symbol drawings

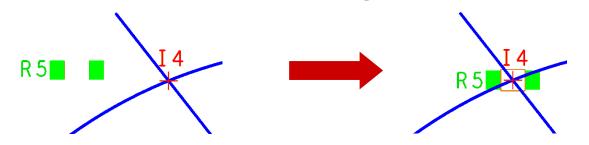


Snap Generator

Snap point types



Placing component R5 to intersection I4 using Edit > Move



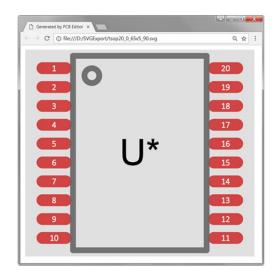
_ Snap	Poin	t Lis	t —			
- I	Е	С	Р	м	х	All
12 (13 (14 (15 (E1 E2 E3 E4 E5 C1 C2 C3 C4 M1 P1 P2	189.5 187.6 189.6 192.5 (190.2 (190.2 (190.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (189.2 (166.4 (166.4 (166.4)))))))))))))))))))))))))))))))))))	5 83. 85.4 88.3 433 7 214 7 995 6 776 6 557 6 147 7 928 7 436 8 791 8 0 88. 405 7 405 4	(45))) (0.88 (0.36) (9.83) (9.83) (9.83) (9.84) (9.84) (10.84) (11.87) (11.87) (11.87) (11.87) (11.87)	(2) (5) (8) (1) (6) (8) (2) (8) (7)		
XY:						Add



SVG Export

- Generates SVG data out of PCB Editor
- Export SVG from current drawing
- Export SVGs for a complete footprint library including HTM report generation
- Profile support
 - Content (layers) and styles (e.g. colors, opacity, non-vectorized texts, etc.) can be specified using predefined profiles

SVG Export
General
Current drawing
C Library
Generate HTML report Portable (Standalone)
Export directory
D:/SVGExport
Options
Profile Current Visibility
V Non-vectorized text Center labels
Preserve zoom level
Apply Close Help



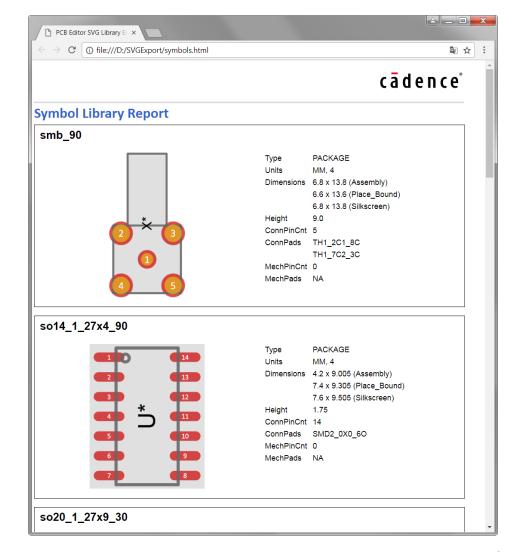


SVG Export

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• Example for HTML library report

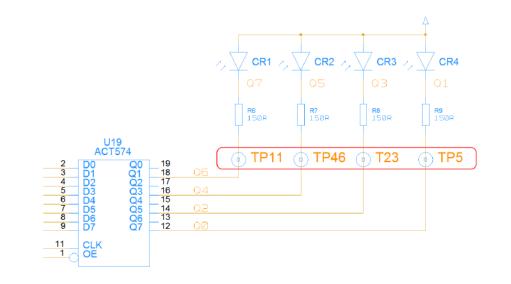
🐉 SVG Export	
General	1
Current drawing	
Library	
C:\Cadence\symbols	
🗹 Generate HTML report 🛛 🔲 Portable (Standalone)	
Export directory	
./SVGExport	
Options	
Profile symbol •	
Non-vectorized text Center labels	
Preserve zoom level	
Apply Close Help	

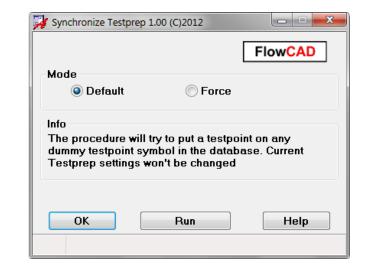


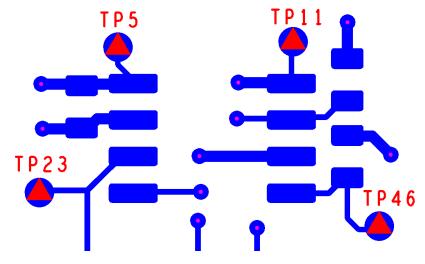


Synchronize Testprep

- Automates the testpoint assignment in PCB Editor when dummy testpoint symbols (one-pin components with Refdes TP*) have been used in the schematic
- Generates testpoint on corresponding pin in PCB
- Post processing can then be done using PCB Editor Testprep functionality







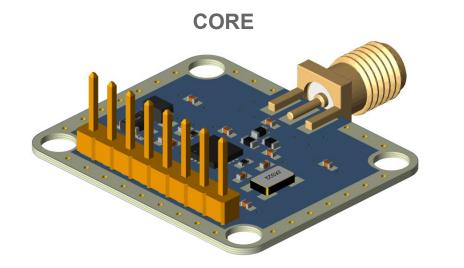


Variant 3D

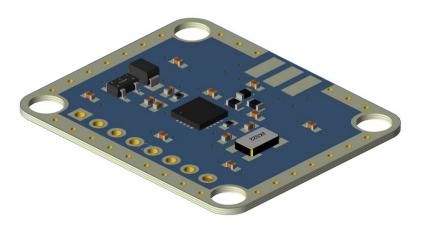
 \bigcirc

- Application that supports 3D variants
 - Based on data from variants.lst
 - Single boards
 - Regular panels
 - Multi board panels

Name	Variant	F
DESIGN	CORE 🔻	D:/Demo/Variant3D/variants.lst
	CORE	
	ALL	
	SMT_ONLY	1
	THT_ONLY	1



SMT_ONLY



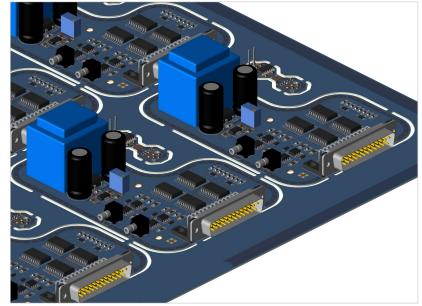


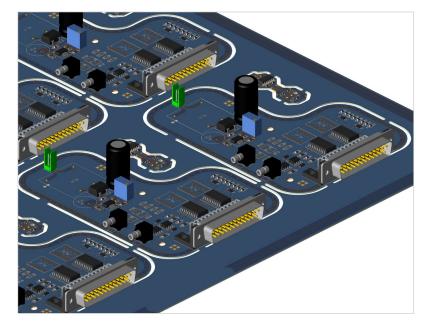
Variant 3D

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• Multi board panels

Name	Variant	Path (variants.lst)
AMPLIFIER	V2	D:/Demo/Variant3D/AMP_variants.lst
SENSOR	V3 👻	D:/Demo/Variant3D/SEN_variants.lst
	CORE V1 V2 V3	







- Gives customers even more flexibility when creating variant assembly views
- Features

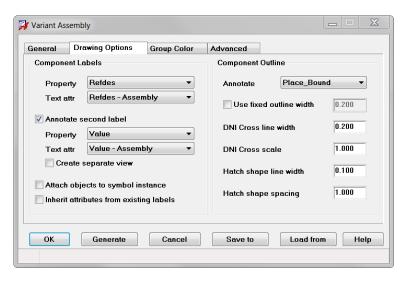
- Automatic generation of all assembly variant views in one step
- Customizable label content, e.g. Refdes, Value, Part_Number with the ability to annotate two labels per component
- Customizable component outline, e.g. Assembly, Place_Bound, Silkscreen, ...
- Customizable style for DNI components, e.g. remove all or draw a thick cross through the label, ...
- Customizable style for Alternate components by using label prefix / suffix, changing colors or hatching component outline
- Supports rule based coloring of objects, e.g. all SMT in green
- Automatic mirroring of bottom view for better readability
- Settings stored in database



User interface

General	Drawing Options	Group Color	Advanced	
Generate	e Assembly View for			
Variant	ASIA	•		
File	D:/demo/variants.	lst		Load
DNI Part	s lify Style Remove	e All 👻	Alternate Parts	Prefix Suffix
Mod	lify Color		📝 Modify Color	
√ Rem	nove second label		Modify Graphics	Hatch Shape 🔻
ОК	Generate	Cancel	Save to	Load from Hel

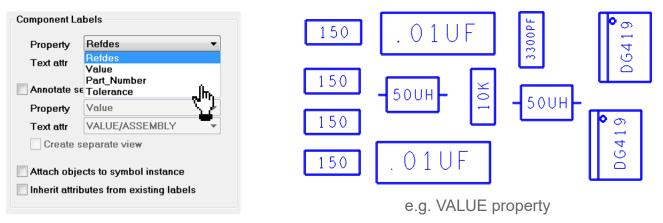
General	Drawing Options	Group Color	Advanced	
	Property	[Value	Color
	FDES DEC_TYPE	▼ U5;1	J11)3*;*0805*	···· · · · · · · · · · · · · · · · · ·
•				
	mable group color		riant color wins over grou	4



General	Drawing Options	Group	Color	Advanc	ed			
Bottom \	/iew		Addition	al layers				
Mode	Mirror to top	•	🔽 Inclue	le additio	nal laye	rs to varia	nt view	
Side	Right -		Top s	side	Sp	ecify]	
Space	10.000		Botto	m side	Sp	ecify]	
Misc			Gene	ral	Sp	ecify]	
🔽 Upda	te custom variables							
Ca	py labels to variant v	iew						
🔲 Full c	lean before update							
Write	view files (*.color)							
ок	Generate		ncel	Car	ve to		d from	He



Customizable label content to be displayed (default is Refdes)



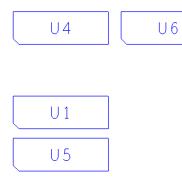
Customizable component outline to be displayed (default is Assembly)

Component Outline Annotate Assembly Assembly		
Use fixed out Place_Bound Silkscreen		
Display DNI Cross line v DFA_Bound	C64	
DNI Cross scale		⁶ U13 ⁶¹
Hatch shape line width 0.100		- <u>Г</u>
Hatch shape spacing 1.000		
	Assembly outline	Placebound outline



Available styles for DNI parts

Style "Remove All"



Style "Cross Graphics"

υ4

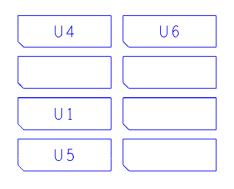
U 1

U 5

U 6

DNI Parts		
Modify Style	Remove All	-
	Remove All	
Modify Color	Remove Label	
	Cross Label	
Remove second	Cross Graphics	

Style "Remove Label"



Style "Cross Label"



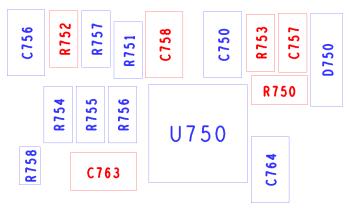


Module: Variant Assembly

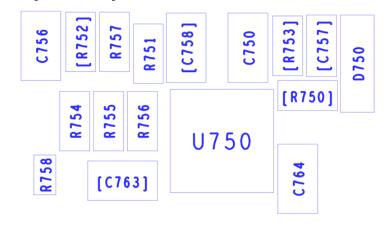
Available styles for alternate parts

Alternate Parts	Prefix [Suffix]
Modify Color	
✓ Modify Graphics	Hatch Shape 💌

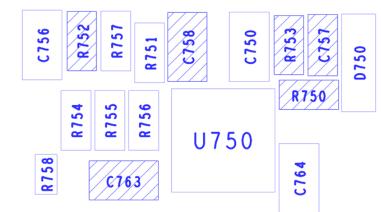
Style "Modify Colors"



Style "Modify Labels"



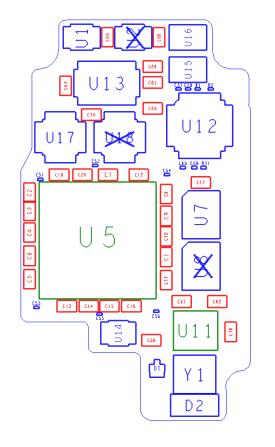
Style "Modify Graphics"





Module: Variant Assembly

Rule based coloring of components



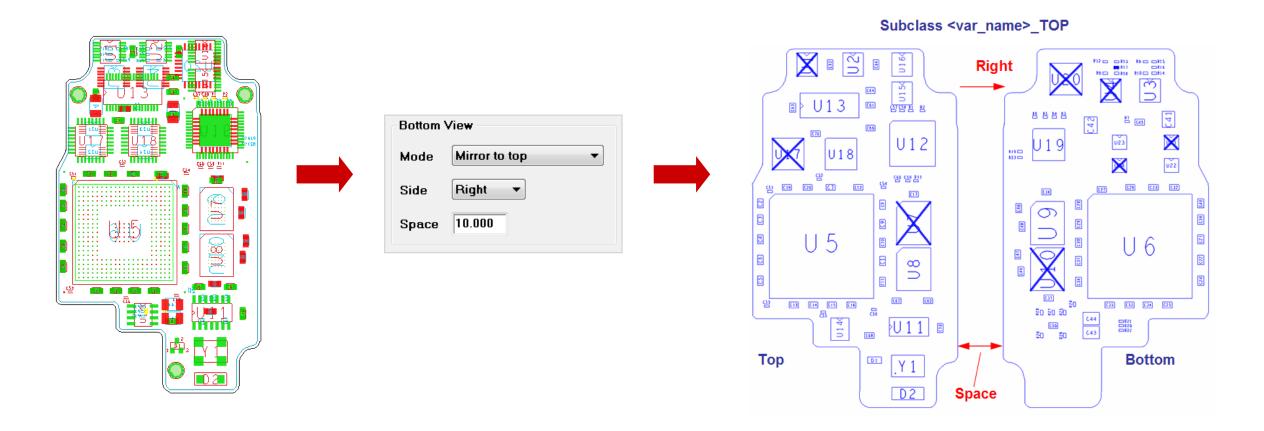
¥	Vari	iant	t Ass	embly						X
	Gene	era	-	Drawing Options	Group Color	Advanced				
				Property	[Value		Color		[
	1			DES	- U5;I					
	_2		JEDE	EC_TYPE	* 060	3*;*0805*				Ξ
										-
			• 11	I					•	•
			Z En	able group color	Va	riant color wins ove	er group color			
		ок		Generate	Cancel	Save to	Load fro	m	Н	əlp

- Color rules can be linked to individual properties
- Several match pattern per rule
- Wildcard support



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Automatic mirroring of bottom view e.g. side by side to top view





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- Creates various reports (BOM) from layout database taking variant information into account
 - Generates reports (e.g. pick & place) data for a variant
 - Can be used for reports on core design also

Configurable content

- Any database attribute
- Ability to distinguish between common and variant parts
- Exclude BOM non-relevant parts (e.g. dummy testpoints)
- Header information, order of columns, column width
- Hierarchical sorting up to three levels
- Option to split output files
- Settings stored in database, export and import capabilities
- Output format
 - HTML, ASCII, CSV

User Interface

🐉 Variant BOM						
General Part Specification Advanced						
Content	Report Format					
Variant name ASIA	Text Show Report					
Core Design Common All Variants	CSV Show Report	Variant BOM				
Output directory USA	✓ HTML ✓ Show Report	eneral Part Specification Advanced Nr Parameter Type Acc. Width Name				
Header Setup	Variant Options					
Insert external file	Report Unchanged	1 ROWNUM Integer 0 -1 POS 2 REFDES V String 0 -1 REF	🙀 Variant BOM			
✓ Insert column names	Report Alternates	3 DEVICE_TYPE				
	Report DNI	4 X Float 2 -1 SYM_X	General Part Specification Advanced			
		5 Y Float 2 -1 SYM_Y	Miscellaneous			
		6 ROTATION · Float 2 -1 ROTATION	Undef value NA Mirror Yes/No Level 1 REFDES	•		
Control Files		7 MIRROR • String 0 -1 MIRROR		Separate by newline		
Variants File D:/demo/variants.lst		8 MOUNT_TYPE v String 0 -1 MOUNTING 9 VARTYPE v String 0 -1 VTYPE	Decimal point dot 🔻 Units mm 🔻			
		9 VARTYPE String 0 -1 VTYPE	Split output file	es		
External Header			Text report			
			Extension bom Column separator	-		
		• [1]	Separate by n	ewline		
OK Generate Cancel	Save to Load from		CSV report Split output file	es		
		✓ Exclude parts by BOM_IGNORE ▼ Value TP*	Level 3 (No Sort)	-		
			Transformation Component location			
		OK Generate Cancel Save to Load from	He Runs transformation rules Quit Sumbal arigin			
			Vse transformation rules Specify O Symbol origin			
			JEDEC_TYPE rotation offset ? Symbol center			
			OK Generate Cancel Save to Load from	Help		

Report Formats



0 Y805 88.01 121.03 90.00 NO SHT BASE 0 Y805 88.01 117.48 90.00 NO SHT BASE 0 Y805 88.01 117.48 90.00 NO SHT BASE 0 Y805 88.01 113.16 90.00 NO SHT BASE 0 Y805 88.01 104.01 90.00 NO SHT BASE 0 Y805 88.01 104.01 90.00 NO SHT BASE 0 Y805 88.01 104.58 90.00 NO SHT BASE 0 Y805 103.51 124.59 0.00 NO SHT BASE			000					
POS: REF: DEVICE: SYM_X: SYM_Y: ROTATION: MIRROR: MOUNTING: YTYPE 1: C1: C2: CAP_B0S-120PFS50V805: 88.01 1: C1: C2: CAP_B0S-120PFS50V805: 88.01 1: C1: C2: CAP_B0S-120PFS50V805: 88.01 1: C1: C3: CAP_B0S-120PFS50V805: 88.01 1: C3: C3: CAP_B0			File: D:/flow	are_demo/varian	it_assembly_b	oom,	/worklib/root/physical/master.csv	
1:C1:CAP_805-120PF550Y805:88.01:121.08.33;90.00;NO;SMT;BASE 2:C2:C2:PB05-120PF550Y805:88.01:117.48;90.00;NO;SMT;BASE 3:C3:CAP_805-120PF550Y805:88.01:117.48;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:113.16;00.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:114.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:114.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:114.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:104.01;90.00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:00;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:100;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:100;NO;SMT;BASE 5:C5:CAP_805-120PF550Y805:88.01:100;NO;SMT;BASE 5:C5:CAP_805-110;NO;ND;ND;ND;ND;ND;ND;ND;ND;ND;ND;ND;ND;ND;			File Close	Help				
	SUV805 SU	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	1:C1:CAP_8 2:C2:CAP_8 3:C3:CAP_8 4:C4:CAP_8 5:C5:CAP_8 6:C6:CAP_8 70:00 70:00 NO 0:00 NO 0:00 NO 0:00 NO 0:00 NO 0:00 NO 0:00 NO 0:	05-120PF55 05-120PF55	07805;114 07805;184 07805;88 0	1.9 01 01 01 01 01	4;108,33;90,00;N0;SHT;BASE ;121,03;90,00;N0;SHT;BASE ;117,48;90,00;N0;SHT;BASE ;113,16;90,00;N0;SHT;BASE ;114,01;90,00;N0;SHT;BASE ;114,01;90,00;N0;SHT;BASE ;124,59;0,00;N0;SHT;BASE ;120,78;90,00;N0;SHT;BASE ;116,46;90,00;N0;SHT;BASE 94;112,40;90,00;N0;SHT;BASE 94;112,40;90,00;N0;SHT;BASE 94;112,40;90,00;N0;SHT;BASE 18;98,68;0,00;N0;SHT;BASE 10;98,68;0,00;N0;SHT;BASE 10;98,68;0,00;N0;SHT;BASE 10;98,68;0,00;N0;SHT;BASE 08;98,68;0,00;N0;SHT;BASE 15;124,59;0,00;N0;SHT;BASE 15;124,59;0,00;N0;SHT;BASE 15;124,59;0,00;N0;SHT;BASE 16;98,68;0,00;N0;SHT;BASE 16;98,68;0,00;N0;SHT;BASE 15;124,59;0,00;N0;SHT;BASE 15;124,59;0,00;N0;SHT;BASE 12;124,59;0,00;N0;SHT;BASE 12;124,59;0,00;N0;SHT;BASE 12;124,59;180,00;YES;SHT;BASE 11;108,58;180,00;YES;SHT;BASE 11;108,58;180,00;YES;SHT;BASE 11;104,01;270,00;YES;SHT;BASE 11;124,59;180,00;YES;SHT;BASE 11;124,59;180,00;YES;SHT;BASE 11;124,59;180,00;YES;SHT;BASE 11;124,59;180,00;YES;SHT;BASE 11;124,59;180,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;116,46;270,00;YES;SHT;BASE 14;1124,59;1180,00;YES;SHT;BASE 14;1124,59;1180,00;YES;SHT;BASE	

							File (Close Help		
								+++++++++++ REF DEVI		+++++++++++++++++++++++++++++++++++++++
								+++++++++++++++++++++++++++++++++++++++	+++++++	
							2	C2 CAP	805-120)PF550V805)PF550V805
							3 4		805-120)PF5507805)PF5507805
HTML	_						5)PF550V805)PF550V805
							7	C7 CAP	805-120	PF550¥805
		-	iant_assembly_bom/worklib/root/pl	hysical/mas	ter.html					
-¤ 🗙 [] 🖨 ?	Sea	arch: 📃 N	/latch word	Mat	ch case				
	POS	RFF	DEVICE	SYM X	SYM Y	ROTATION	MIRROR	MOUNTING	VTYPE	
	1	C1	CAP 805-120PF550V805	114.94	108.33		NO	SMT	BASE	
	2	C2	CAP 805-120PF550V805	88.01	121.03		NO	SMT	BASE	
	3	C2	CAP 805-120PF550V805	88.01	117.48		NO	SMT	BASE	
			_							
	4	C4	CAP_805-120PF550V805	88.01	113.16		NO	SMT	BASE	
	5	C5	CAP_805-120PF550V805	88.01	104.01		NO	SMT	BASE	
	6	C6	CAP_805-120PF550V805	88.01	108.58	90.00	NO	SMT	BASE	
	7	C7	CAP_805-120PF550V805	103.51	124.59	0.00	NO	SMT	BASE	
	8	C8	CAP_805-120PF550V805	114.94	120.78	90.00	NO	SMT	BASE	
	9	C9	CAP_805-120PF550V805	114.94	116.46	90.00	NO	SMT	BASE	
	10	C10	CAP_805-120PF550V805	114.94	112.40	90.00	NO	SMT	BASE	
	11	C11	CAP_805-120PF550V805	114.94	103.76	90.00	NO	SMT	BASE	
	12	C12	CAP_805-120PF550V805	109.58	124.56	0.00	NO	SMT	BASE	
	13	C13	CAP_805-120PF550V805	95.38	98.68	0.00	NO	SMT	BASE	
	14	C14	CAP_805-120PF550V805	99.70	98.68	0.00	NO	SMT	BASE	
	15	C15	CAP_805-120PF550V805	103.76	98.68	0.00	NO	SMT	BASE	
	16	C16	CAP_805-120PF550V805	108.08	98.68	0.00	NO	SMT	BASE	

Text

File Close Help

File: D:/floware_demo/variant_assembly



- Hierarchical sorting
 - Up to three levels
 - Options to add newline for level 1 and level 2
 - Options to split output files for level 1 and level 2

Sort Orde	r
Level 1	VARTYPE 🔻
	📝 Separate by newline
	Split output files
Level 2	MIRROR -
	Separate by newline
	Split output files
Level 3	REFDES -

6	VA	RI_4.bom	(D:\vari_	demo	(mfg) - GVI	м												3
Da	ate	i Editier	en W	erkze	uge Syn	tax P	uffer /	Ansicht	Hi	lfe								
91		9 8 9	C X	0 🛍	🗟 원 🔁	🕹 📥	â T (l 💷	2									
+++•	+++	++++++++	++++++	++++	++++++++	+++++	******	******	+++	+++++	+++	++++	++++4	+++	++++++++	+++	++++++	1
POS	I	REFDES	DEVIC	Έ			1	UTYPE	Т	MIRROR		х		L	Y	I	ROT	
+++•	+++	*******	+++++	+++++	*******	+++++	******	++++++	+++	+++++	+++	++++	++++	+++	*******	+++	++++++	
1	Т	C1	CAPAC	ITOR.	_EL-10UF,	20%,10	6,4MM	BASE	Т	NO	I.	-127	. 000	Т	317.500	I	0.000	
2	Т	C2	CAPAC	ITOR.	_EL-10UF,	20%,10	6,4MM	BASE	Т	NO	Т	-119	. 380	L	317.500	I	0.000	
3	L	C3	CAPAC	ITOR.	_EL-10UF,	20%,10	6,4MM	BASE	Т	NO 🥄 👘	Т	-111	. 760	Т	317.500	I	0.000	
4	Т	UR3	MBZ52	232B_5	SOT23-BAS	E	1	BASE	1	NO	Т	-101	. 600	Т	317.500	L	0.000	
5	Т	UR1	MBZ52	232B_	SOT23-BAS	E	- 🗡 I	BASE	L	YES		-101	. 600	Т	325.120	L	0.000	
6	Т	UR2	MBZ52	232B_5	SOT23-BAS	E	/ 1	BASE	Т	YES 💌	X	-101	. 600	Т	309.880	I	0.000	
7	L	UR4	MBZ52	232B_5	SOT23-BAS	E	(I	BASE	L	YES	$\langle 1 \rangle$	-101	. 600	Т	335.280	L	0.000	
		····· (3)			- (1)				(2	2)						L
8	Т	R1	RESIS	TOR-2	22,1/2W,5	%		CHANGE	Т	NO			. 220	Т	307.340	I	0.000	
9	Т	R4 /	RESIS	TOR-S	56,1/2W,5	%	\ ^ I	CHANGE	Т	NO	1	-109	. 220	Т	299.720	I	0.000	
10	Т	R6 /	RESIS	TOR-1	110,1/2W,	5%	\ 1	CHANGE	L	NO	1	-101	. 600	Т	302.260	L	0.000	
11	Т	R2	RESIS	TOR-	33,1/2W,5	%	_\ I	CHANGE	1	YES	1	-109	. 220	Т	335.280	L	0.000	
12	Т	R3	RESIS	TOR-4	47,1/20,5	%	_ \ _ I	CHANGE	L	YES	Т	-109	. 220	L	325.120	I	0.000	
13	Т	R5	RESIS	TOR-6	68,1/2W,5	%	_ \ I	CHANGE	Т	YES	1	-111	. 760	Т	330.200	L	0.000	
14	Т	Q1	MBT22	22A_	SOT223H-E	ASE	- 1	DNI	L	NO	I.	-121	. 920	L	302.895	I	0.000	
15	Т	J1	JACK_	4_TY	PE1-4PIN		1	DNI	1	YES	1	-122	. 492	L	336.804	I	0.000	
			-	_														1
_															21,0-1		Alles	



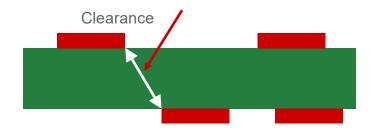
- Transformation rules
 - Sometimes users need to transform x, y and rotation due to Pick & Place requirements from manufactory
 - E.g. always subtract 360 from angles given by PCB Editor for components on BOTTOM side
 - Formulas can be specified for TOP and BOTTOM separately
 - Unit specifiers such as MM, MILS etc. are supported

	-Footprint location	DN						
	XY at 🧕 Syn	nbolorigin 🔘	Symbol center					
	🔽 Transform 3	X,Y,angle	Specify					
🥻 Varia	nt BOM			x				
Top s	ide	Botto	m side					
X =	×	X =	(100 MM) - x					
Y =	У	Y =	У					
Rot	= rot	Rot	= 360 - rot					
			e of 360 for angles equal or	r				
greater than 360 degrees Note: You may also use unit specifiers in your formulas, possible values are um, mm, mil, inch and cm.								
	Close	Cancel	Help					



Z-DRC

- Checks clearances along the Z-axis
- Useful for applications which have to meet safety and explosion requirements
- Objects to be checked can be specified on net or netclass basis in any combination
- Spacing value can be specified manually or derived from DRC system (Constraint Manager)
- Graphical DRC: Markers & Overlapping
- Cross probing and filter capabilities



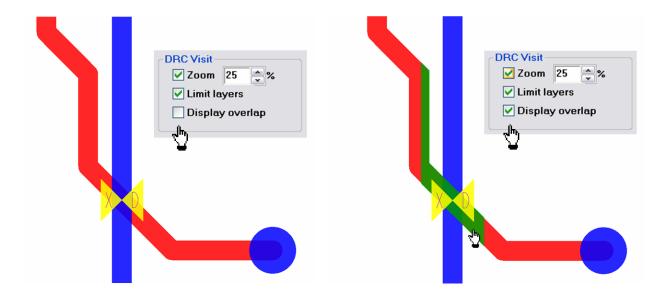
ZDRC		
Main Output Spacing value DRC system Fix 13.000 Layer distance calculation Include all Cu layers Exclude external Cu Exclude all Cu	Group A [Class/Nets] ALL CLASS ANALOG_SPACE CLS1 CLS2 NO_TYPE	Group B [Class/Nets] ALL CLASS ANALOG_SPACE CLS1 CLS2 NO_TYPE
All dielectric thicknesses within current ZDRC layer pair plus Cu thicknesses from layers **between** the current ZDRC layer pair OK ZDRC	Limit selection to: Start TOP End BOTTOM Clear All	Limit selection to: Start TOP - End BOTTOM - Help



Z-DRC

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• The negative margins (amount of overlapping) can be displayed once a DRC has been selected in the Output tab



🐉 ZDRC			
Main Output			
DRC List			
2 (5339.376 2) 3 (5338.876 2) 4 (5338.876 2) 5 (5851.501 3) 6 (5944.0 3)	700.0) N12V ↔ P2 700.0) N12V ↔ P2 700.0) N12V ↔ P2 I 32.001) N12V ↔ I 3.6) N12V ↔ P24V	P24V S1 ↔ IS2 L-L req: 1 4V VCC ↔ IS2 L-V req: 13 4V VCC ↔ IS2 L-V req: 13 4V IS1 ↔ IS2 L-V req: 13 P24V IS2 ↔ IS1 L-L req: 13.000 2V BOTTOM ↔ VCC L-P 1	req: 13.000000 3.000000 000000 3.000000 3.000000 0000
DRC Filter Layer: ALL Type: ALL Net: *		DRC Visit V Zoom 25 2% Limit layers V Display overlap	Reports DRC Errors Layer distances
ОК	ZDRC Up	date -> Clear A	NI Help



FloWare Modules Schematic Entry

OrCAD Capture / Allegro Design Entry CIS



FloWare Modules Schematic Entry

- Flat Net Utilities
- Smart Aliases
- Split Wire

- <u>Testpoint Check</u>
- <u>Tortoise SVN Integration</u>
- Update Titleblock



- TCL applications with features to report and display the complete physical net (flat net) over all pages
- Very useful for review purposes when working with hierarchical designs
- Fully integrated into standard operations (e.g. select)
- Features

- Report the physical net name in the command window while selecting wires in the canvas
- Display the physical net name in tooltip
- RMB > Highlight / De-highlight physical net over the full hierarchy



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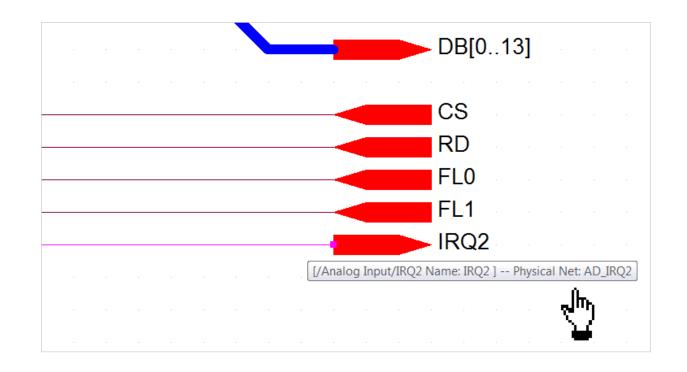
Physical net name report





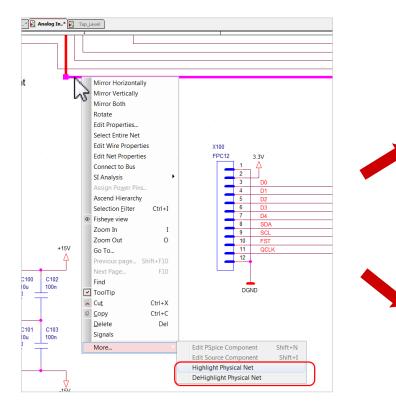
 \bigcirc

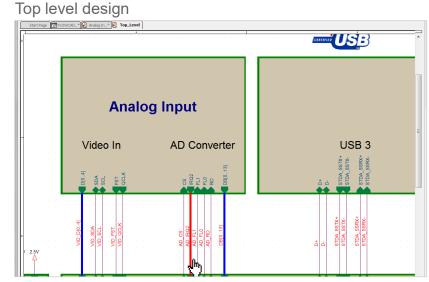
Tooltip reporting physical net name



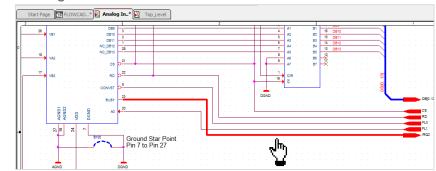


• Highlight / De-highlight physical net on all pages / hierarchies





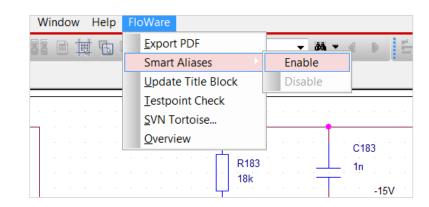
Analog subblock





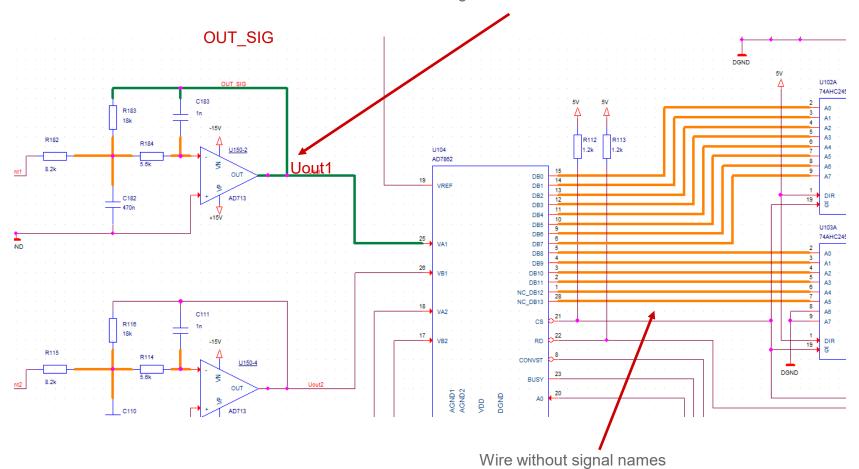
- TCL application with smart editing and highlight capabilities when working with user defined signal names (aliases)
- Features

- Dynamic highlighting of unnamed wires
- Dynamic highlighting of wires with multiple different signal names
- Smart rename when editing a signal name





• Dynamic Highlight

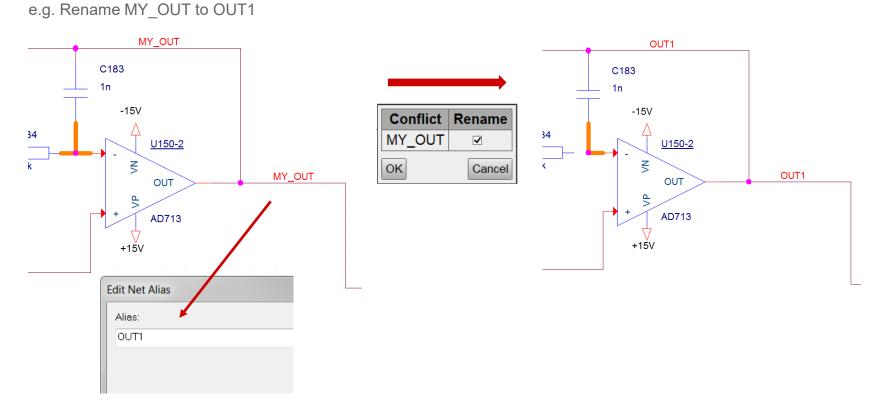


Different signal names on same "wire"



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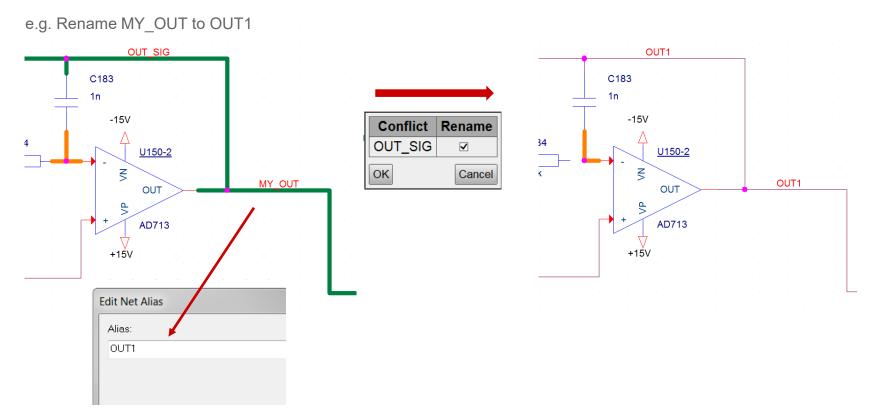
Smart Rename: Keeps signal names in sync even if signal names have been assigned at multiple locations





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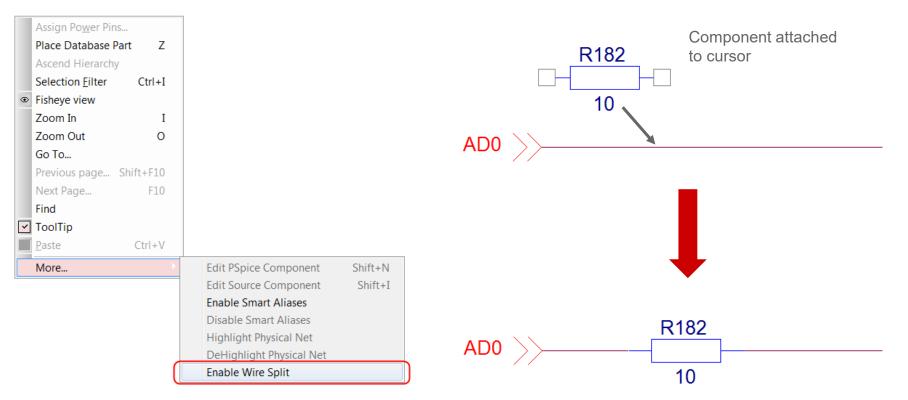
• Smart Rename: Even helps resolving conflicts when different signals names were present





Split Wire

- Provides automatic wire split when components (e.g. resistors) are placed / dropped on wires
- Enable / Disable through context menu



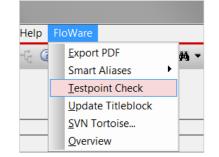


Testpoint Check

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- Check testpoint coverage for whole design
- Based on user-defined testpoint components (e.g. One-pin components TP*)
- Configurable search criteria
 - Reference = TP*
 - Value = Testpoint
- Status report

Datei Editieren Werkzeuge Syntax Puffer Ansicht Hilfe		
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flw_tpcheck.txt - Edit			_ O X
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	Check Report		[
Design: FL	DWCAD_CIS.DSN		
Date: Ap	cil 02 10:51:56 20	15	
Testpoint i	dentifier:		
Propert	Reference	Value: TP*	
Untested ne +15V -15V 0.75VRE 0.75VTT 0.9VREF 0.9VTT			
	TP10 TP23	45	



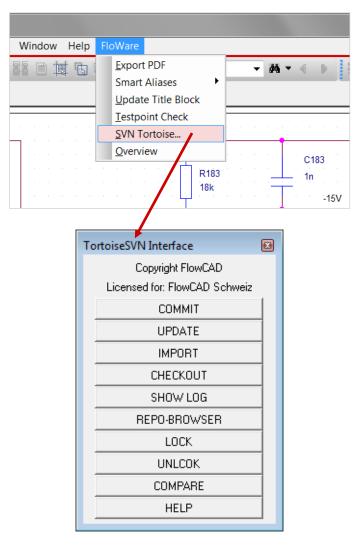
Features

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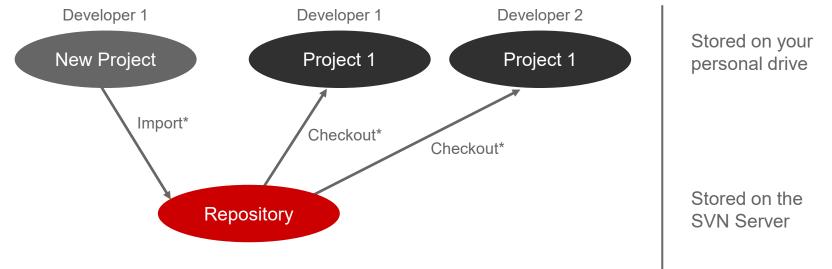
- Import a project to a SVN directory
- Committing your project to the server
- Load the latest project version from the server
- View the log-file
- Checkout a directory
- Lock / unlock a project
- Compare only with CIS license
- Each command is directly available in Capture
- This module always use your entire project directory

Prerequisites

- Tortoise SVN (Open Source)
- SVN Server (Open Source)



Use model: Creating a new project

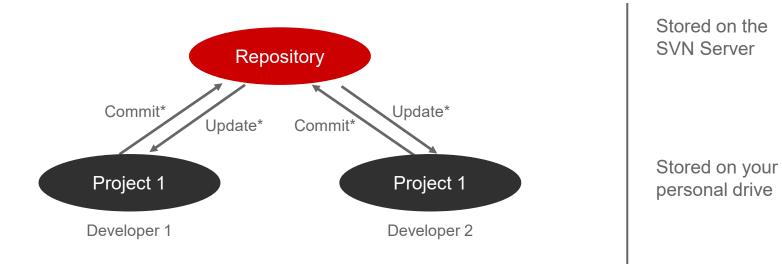


* Commands launched from the Capture TortoiseSVN interface



Use model: During the daily use

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* Commands launched from the Capture TortoiseSVN interface

FlowCAD Confidential 186



• When committing a project, you can add messages which will be stored on your server, for example:

oiseSVN Interface		Commit - C:\demo
Copyright FlowCAD		Commit to:
Licensed for: FlowCAD Schwei:	iz	https://flowcad-gyspbft:8443/svn/Sandbox/DemoMonday Message:
сомміт —		Recent messages
UPDATE		
IMPORT		
СНЕСКОИТ		
SHOW LOG		
REPO-BROWSER	_	Changes made (double-click on file for diff):
	_	Path Extension Text status Property status Lock
REPO-BROWSER LOCK		
REPO-BROWSER LOCK UNLCOK		Path Extension Text status Property status Lock Image: DEMO1.DSN .DSN modified normal Image: Demositive status I
REPO-BROWSER LOCK UNLCOK COMPARE		Path Extension Text status Property status Lock Image: DEMO1.DSN .DSN modified normal Image: DEMO1.opj .opj modified normal Image: DEMO1_0.DBK .DBK modified normal
REPO-BROWSER LOCK UNLCOK		Path Extension Text status Property status Lock Image: DEMO1.DSN .DSN modified normal Image: DEMO1.opj .opj modified normal Image: DEMO1_0.DBK .DBK modified normal Image: DEMO1_0.DBK .DBK modified normal Image: DemO1_0.DBK .DBK modified normal



• View the log messages on your project history

Log Messages - TESTCDNLIVE.DSN		<u>_ </u>	
From: 06.05.2011 💌 To: 06.05.2011 💌 🔎	Messages, authors an	d paths	3
Revision Actions Author Date	Message		
57 Marco 13:47:58, Freitag, 6. Mai 2011 54 Marco 13:45:27, Freitag, 6. Mai 2011 53 Marco 13:36:47, Freitag, 6. Mai 2011	Modified C3! Added R3!		TortoiseSVN Interface
52 👸 Marco 13:34:45, Freitag, 6. Mai 2011 51 📮 Marco 13:30:42, Freitag, 6. Mai 2011			Copyright FlowCAD
	For complete history deselect 'Stop on copy/rename'		Licensed for: FlowCAD Schweiz
			COMMIT
Modified C3!			UPDATE
			IMPORT
			CHECKOUT
Action Path Copy from path Revisi			SHOW LOG
Modified /CDNLIVE/TESTCDNLIVE.DSN Modified /CDNLIVE/TESTCDNLIVE.opj			REPO-BROWSER
Modified /CDNLIVE/TESTCDNLIVE_0.DBK			LOCK
			UNLCOK
5howing 5 revision(s), from revision 51 to revision 57 - 1 revision(s) select ✓ Hide unrelated changed paths	ed.	Statistics	COMPARE
Stop on copy/rename			HELP
Include merged revisions		Help	



• Design Compare:

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The latest version from the SVN Server will be compared with your local version

å ·C B			
bject	Object Type/Value	Object	Object Type/Value
Objects from E:/TEMP/TESTDIFF/PROJECT1	DSN	Objects from E:/TEMP/TESTDIFF/Diff/PROJECTI	DSN
E:\TEMP\TESTDIFF\PROJECT1.DSN	Design View	E:\TEMP\TESTDIFF\DIFF\PROJECT1.DSN	Design View
SCHEMATIC1	SCHEMATIC_VIEW	SCHEMATIC1	SCHEMATIC_VIEW
PAGE1	SCHMATIC_PAGE	PAGE1	SCHMATIC_PAGE
TitleBlock	Schematic_Title_Block	TitleBlock	Schematic_Title_Block
⊳ <mark>U1</mark>	COMP_INSTANCE	⊳ <mark>U1</mark>	COMP_INSTANCE
⇒ <mark>U2</mark>	COMP_INSTANCE	▷ U2	COMP_INSTANCE
Þ U?	COMP_INSTANCE	NOT_PRESENT	
[U?]			

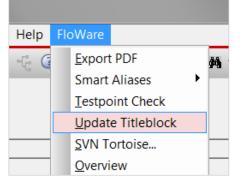
• This command works only when you have a CIS license



Update Titleblock

- Automatic update of titleblock properties
- Driven by external configuration file customvar.cfg
- Variant aware

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🥵 customvar.cfg + (D:I_Kit\project) - GVIM1	
Datei Editieren Werkzeuge Syntax Puffer Ansicht Hilfe	
금 🖬 🛱 볼 9 6 X 🖻 🎕 🍇 운 운 📥 📥 ጲ 7 🏟 💶 ? 🎗	
[Customvar BASE]	
Title=FlowCAD Evaluation Kit BASE	
Doc=\$30861-Q4711-X-2	
RevCode=1.9	
[Customvar ASIA]	
Title=FlowCAD Evaluation Kit ASIA	Variant Nama - USA
Doc=\$30861-Q4812-X-3	Variant Name = USA
RevCode=B.4	
[Customvar EUROPE] Title=FlowCAD Evaluation Kit Europe Doc=\$30861-Q4913-X-4	FlowCAD FlowCAD München - Zürich - Gdansk www.FlowCAD.eu
RevCode=1.5	www.newoAb.ed
[Customvar USA] Title=FlowCAD Evaluation Kit USA	Title FlowCAD Evaluation Kit USA
Doc=\$30861-05014-X-r5	Size Document Number Rev
RevCode=3.1	A3 S30861-Q5014-X-r5 3.1
20,0-1 Anfang	Date: Tuesday, March 31, 2015 Sheet 1 of 19



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Please do not hesitate to contact us. Für weitere Fragen und Informationen stehen wir gerne zur Verfügung.

FlowCAD Deutschland

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Mozartstr. 2 85622 Feldkirchen bei München T +49 89 45637-770 info@FlowCAD.de



FlowCAD Schweiz

Hintermättlistr. 1 5506 Mägenwil T +41 56 485 91 91 info@FlowCAD.ch



FlowCAD Polska

ul. Sąsiedzka 2A 80-298 Gdańsk T +48 58 727 90 90 info@FlowCAD.pl





International Contacts (1/2)

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For Nordic Region contact Nordcad Systems A/S

– Denmark:	support@nordcad.dk	Phone: +45 96 31 56 99
 Norway: 	support@nordcad.no	Phone: +47 21 55 28 28
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• For Benelux contact CB Distribution BV

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- For Spain and Portugal contact CB Distribution Southern Europe SL
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 - Support: <u>support@cb-distribution.es</u>

Phone: +34 91 0024576

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International Contacts (2/2)

- For France contact Artedas France
 - Pricing and info: info@artedas.fr
 Phone: +33 170916720
 - Support: techsup@artedas.fr

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- For United Kingdom contact Parallel Systems
 - Pricing information, demo keys:
 - E-mail: sales@parallel-systems.co.uk
 E-mail: info@parallel-systems.co.uk
 Technical issues:
 E-mail: support@parallel-systems.co.uk
 Phone: +44 1344 203244
 Phone: +44 1344 203244
- For North America contact EMA
 - Pricing and info: info@ema-eda.com
 - Support: techsupport@ema-eda.com

Phone: +1 800 813 7494 Phone: +1 585 334 6001

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