SPECCTRAQUEST SI EXPERT
HIGH-SPEED SYSTEM LEVEL DESIGN AND ANALYSIS

SPECCTRAQuest SI Expert is an integrated design and analysis environment for electrical engineers creating high-speed digital PC boards and systems. It allows designers to explore and resolve electrical performance-related issues in all stages of the design cycle. By exploring and making trade-offs between timing, signal integrity, crosstalk, power delivery, and EMI — designers are able to optimize electrical performance and reliability before committing to the design for manufacture. SPECCTRAQuest analyses can be performed at the board, multi-board, and/or system level — across multiple system design configurations.

ISSUES IN HIGH-SPEED DESIGN
High-speed system designers must contend with the simultaneous issues of timing analysis, signal integrity, crosstalk, power delivery, and EMI. While these issues are often addressed separately using different analysis tools, modern high-performance designs require these issues be addressed both collectively and continuously throughout the design process. As design rules are created and subsequently refined, they must be imprinted into the design database to drive the PCB design process. Changes made to the design to optimize signal integrity will have an impact on system timing and radiated EMI.

A design process that optimizes any high-speed design characteristic without assessing its impact on other high-speed issues can only prolong the design cycle and increase the chance of error. By allowing designers to analyze and address all high-speed design issues concurrently, SPECCTRAQuest™ SI Expert reduces both the time and risk required to bring a new high-speed system to market.

With shrinking timing margins, users need to be able to consider the effects of package design on the overall performance of the signal on the PCB system that can include several PC boards in a multi-board system. SPECCTRAQuest SI Expert supports the entire high-speed design flow from pre-layout exploration of design parameters such as differential impedance — through development of physical parameters, to imprinting of constraints within the PCB database for constraint-driven design flow, and finally to post-layout extraction and verification of complex high-speed PCB systems.

SPECCTRAQUEST SI EXPERT COMPONENTS
SPECCTRAQuest provides a set of modules that are completely integrated to support the entire high-speed PCB system design. It is tightly integrated with the Allegro® PCB layout system as well as with the industry standard SPECCTRA® autorouter for routing critical nets based on high-speed constraints.

SPECCTRAQuest directly reads and writes the Allegro PCB database format (.brd file) to provide complete integration with Allegro-based PCB design flows. This allows you to perform high-speed analysis at any stage of the design cycle: when the board is partially or fully placed; partially or fully routed; and even when no netlist or PCB database exists. SPECCTRAQuest’s unique ability to
operate directly from the PCB database without translation, and its unique ability to create constraints that drive the placement and routing processes, ensures that high-speed design constraints are quickly and accurately implemented.

SPECCTRAQuest SI Expert includes eight main components: SPECCTRAQuest Model Integrity, floorplanner/editor, Constraint Manager, SigXplorer topology exploration environment, SigNoise simulation subsystem, EMI design rule checker, EMControl, and SPECCTRA Expert autorouter.

SPECCTRAQUEST MODEL INTEGRITY
The Model Integrity module within SPECCTRAQuest SI Expert allows you to create, manipulate, and validate models quickly in an easy-to-use editing environment. Model Integrity provides a model browser and syntax checker for models written in IBIS as well as advanced models written in Device Modeling Language (DML) from Cadence. The marker navigation functionality provides an easy way to fix IBIS model parsing problems. Models can also be verified using SigNoise with simple test circuits specified within Model Integrity.

SPECCTRAQUEST FLOORPLANNER/EDITOR
The SPECCTRAQuest floorplanner provides a graphical view of the PCB database allowing you to view, simulate, and edit the PCB design. Designers can quickly and easily evaluate the effects of different placement strategies on design behavior. You can perform test routing using proposed electrical constraints to ensure high-speed design rules are achievable before passing them on to the PCB layout designer.

Hierarchical constraint management means that the same constraints can be applied to a collection of signals and overridden on a case-by-case basis. Constraint Manager is completely integrated with the Allegro design rules-checking system; the different high-speed rules can be checked in real time as the design process proceeds, with the results presented as part of the Constraint Manager spreadsheets. Any design parameters that do not meet their associated constraint values are highlighted. Constraint Manager also integrates the results of SI analysis, allowing designers to manage simulation-based electrical constraints. By combining knowledge of bus operating speeds with component timing data and the results of SI analysis, one spreadsheet shows the designer whether or not critical system level timing requirements will be met.

At any point during physical design, you can launch the Constraint Manager to view high-speed constraint information associated with the design. The spreadsheet presents two views of the constraint information in the database. One view allows you to see the different electrical constraint sets present in the database and their associated constraint values. The other view presents the different nets contained in the system, the names of the constraint sets associated with those nets (if any), and their associated constraint values. Constraint Manager also displays the results of design analysis in real time alongside the constraint values in the spreadsheet and color codes the results to indicate success or failure. This allows designers to see the impact of any design changes immediately updated in the spreadsheet.

SIGXPLORER TOPOLOGY DEVELOPMENT ENVIRONMENT
SigXplorer is a graphical environment for exploring, analyzing, and defining interconnect strategies that provide an electrical view of the physical interconnect. This allows the electrical engineer to explore different placement and routing strategies from an
electrical standpoint and develop a comprehensive set of design rules. SigXplorer extracts electrical views of nets from both placed (pre-route) and finished (post-route) databases at which point the net model can be analyzed and edited in detail.

SigXplorer displays the electrical model of the net and the associated simulation results within a single window. The upper portion of the window shows the net model, while the lower portion of the window contains a series of spreadsheets that display editable circuit parameters and control what type of simulation is running, which measurements are presented, and the associated simulation results.

Once the appropriate electrical design rules have been determined, SigXplorer allows you to capture design constraints as an ECSet that will be imprinted into the PCB database and used to drive the physical design process.

SigXplorer serves three different functions in the overall SPECCTRAQuest high-speed design process:

1 Pre-route Topology Exploration and Solution Space Analysis
SigXplorer is used to perform “what if” analysis and determine the effects of different routing strategies, component values, and design tolerances. Swept-parameter analysis is used to model the behavior of the circuit under a wide range of conditions, and define the optimum design constraints for the final design. For example, you can sweep design parameter such as differential impedance and delay/length. Once design parameters are chosen, you can then explore physical implementation parameters such as trace width, gap, and maximum uncoupled length for differential signals.

For pre-route analysis, SigXplorer can use either ideal (lossless) or non-ideal (lossy or lossy coupled) representations of transmission lines.

2 Template-driven Design
SigXplorer allows routing strategies to be graphically captured for “imprinting” into the PCB database. SigXplorer is used to graphically define the desired routing strategy including pin ordering, the location of any “T-points” (virtual pins), the locations of terminators, and other discrete devices on the net. High-speed routing rules including physical or electrical lengths, target impedances, physical or electrical length matching requirements, stub lengths, EMI constraints, and other high-speed rules are captured as part of the topology template. This topology template is then used as a routing blueprint and referenced by all the nets in the PCB design with the same electrical requirements. In this manner, a single topology template can quickly and easily be used to constrain entire buses within the target design.

SigXplorer allows electrical and physical design rules to be captured as topology templates that drive the placement and routing processes.

3 Post-route Analysis
SigXplorer extracts a detailed electrical representation of how the net was physically implemented, including detailed models for trace cross-sectional characteristics, routing layers, via models, and trace lengths. Because SigXplorer presents the post-route simulation model as a graphical, electrical representation, designers can quickly isolate the causes of any unexpected design problems. SigXplorer allows the designer to edit the post-route net model and re-simulate to quickly determine the effect of various changes to the routing strategy. Once the corrective action has been identified, you can use that knowledge to update the PCB design.

SigXplorer extracts post-route interconnect models that provide detailed electrical characteristics of routed etch, vias, and connectors.

SIGNOISE SIMULATION SUBSYSTEM
SigNoise is the Cadence simulation environment for signal integrity, crosstalk, and optional EMI analysis. SigNoise includes the tlsim simulation engine, the SigWave waveform display, the DML modeling language, translators from other modeling formats, and a library model editing/management subsystem. SigNoise integrates directly with the SPECCTRAQuest floorplanner, SigXplorer, and Allegro Expert to provide simulation results from the different physical and electrical views of the interconnect.

The tlsim simulation engine is a SPICE-based simulator that combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. Tlsim includes an IBIS-style behavioral driver element that models I/O behavior based on the V-I and V-T data provided by behavioral modeling.
helps designers identify which nets
are likely to cause EMI problems, and
explore the design strategies required
to keep radiation within acceptable
levels. Near-field EMI analysis is
available within SPECCTRAQuest floor-
planner that predicts radiated energy
immediately above the board surface.
By analyzing near-field EMI patterns,
you can identify which portions of a
routed trace are producing the most
radiated energy and adapt the
design accordingly.

The SigWave waveform display can
present simulation results in multiple
formats. The oscilloscope mode allows
display of individual waveforms to be
turned on and off, provides markers
for use in making on-screen measure-
ments, and allows notes to be added
to the display. The logic-analyzer
mode presents waveforms alongside
each other, so that logic behavior and
bus transactions are easier to observe.
The spectrum analyzer mode displays
signal behavior in the frequency
domain using one of several different
FFT techniques. The eye-diagram mode
is useful for viewing patterns in long
simulation sequences and allows the
user to interactively define the signal
period and starting offset. SigWave
allows waveform data to be directly
imported from various standard test
equipment formats and the output
formats of popular SI analysis tools.

EMCONTROL

EMControl provides differential-mode
EMI analysis and advanced EMI design
rule checking to the SPECCTRAQuest
design environment. EMControl
provides prediction of far-field
differential-mode radiated emissions
in both SigXplorer and the
SPECCTRAQuest floorplanner.
Simulation of differential emissions
helps designers identify which nets

The high-speed design cycle:
Architectural analysis

SigXplorerer can be used for standalone
topology design and analysis before
a PCB database is available. This type
of analysis is common at the earliest
stages of the design cycle, where
designers perform studies on the
impact of using a new device technol-
ogy or assess the impact of increasing
the bus transfer rate. You can use
SigXplorer to build and validate
detailed electrical topology models
and prove that a new technology is
viable before the detailed design
process begins.

Topology exploration

Once the design schematic has been
captured and packaged, you can use
SPECCTRAQuest to quickly evaluate
the effect of different placement
and routing strategies. The designer
extracts an electrical model of the net
that reflects the way the autorouter
would route the target net with the
design rules left “as is.” SigXplorer is
used to analyze the net and determine
if an alternative design strategy is
required. The net’s electrical rules can
then be defined for imprinting into
the PCB database. Using this “explore-
constrain-test” model, designers can
quickly and effectively determine the
best strategies for optimizing the
behavior of critical nets.

Solution space exploration

Solution space analysis extends
topology exploration by taking
tolerances into account. Tolerances
result from manufacturing-related
variances (device buffer speed,
impedance fluctuation, etc.) or can
represent a range of design condi-
tions. For example, the differential
impedance or the different permissible
routed lengths for a section of trace.
SigXplorer allows you to enter the
design parameters to be varied, and
then automatically analyzes the circuit
under all possible combinations of
conditions. For example, you can then
explore physical implementation
parameters such as trace width, gap,
and maximum uncoupled length.
You can also do broadside and edge-coupled crosstalk analysis where an aggressor can be a single line or another differential pair signal.

Solution space analysis extends topology exploration by taking tolerances into account.

The results of the swept-parameter analysis are displayed in a spreadsheet format within the SigXplorer window. You can select any of the different simulation “cases” and view the associated simulation waveforms. The spreadsheet data can be sorted within the SigXplorer interface, or exported in a standard tab-delimited format for use with other spreadsheet and data post-processing programs. Designers can use the swept-parameter analysis capabilities of SigXplorer to identify robust routing and placement rules that ensure the design will work reliably under real-world conditions.

TOPOLOGY TEMPLATE-DRIVEN DESIGN

Once the high-speed design rules have been defined, SigXplorer is used to graphically create a topology template that will be used as the blueprint for placing and routing the design. Constraint Manager gives you the flexibility of importing those rule sets directly into the PCB database or forwarding the individual rule sets to the CAD group for use in placing and routing the board. Topology templates can also be created directly from semiconductor manufacturers' routing guidelines, effectively translating paper design rules into their electronic counterparts for use in driving the physical design process. When robust design rules are used to drive the placement and routing processes, the likelihood of achieving a “right first time” design process is greatly increased.

TIMING-DRIVEN PLACEMENT

The Constraint Manager allows you to view different electrical rules in the database, and updates in real time as components are moved and nets are routed. By showing the electrical design rules associated with each component, one of the Constraint Manager's spreadsheets aids you in optimizing multiple tradeoffs associated with the placement of each component. This timing spreadsheet integrates Si analysis with component timing information, providing bus-level static timing analysis directly from the PCB database. It combines component-level timing information (device output delay, setup/hold requirements) with the results of Si analysis (min/max flight time) and system-level information (clock period and clock jitter/skew budgets) to provide system-level, post-layout timing analysis directly from the PCB database.

Because SPECCTRAQuest Si Expert and Constraint Manager operate directly off the Allegro PCB database, violations of electrical design rules can be graphically displayed as design rule checking (DRC) violations in the PCB layout and colored violations with margin information in the Constraint Manager spreadsheet. This allows designers to quickly identify problems in the database, without the need to run exhaustive post-layout simulations just to find simple electrical violations. Design-rule violations are displayed graphically, allowing the user to select the DRC in question to obtain detailed information about the rule violation.

CONSTRAINT-DRIVEN DESIGN

SPECCTRAQuest Si Expert allows electrical designers to choose how involved they will become with the physical design process, depending on the specific design scenario and their experience level. SPECCTRAQuest allows users to place and test-route sections of the design and ensure that high-speed design rules are physically achievable. While designers can choose to “lock down” traces and pass the routing information forward to PCB layout, this is not required. When solution space analysis is used to define robust routing rules, the PCB layout designer is free to use any routing strategy that meets the electrical design rules. This gives you maximum freedom to create routing strategies that accommodate other design constraints (mechanical, cost, etc.) and optimize the overall design.

SPECCTRAQuest SI Expert leverages the extensive DRC capabilities of Allegro to quickly identify violations of electrical and physical design rules. Common problems can be identified and resolved before post-route simulation begins.
Because the design rules are contained in the Allegro database, the PCB layout designer can leverage Allegro’s DRC system and the Constraint Manager to detect electrical design problems in real time, instead of passing the design back to the electrical engineer for lengthy analysis. Imprinting the design rules into the Allegro database allows the physical designer to ensure that the design complies with electrical rules. This eliminates any risk of miscommunication between the electrical and physical designers and any associated schedule impact. Allegro Expert allows the physical designer to take individual topology templates from the electrical designer and individually imprint them into the database. Constraint Manager can also be launched from Allegro Expert. This allows the physical designer to use the same mechanism as the electrical designer to take updated versions of electrical rules, and selectively imprint them into an existing design to determine impact on existing placement and routing, before committing the changes to the database. In this manner, the interactions between the electrical and physical designers can be optimized, and the tradeoffs between physical and electrical constraints can be best understood and managed.

POST-LAYOUT ANALYSIS
Once the physical design is complete, SPECCTRAQuest SI Expert is used to perform system-level signal integrity, crosstalk, and optional EMI analysis on the design. SPECCTRAQuest SI Expert allows multiple PCB designs to be “linked” together to form a complete system definition, including any connectors/cables and their associated parasitic information.

When the full SPECCTRAQuest design flow is used to define critical net placement and routing strategies, the chance of finding speed-related problems after layout is minimized. If and when problems do occur, SPECCTRAQuest’s integration with the Allegro database eases the process of understanding and fixing the problem. Extraction of detailed post-route electrical models into SigXplorer allows the designer to understand exactly how the net was routed from an electrical standpoint. The post-route topology can be edited for “what if” exploration to determine the potential benefits of changing the routing strategy. Once the cause of the problem is understood, the etch can be edited directly in SPECCTRAQuest SI Expert and re-analyzed, or the design rules can be modified and passed back to the PCB layout designer for modification.

HIGH-SPEED MODELING
SPECCTRAQuest SI Expert can accept device models from a variety of different high-speed digital modeling formats. Support for the IBIS 3.2 modeling standard allows SPECCTRAQuest to use models created by most semiconductor manufacturers. Models can also be translated from the Innoveda®/Quad XTK® simulator format, or created from Spice device models. In addition, SPECCTRAQuest SI Expert provides users looking to model more complex devices, a Device Modeling Language (DML). The Model Integrity module included in SPECCTRAQuest SI Expert allows users to create, manipulate (edit, cut-and-paste) and validate models that can be in IBIS 3.2 or DML format.

SPECCTRAQuest SI Expert Model Integrity module.

The simulation engine in SPECCTRAQuest (tlsim) includes a lossy, coupled, frequency-dependent transmission line model that provides highly accurate modeling of the electrical behavior of PCB traces. An integrated electrical field solver is used to determine the electrical characteristics of routed etch and create electrical models of PCB vias.

COMPATIBILITY
SPECCTRAQuest SI Expert has been designed for use with the Allegro Expert PCB layout system and the SPECCTRA Expert autorouter. SPECCTRAQuest SI Expert works with any front-end schematic capture system capable of outputting a packaged Allegro netlist and can read in the same netlist formats as Allegro. For designs captured with Cadence’s Concept® HDL editor, the design synchronization utility compares the logical and physical representations of the design, automatically identifying any differences and allowing the designer to specify which properties or components should be transferred between representations.

Topology templates created with SPECCTRAQuest SI Expert can also be associated with critical nets at the schematic level with Constraint Manager, and the imprinting of the associated design rules performed automatically when the netlist is read into either SPECCTRAQuest SI Expert or Allegro Expert. This allows the association between high-speed...
design rules and critical nets to be captured as part of the schematic representation for the system.

New SPECCTRAQuest differential pairs exploration and extraction functionality allows you to simulate differential signals as a unit in pre- and post-layout simulations, improving both design quality and productivity. SigXplorer’s solution space exploration capability has been extended to allow engineers to sweep design parameters such as differential impedance and delay/length. Once design parameters are chosen, you can then explore physical implementation parameters such as trace width, gap, and maximum uncoupled length. Engineers can also do broadside and edge-coupled crosstalk analysis where an aggressor can be a single line or another differential pair signal. Once constraints are developed and physical layout (routing) is complete, you can extract the differential signal as an entity for post-layout verification.

SYNCHRONOUS SYSTEM DESIGN

The standard synchronous design flow for SPECCTRAQuest builds on the rules-based design flow by using SigNoise to perform extensive pre- and post-route SI analysis. Solution space analysis explores topologies and defines optimum placement and routing rules. Once the design rules are captured as a topology template, the rules are imprinted into the database and used to drive the placement and routing processes. The design process proceeds as with template-driven design, with the addition that SI analysis can be performed at any point in the design process. When placement and routing is complete, post-route signal integrity and crosstalk simulations are used to sign-off the design before committing it to manufacturing.

The latest generation of high-speed system designs employ system buses that use source-synchronous (clock-forwarding) techniques to achieve dramatic increases in data transfer rates. These new technologies require a completely different approach to system level timing and signal integrity analysis. SPECCTRAQuest SI Expert allows you to model these complex new bus designs, perform protocol-level timing analysis, and define their own custom simulation-based timing measurements to parameterize the results of simulation. Combined with SigXplorer’s swept-parameter analysis capabilities, these capabilities make SPECCTRAQuest SI Expert the most powerful and flexible tool available for next-generation custom bus design and analysis. Design rules defined using these advanced simulation techniques are captured as topology templates and used to drive the placement and routing processes, as with the other design flows.

MENTOR BOARD STATION FLOW

SPECCTRAQuest SI Expert can be used in conjunction with the Mentor® Board Station® PCB design system to provide high-speed design and analysis within a Mentor-based PCB design environment. SPECCTRAQuest is used to perform high-speed analysis, and to define the high-speed design rules used to drive the SPECCTRA autorouter. Once the design has been placed and routed in accordance with the high-speed rules, the results are passed back to the Mentor Board Station environment via the SPECCTRA interface. This allows SPECCTRAQuest SI Expert and SPECCTRA to be used for high-speed design and analysis, while the existing Board Station-based manufacturing output process is used for committing the design to manufacturing.

SPECCTRAQUEST PRODUCTIVITY ENHANCERS:

INTEL ARCHITECTURE DESIGN KITS

Cadence has worked with Intel to provide extensive support for the IA-32 and IA-64 architectures. Intel® Architecture Design Kits combine verified SI models with topology templates for Intel-specified design rules, sample PCB layouts and tutorial
“how to” movies illustrating the use of best-known practices for creating IA-32/64 designs with SPECCTRAQuest SI Expert. Intel Architecture Design Kits are available free of charge to qualified customers. For more information, visit www.specctraquest.com, a SPECCTRAQuest users community or contact your Intel or Cadence representative.

XILINX VIRTEX II-PRO DESIGN KIT

Xilinx® and Cadence engineers have worked together to provide a high-speed design kit in SPECCTRAQuest format for multi-gigabit serial Rocket I/O™ transceivers integrated in Xilinx’ Virtex II-Pro FPGAs. The SPECCTRAQuest Design Kit helps engineers shorten design cycles and reduce signal integrity problems when implementing multi-gigabit serial transceivers in PCB systems. It contains correlated silicon models as well as pre-configured topologies ready to simulate. It also contains fully coupled frequency-dependent lossy package, PCB trace, via and connector models to fully simulate and evaluate the signal quality and degradation issues inherent in designs with multi-gigabit transceivers. For more information, visit www.xilinx.com or contact your Xilinx or Cadence representative.

METHODOLOGY SERVICES

Cadence provides a complete offering of customer services called methodology services. From individual product solutions to team-based environments, methodology services help customers achieve maximum productivity in a minimum amount of time. Our methodology experts can deploy a PCB development process that delivers repeatable design successes while reducing your time to market.

CADENCE METHODOLOGY SERVICES INCLUDE:

QuickStart Services - A QuickStart service is a pre-packaged, pre-defined, and pre-priced service that includes installation and verification of a Cadence product. It helps accelerate the implementation and use of a Cadence solution within a specific engineering environment.

CIS Implementation and Database Creation Services – Using your internal resources to install new systems and software can disrupt your workflow. Methodology services can take the burden off your IS and engineering staff with CIS Implementation and Database Creation services. A team of CIS professionals can deliver a completed CIS implementation service or prepare and populate your existing library. Our involvement ensures that you’ll have an optimal configuration from the start.

Conversion Services – Cadence methodology services offers several migration services. If you have designs or libraries that need to be migrated, we can perform the conversions for you. These services are especially useful when you have large numbers of files to convert, or if you have designs that require hand conversion beyond the capabilities of commercial translators.

Onsite Consulting – Please contact your Cadence account manager for detailed information on how a Cadence application engineer can assist you.

EDUCATION SERVICES

From basic product training to advanced high-speed PCB and IC packaging design techniques, Cadence training and education services accelerate your learning curve and put your company on a direct path to increased competitiveness. A variety of public, private, and Internet-based courses are available. For detailed information on training schedules and locations, please visit: www.cadence.com/education.

FOR MORE INFORMATION

Email us at pcbsalesinfo@cadence.com. Or log on to www.cadencepcb.com. To locate a Cadence PCB sales office or Value-added Reseller in your area, visit www.cadencepcb.com/contacts/globalnetwork.