HIGH-SPEED SYSTEM INTERCONNECT DESIGN

CADENCE TECHNOLOGIES MEET INDUSTRY’S NEED FOR SPEED
HIGH-SPEED PACKAGE-BOARD DESIGN TECHNOLOGIES MOVE AT MULTIGIGABIT SPEED

Electronics miniaturization, nanometer silicon, multigigabit serial interfaces, mixed-signal devices, and system-level design are creating new challenges for PCB designers. The complex challenges — ensuring signal integrity, reliable timing, adequate power distribution, and successful multi-layer routing — can no longer be met with traditional tools and traditional design methodologies.

Intent on providing leading-edge solutions to these problems, Cadence has introduced a number of new technologies that address high-speed PCB system interconnect design. Some are first-of-a-kind technologies, some involve silicon-package-board co-design technologies, all are designed to increase engineering productivity and optimize the quality and performance of electronic products.
CONCEPT HDL EXPERT
Concept® HDL schematic capture offers powerful schematic design capabilities and integrates easily with PSpice® analog and mixed-signal simulation and Cadence® NC-Sim digital simulation. Coupled with Constraint Manager, Concept HDL expedites the design process by automating the communication of high-speed design requirements between engineer and board designer.

CONSTRAINT MANAGER
Constraint Manager is an intelligent spreadsheet-based electrical constraint management system that improves time-to-market by limiting the number of iterations between engineering, layout, and prototype. It provides a real-time display of high-speed rules and makes the information available in all stages of the design process to all members of the design team. With a highly optimized spreadsheet interface, users can capture, manage, and validate the different rules in a hierarchical fashion.

ALLEGRO EXPERT
Allegro® Expert PCB layout is the world’s leading advanced PCB layout system. Allegro employs an interactive, high-speed, constraint-driven environment for creating and editing complex, multi-layer PCBs. Features include: advanced floorplanning; push, shove, slide and bubble etch editing; comprehensive differential pair support; real-time electrical and physical DRC; and a host of high-volume manufacturing capabilities.

SPECCTRAQUEST SI EXPERT
SPECCTRAQuest™ SI Expert provides a complete environment for the exploration, design, simulation, and analysis of high-speed digital systems interconnect. SPECCTRAQuest SI Expert provides a Topology Editor for solution space exploration,
hierarchical Constraint Manager, interconnect editing, and a comprehensive set of pre- and post-layout analysis tools. A SPECCTRAQuest analysis can be performed at the IC package, board, multi-board, and/or at the system level across multiple design configurations for true, die-to-die interconnect design and analysis.

**SPECCTRA EXPERT SYSTEM**
Designed to handle high-density PCBs that require complex high-speed design rules, SPECCTRA® Expert employs powerful shape-based algorithms to make the most efficient use of the routing area. It is the market-leading solution for automatic and interactive interconnect routing for PCB and IC packaging.

**PCB LIBRARIAN EXPERT**
Incorporating the latest technology from Cadence, PCB Librarian Expert automates and accelerates the entire library creation process. It contains everything a librarian needs to create, validate, and verify the packaging of library parts from Concept HDL schematic capture through the Allegro PCB layout flow. Included are Library Explorer and Part Developer for part generation.

**APD AND APE FOR ADVANCED IC PACKAGING**
Cadence Advanced Package Designer (APD) and Advanced Package Engineer (APE) solutions offer the industry’s most robust set of capabilities targeted at current and future packaging technologies. A new Autowire Bond capability for designing stacked-die packages, used in the fast growing system-in-package (SiP) market, meets manufacturers’ need for reduced design cycles and designers’ need for flexibility and reliability.
CO-DESIGN METHODS REDUCE COSTS, TIME TO MARKET

Faced with a fast system-on-chip (SoC) or system-in-package (SiP), a package with 2,000 I/Os, a complex multi-layer board, and a rapidly closing market window, engineers are eager to look across design domains for time and cost savings. Working with our partners and customers, Cadence has developed a number of technologies that support co-design methodologies. They represent some of the most exciting technologies in PCB system design today.

SILICON DESIGN-IN KITS SOLVE NEW DEVICE DESIGN DILEMMAS

Implementing a new generation high-speed device into a PCB system is a time-consuming and costly process. Because PCB and IC design environments are so different, SPICE (IC) models must be translated to IBIS (PCB) models in a lengthy and error-prone process. To address this issue, a new capability in SPECCTRAQuest allows IC manufacturers to create silicon design-in kits that enable PCB system designers to drastically reduce implementation times for new devices.

A design-in kit, an electronic blueprint for simulating and implementing silicon devices in a system, speeds time-to-volume production for IC manufacturers and time-to-market for systems companies.

COMPLETE DIFFERENTIAL SIGNAL DESIGN SOLUTION SPEEDS NETWORK APPLICATIONS

Today, complex multi-board network and communications applications can have hundreds — or even thousands — of differential signal pairs, causing long design cycles as engineers perform numerous ‘layout-simulate-fix’ iterations to successfully complete a design. The new Cadence integrated differential signaling design solution allows engineers to create, constrain, simulate, and manage differential signals throughout the entire design flow, addressing the problems inherent in integrating nanometer-scale devices into systems.

CONCURRENT IC PACKAGE AND PCB DESIGN

Cadence continues to advance its IC packaging suites with the latest in concurrent design methods. Advanced Package Engineer uses a convergent methodology that considers the path from the silicon-to-package, package-to-board, and back to silicon, ensuring signal integrity across the interconnect. Plus, as the majority of IC packaging foundries use Cadence design technologies, both IC packaging engineers and systems designers can co-design and analyze the die-to-die interconnect, helping to ensure package performance is optimized in the entire system.
Cadence PCB technologies are used to design today’s leading-edge high-speed products. Using Cadence products to the their fullest extent not only allows engineers and designers to meet the challenges of high-speed board designs, but also do it with unprecedented speed.

For more information, visit [www.cadence.com](http://www.cadence.com).