Quickstart OrCAD / Allegro PCB Editor

Version 22.1

FlowCAD

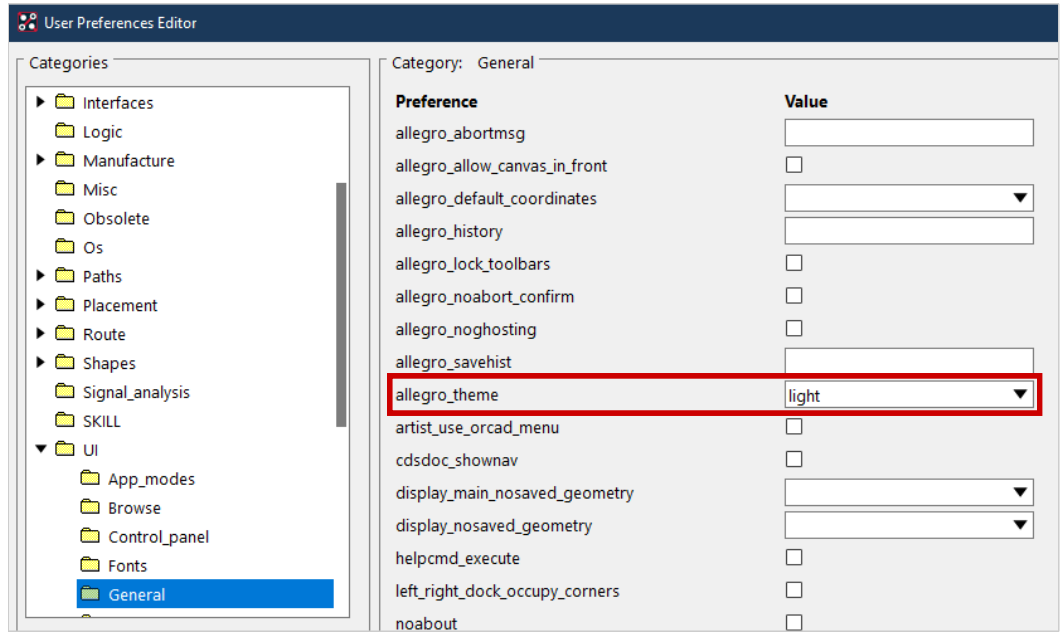
Table of Contents

Introduction – In General

- This documentation is created for first time users of Allegro / OrCAD PCB Software. It is neither a training handbook nor a complete user manual.
- Since instructions focus on PCB Editor only, there are no instructions for schematic entry. Start point for this quick start is an already completed OrCAD Capture schematic. A separate OrCAD Capture quick start document is available.
- Because of compactness of this documentation it is not possible to take up all available commands and their options. Here we reference to extensive online help documentation which is part of installation.
- Based on a simple schematic and related PCB layout we will elaborate most important steps of design flow. First time users of PCB Editor are enabled to complete first tasks independently with minimum effort.
- Detailed training offers for the different tools can be found at https://www.flowcad.com/en/training.htm

Introduction – Color Scheme

- The PCB Editor can be operated in both, a light and a dark theme.
- Icons will appear differently depending on which theme is selected.
- The color scheme can be switched under **Setup > User Preferences > UI > General**.
- This quick start shows light theme.

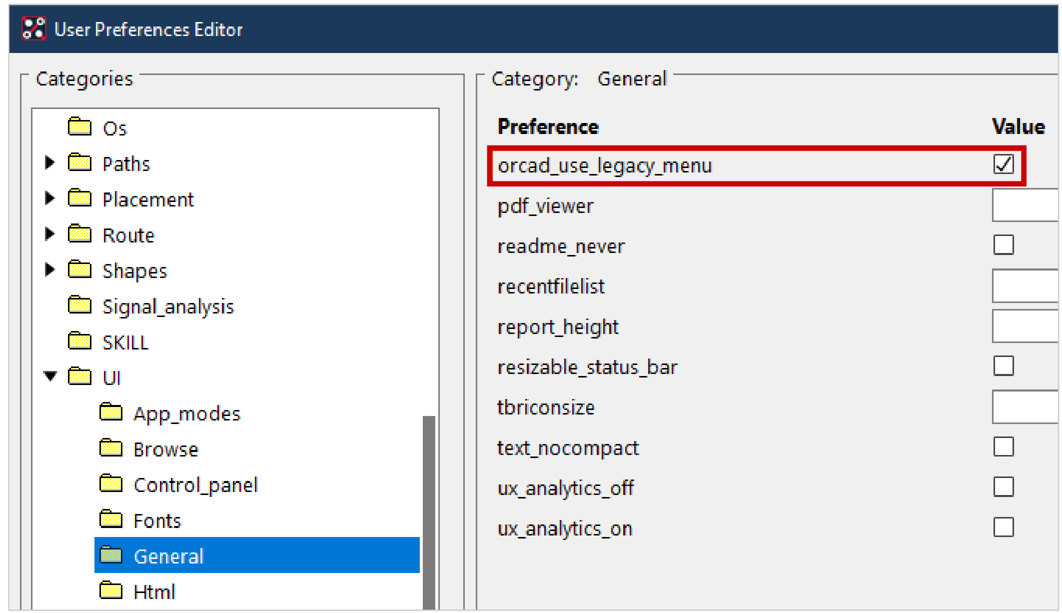


- Light Theme

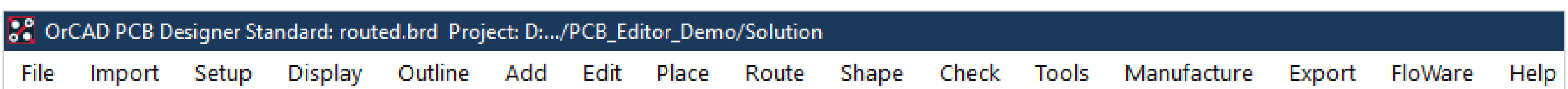
- Dark Theme

Introduction – Menu Structure

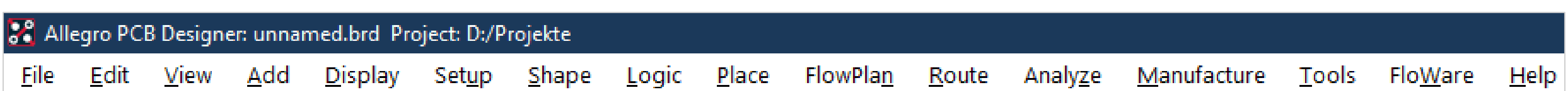
- Depending on whether an OrCAD or Allegro license is used, the menu structure is different.
- In this quick start the Allegro menu structure is used, because OrCAD can be operated with the Allegro menu.
- You can switch the menus under **Setup > User Preferences > UI > General**.



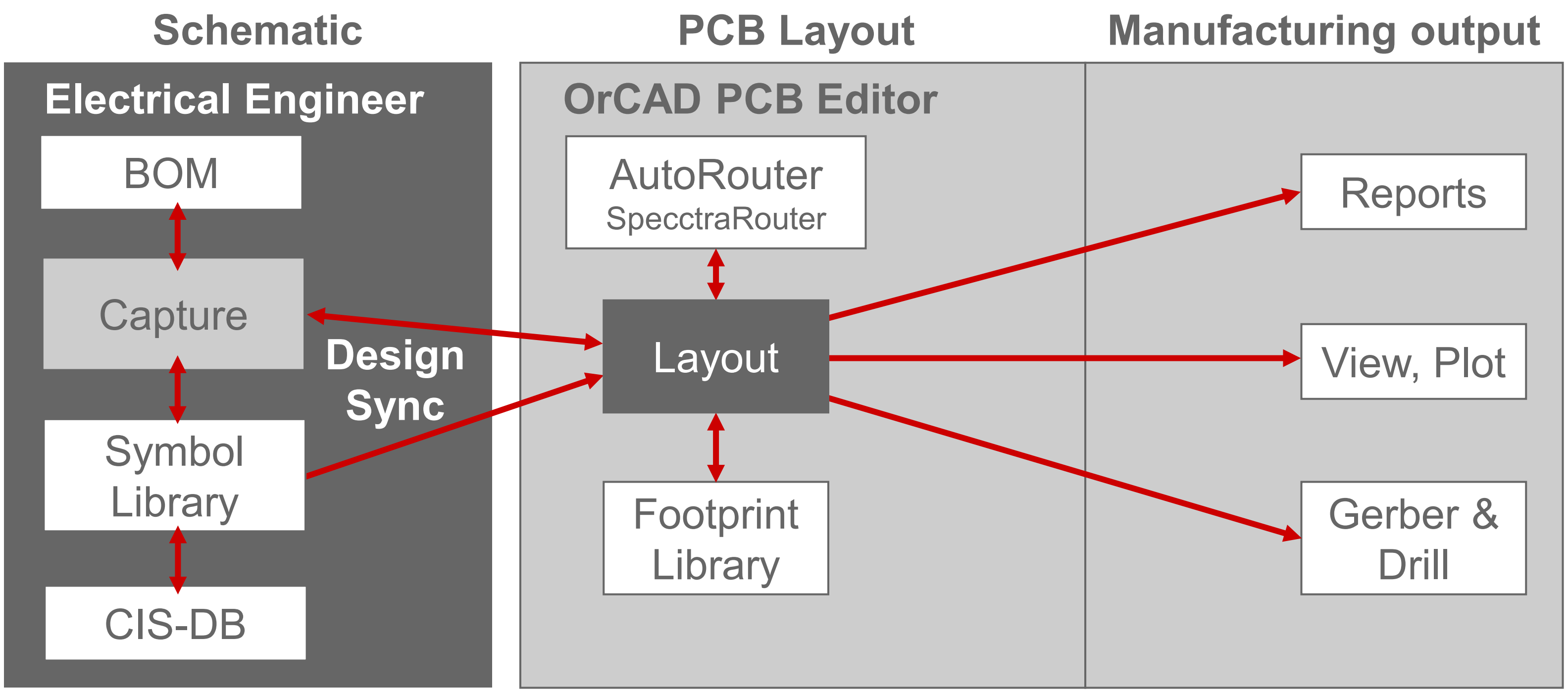
- OrCAD Menu



- Allegro Menu



OrCAD PCB Design Flow



- As you can see, the OrCAD PCB Designer Flow consists mainly of two parts.
  - These are the schematic capture module **Capture** and the layout module **OrCAD PCB Editor**.
- Both modules are supplemented by additional sub packages who represent in each combination an ideal tool, enabling the user to complete all tasks with maximized efficiency.

Necessary Steps in Schematic

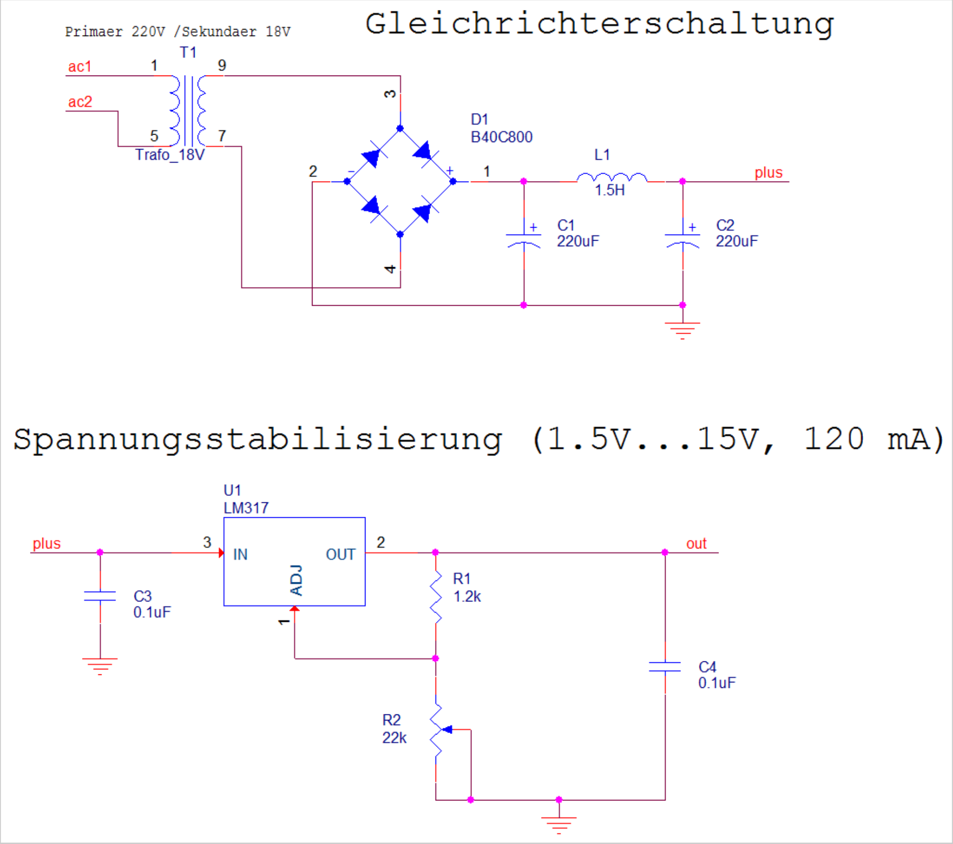
Necessary Steps in Schematic

- The steps described in this chapter give a brief overview.
- For Capture CIS a separate quick start is available.
- Logic data already exists in the training data and can be directly imported into a board-file as described in Lab Import of Logic Information on page 76.
- Logic data required for PCB Editor quick start can be found at: ~\PCB_Editor_Demo_22_1\PCB_Editor_Demo\project2

Schematic Template

The goal of a design flow is, as already mentioned in the introduction, is to design a PCB layout based on an existing schematic.
Please see below schematic used for our demo example.

More details regarding the Capture flow can be found in the Capture CIS Quick Start documentation.



REFDES – Footprints

In the list below we have listed footprints name of the parts manually assigned in the schematic. Footprints are symbols of electronic components used in the layout tool.

- T1 = ERA-EI30-2_8VA
- D1 = SM_GL_BRUECKE
- U1 = TO220abv
- R1 = SMR_1206
- R2 = VRES34
- L1 = SML_2220
- C1, C2 = Cpol_508
- C3, C4 = SMC_1206

Please ensure correct spelling.

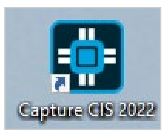
Start of Capture

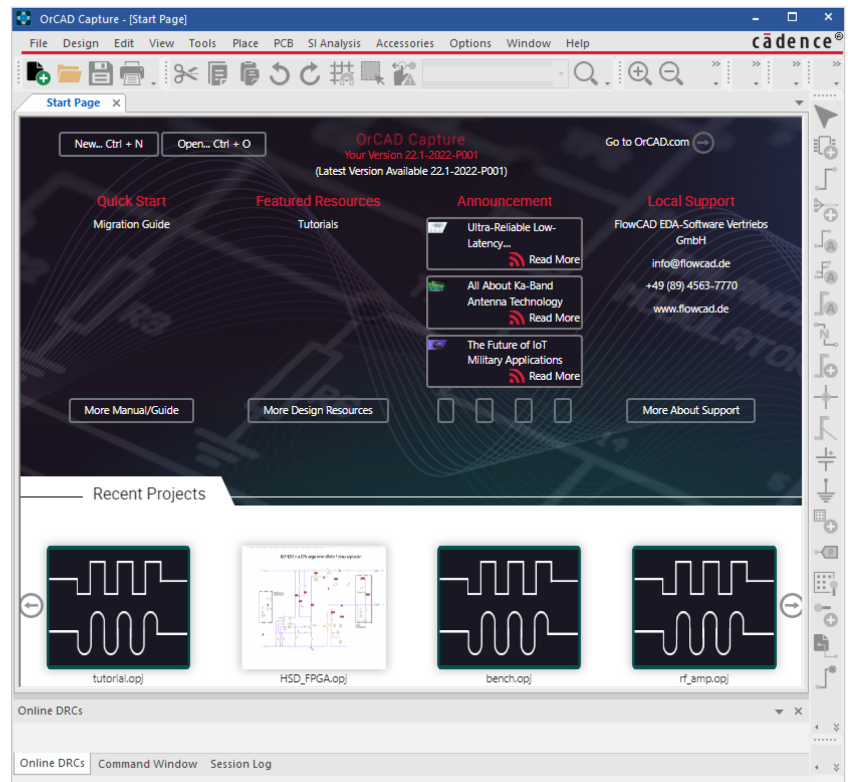
After starting Capture,
the Capture **Session Frame** window will open.

Start via:
Start > All Programs >
Cadence PCB 2022 > Capture CIS

or

Link
Icon on desktop





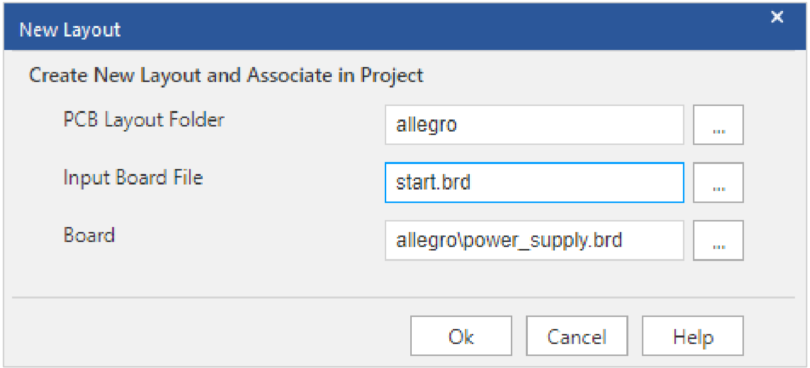
At the bottom of the window the **Session Log** window appears. It can be viewed also in a separate window. All events of the current session and messages from other Capture tools are listed here.

File > Open > Project… will open an existing project, in which the design (Power_Supply) is defined.

Layout Creation

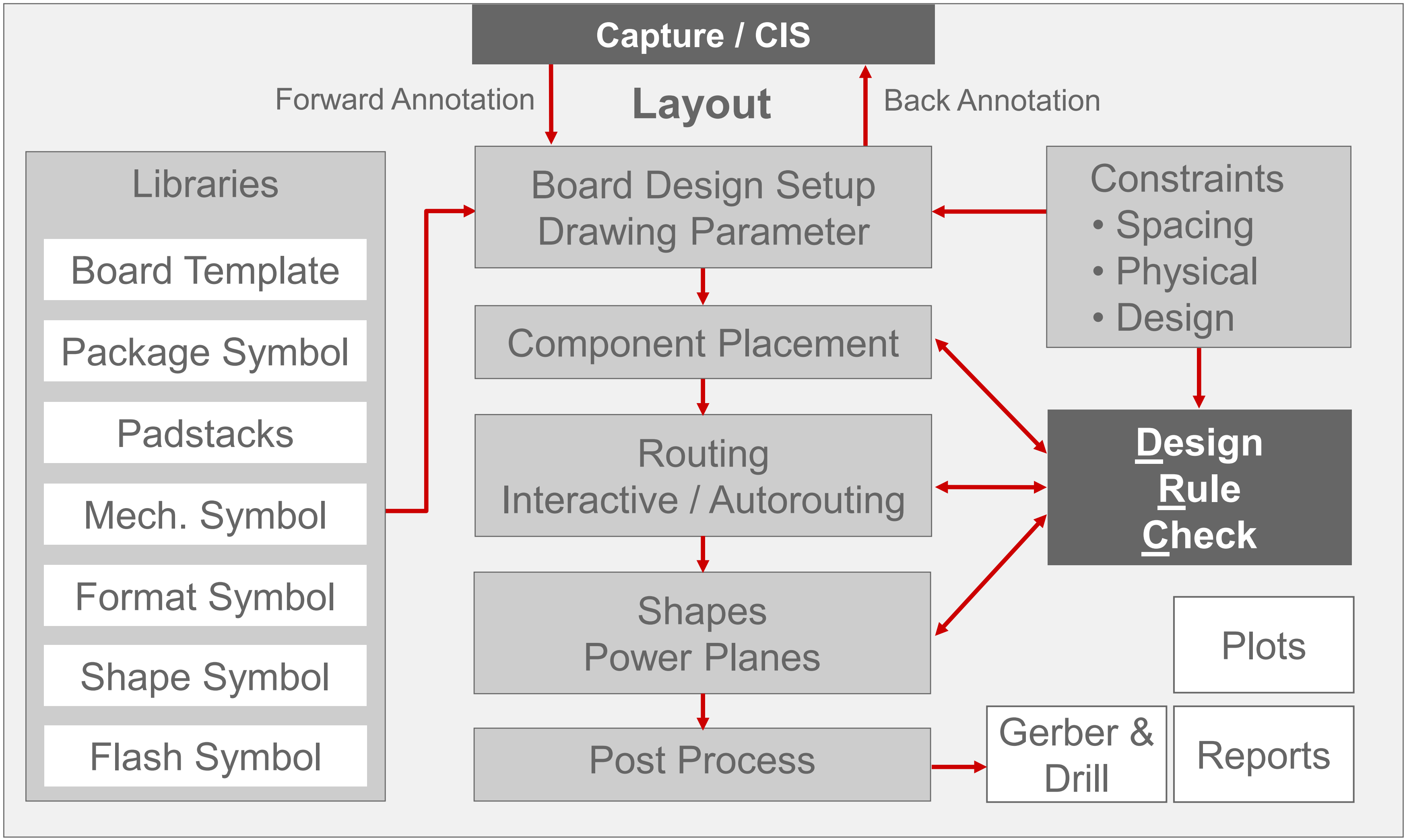
The logic data gets transferred via **PCB > New Layout** into new PCB.

- PCB Layout Folder: Folder for netlist data
- Input Board File: A base or predefined board template
- Board: New generated board file



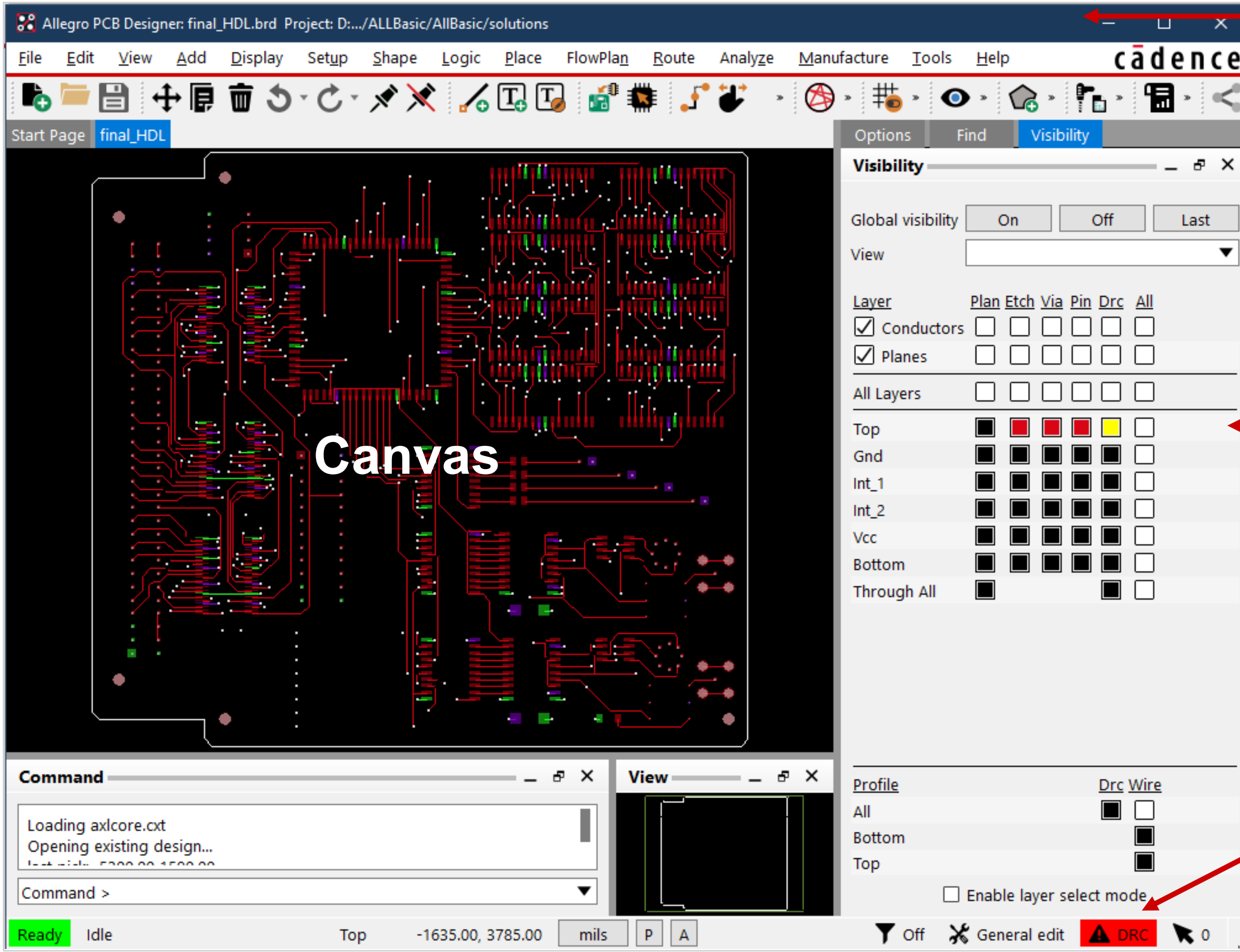
PCB Editor Flow Overview

PCB Editor Flow Overview



User Interface

PCB Editor and Canvas



Title Bar

Pull-down Menus

Icons / Toolbars

Control Panel(s)

Command Window

DRC Status

Status bar

Active Command

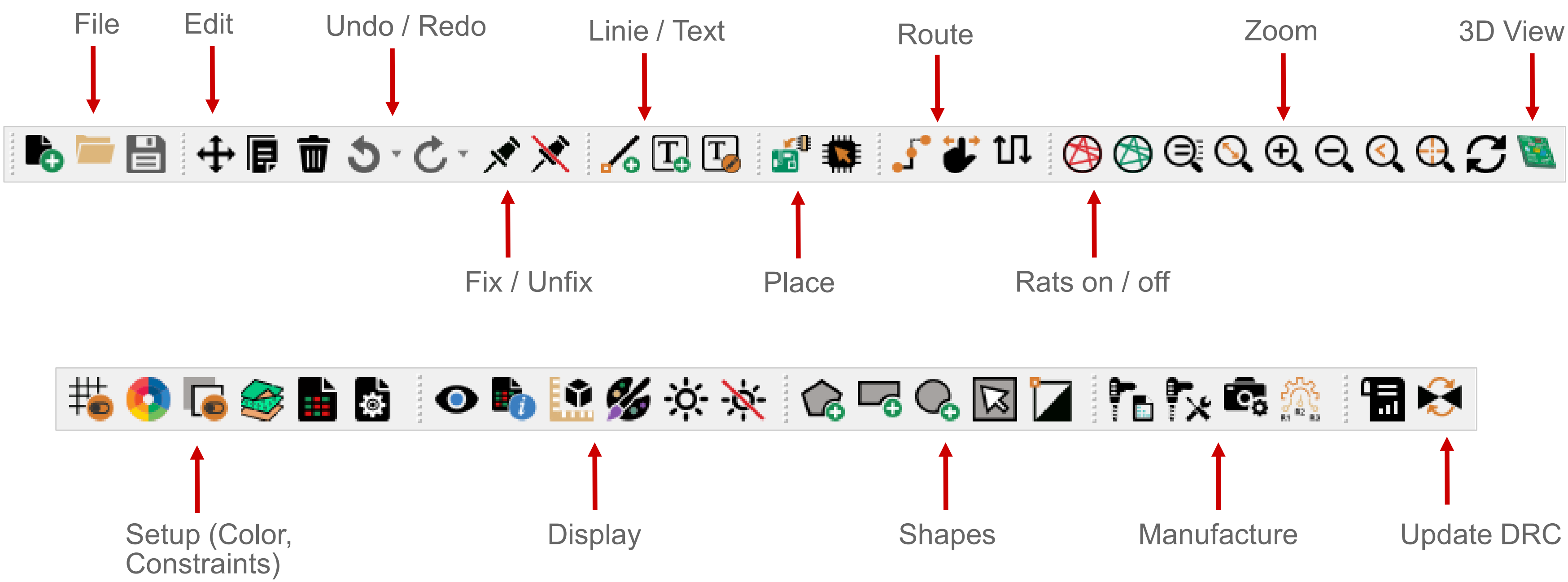
Active Layer

Cursor Position

Application Mode

Icons and Toolbars

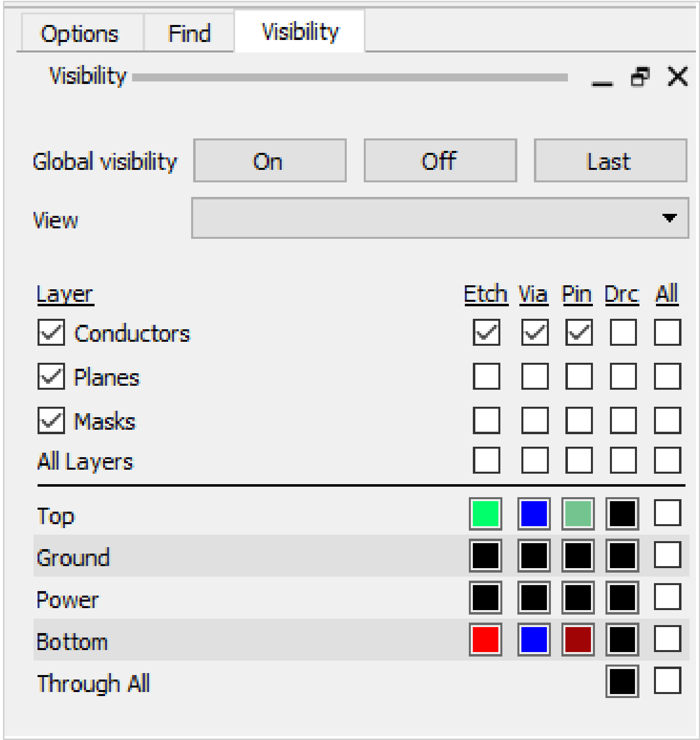
Here you can see the icons of the PCB Editor. They are bundled in groups, so-called toolbars.
View > Customize Toolbar allows to view or hide toolbars.
Like in Windows, toolbars can be arranged along outer edges of the Capture window or in a separate location.



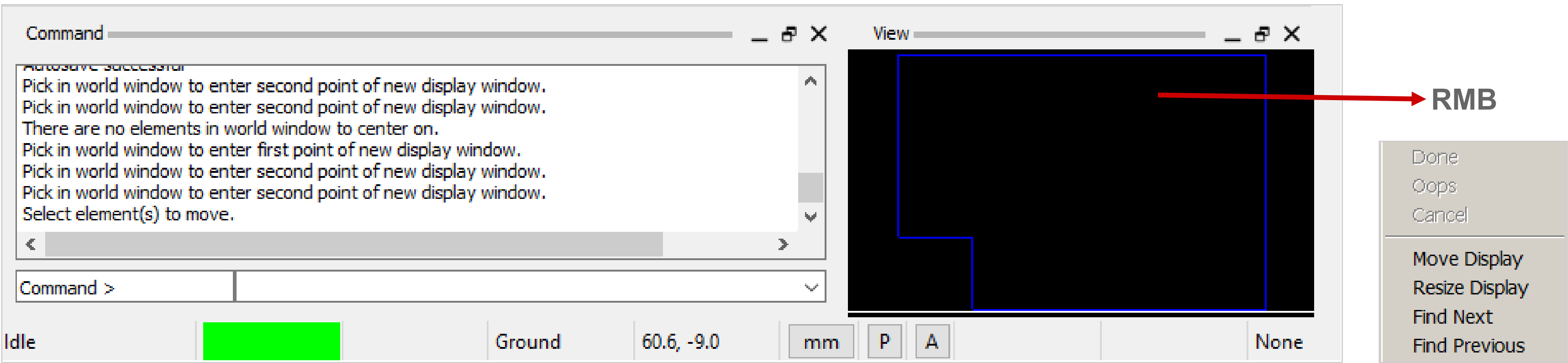
Note
When you hover with the mouse curser over an icon, a short description will be displayed.

Control Panels and World View Window (I)

- Options Tab
  - Shows current parameters and values for active command
  - Shows fields to control active commands
- Find Tab (Find Filter)
  - Controls which objects can be selected
  - You can also select objects by entering their name
- Visibility Tab
  - Controls visibility of routing objects (Etch, Pin, Via, DRC) on conductor and plane layers



Control Panels and World View Window (II)



View Window

- Shows actual view section relative to entire design
- Allows also to zoom into areas of the design

Command Window

- Allows to enter coordinates and command and shows system messages

Tip

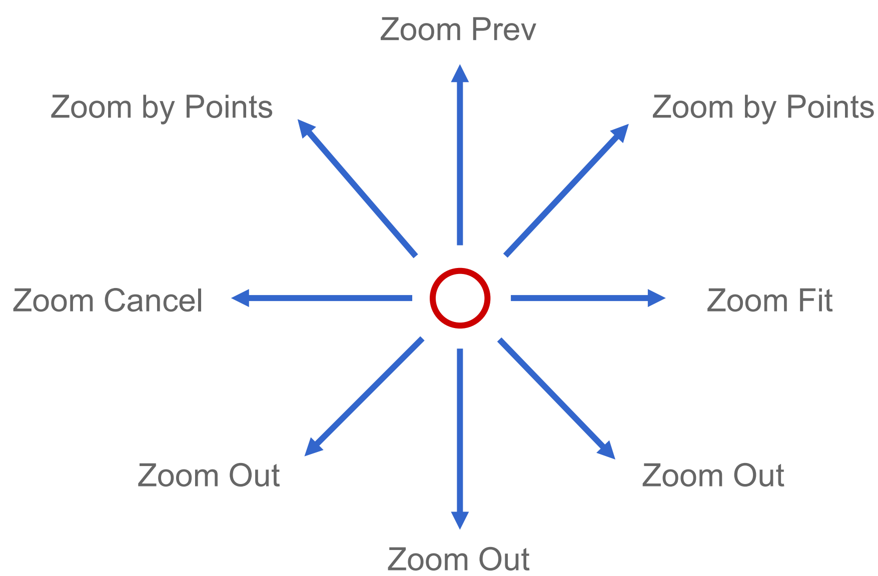
- For larger working area all windows can be closed separately (**View > Windows** or via).

Zoom Control with Middle Mouse Button

The middle mouse button provides a universal tool to zooming and panning in the design canvas.

1. Circle in the middle represents the original selection point. **1st click** with the middle mouse button (MMB).

2. The arrows represent the direction of mouse movement and following **2nd click** (MMB).



3. Press the middle mouse button (MMB) and move mouse. This is the way to pan actual view.

4. A double click (MMB) will execute command **Zoom Center.**

Aliases, Function Keys and Strokes

Aliases, Function keys and strokes allow to execute complete commands or even macros with one click.

Try to perform following examples as alias, function key and stroke:

1. Load board **sample.brd** (folder sample).
2. Type following commands, one after the other, in the command window and confirm with **ENTER:**
   - **alias Home zoom fit** (Assignment of ZOOM Fit on Pos1-key. Please ensure correct large and lower case).
   - **funckey r iangle 90** (Assignment of 90-degree rotation on R-Key. Please ensure correct large and lower case).
3. Use middle mouse key to zoom into a small area.
4. Press key Pos1 (or Home using an English keyboard). Command Zoom Fit will be executed.
5. Choose **Edit > Move** and select a component.
6. Press key **R** multiple times. Component will rotate by 90 degree every time.
7. Press **RMB > Done.**
8. Press **Ctrl** key and at same time **RMB.** Draw a small **Z** over a component.
9. Command **Zoom in** will be executed.

You have successfully defined an alias and a function as well as a stroke function.
Type **alias** in command line and **ENTER**. All default aliases and function keys will be displayed.
Select **Tools > Utilities > Stroke Editor.** Stroke editor will start and show all predefined strokes.

Tip
Two assignments above are only present in current session. How to define this kind of assignment permanently, will be explained in the next chapter.

Workspace

PCB Editor Data Structure

- A Board File (xyz.brd) is collection of many drawing layers. Each of these layers can be switched visible or invisible. To each layer a color can be assigned.
- PCB Editor is managing these drawing layers within a hierarchy of folders, classes and subclasses. Folders are a collection of classes to support users controlling colors and visibility.
- All elements are stored in kind of a 2-level database.
  - **First level** is referencing to different predefined classes. Some dedicated classes are combined in specific folders. Folders and classes can neither be deleted nor can new ones be added.
  - Within each class there are multiple subclasses. Subclasses are **second level** of database. They are called layers in the design. Predefined subclasses can not get deleted. You can add as many new subclasses as you want. These can get deleted if they do not contain any data.
- All copper structures are done on subclasses of class Etch.
  - For each electrical layer of the board you must add an appropriate subclass. This means, for a 4-layer multilayer you need four subclasses under class Etch.
- A new PCB board is by default generated as a 2-layer board consisting of top and bottom.
  - Predefined subclasses top and bottom can not get renamed or deleted.

Folders, Classes and Subclasses (I)

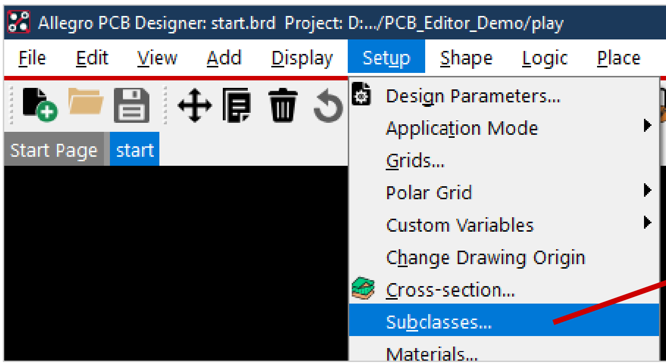
Folder	Classes	Subclasses
Display	Temp Highlight, Grids, Ratsnest (top, bot, thru), Perm Highlight, Waived DRCs, Drill holes, Via Label, Stacked via Label, Background, Pattern, Shading, Transparency	No Subclasses
Stackup / Conductor	Pin, Via, DRC, Etch, Anti Etch, Boundary	Top, Bottom (and all other user defined PCB board design layers)
Stackup / Non_Conductor	Pin, Via, DRC, Etch, Anti Etch, Boundary	Soldermask_Top, Soldermask_Bottom, Pastemask_Top, Pastemask_Bottom, Filmmasktop, Filmmaskbottom, Through All, Package_Top, Package_Bottom
Areas	Route Keepout, Via Keepout, Package Top, Bottom, Through All, Package Keepout, Package Keepin, Route Keepin, Constraints Region	Top, Bottom, Inner_Plane_Layers, Inner_Signal_Layers, Outer_Layers, Through All
Board Geometry	Board Geometry	Outline, Plating_Bar, Assembly Notes, Tooling_Corners, Dimension, Place_Grid_Top, Place_Grid_Bottom, Top_Room, Bottom_Room, Both_Rooms, Switch_Area_Top, Switch_Area_Bottom, Silkscreen_Top, Silkscreen_Bottom, Assembly_Detail, Soldermask_Top, Soldermask_Bottom, Off_Grid_Area, NcroutePath, Wb_Guide_Line

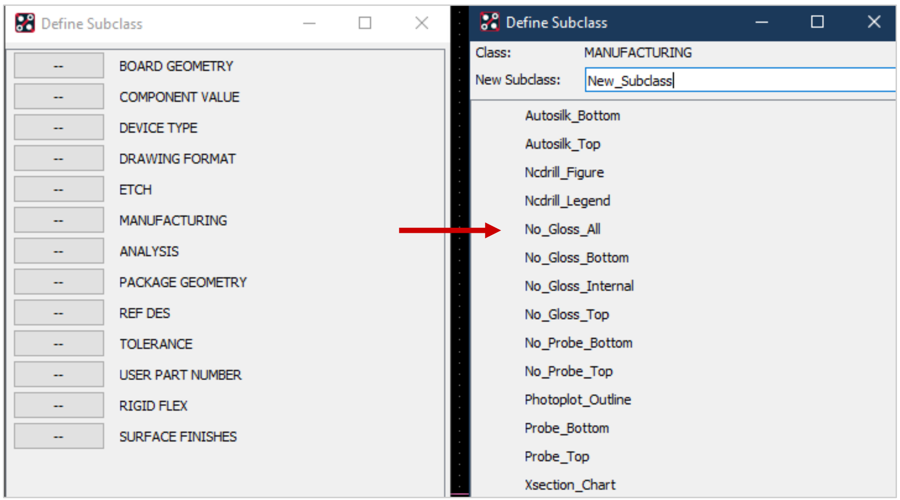
Folders, Classes and Subclasses (II)

Folder	Classes	Subclasses
Package Geometry	Package Geometry	Assembly_Top, Assembly_Bottom, Place_Bound_Top, Place_Bound_Bottom, Pin_Number, Pad_Stack_Name, Silkscreen_Top, Silkscreen_Bottom, Body_Center, Soldermask_Top, Soldermask_Bottom, Display_Top, Display_Bottom, Modules, Dfa_Bound_Top, Dfa_Bound_Bottom, PasteMask_Top, PasteMask_Bottom
Embedded Geometry	Embedded Geometry	All
Components	Comp Value, Device Type, Ref Des, Tolerance, User Part Number	Assembly_Top, Assembly_Bottom, Display_Top, Display_Bottom, Silkscreen_Top, Silkscreen_Bottom
Manufacturing	Manufacturing	Autosilk_Top, Autosilk_Bottom, Ncdrill_Legend, Ncdrill_Figure, No_Gloss_All, No_Gloss_Top, No_Gloss_Bottom, No_Gloss_Internal, No_Probe_Top, No_Probe_Bottom, Photoplot_Outline, Probe_Top, Probe_Bottom, Xsection_Chart
Drawing Format	Drawing Format	Drawing_Origin, Outline, Revision_Block, Revision_Data, Title_Block, Title_Data
Analysis	Analysis	Low_Isocontour, Medium1_Isocontour, Medium2_Isocontour, Medium3_Isocontour, High_Isocontour, Pcb_Temperature

Folders, Classes and Subclasses (III)

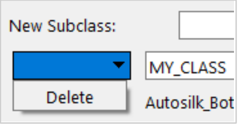
To add additional layers (subclasses) to a PCB, the desired class should be selected in the pull-down menu **Setup > Subclasses**. The name of the new subclass can be defined in subsequent windows.





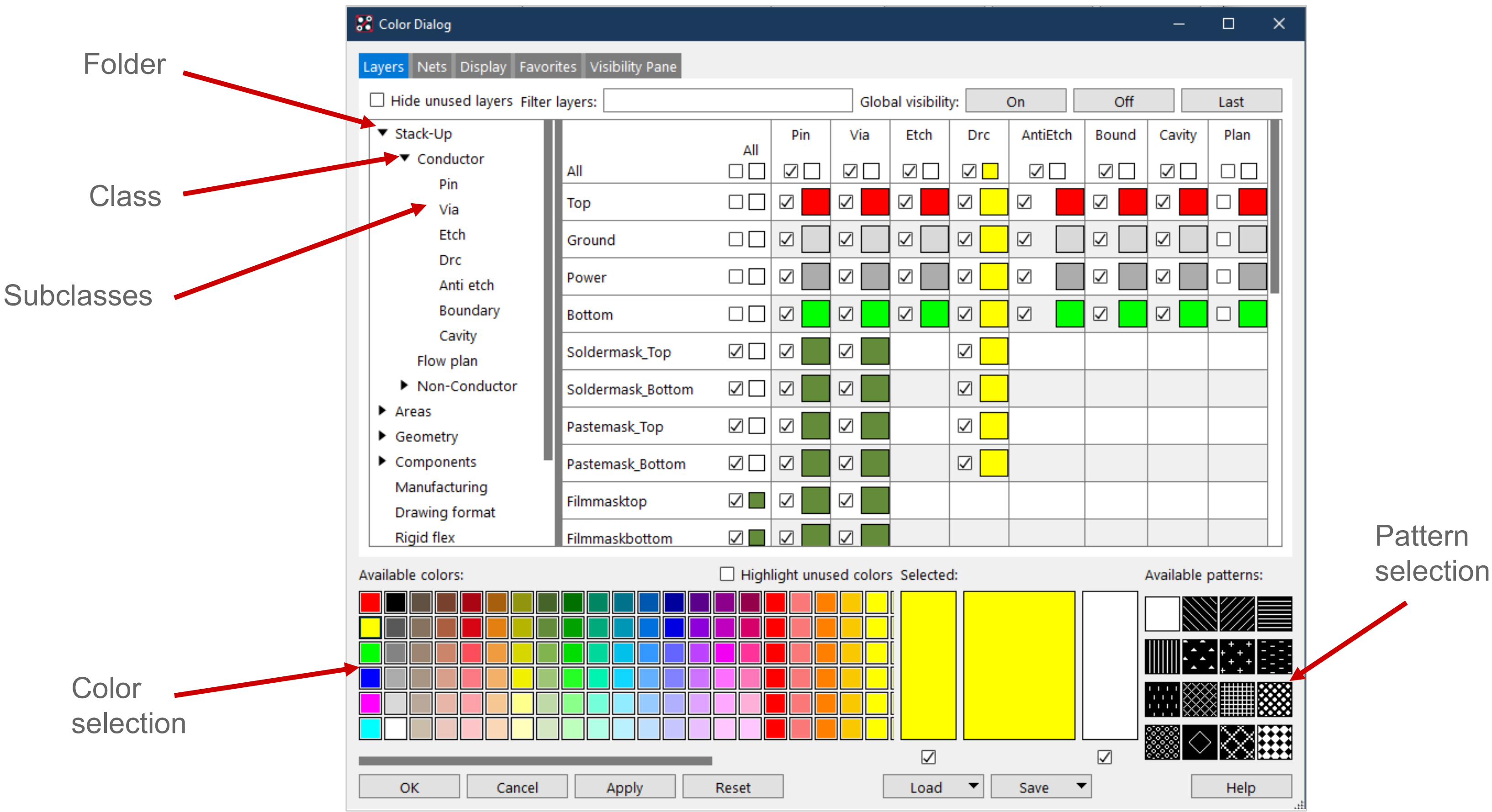
With exception of routing layers (Etch)
all user defined layers can be entered via these menus. When you choose **ETCH**, the Layer Stackup will be started automatically to define additional routing layers. More details on this topic at page 72.

All user defined layers have a white background to highlight user defined layers in menus. All other layers are default layers of the system. One click on arrow button will delete a user defined layer. Only layers without any data can be deleted.



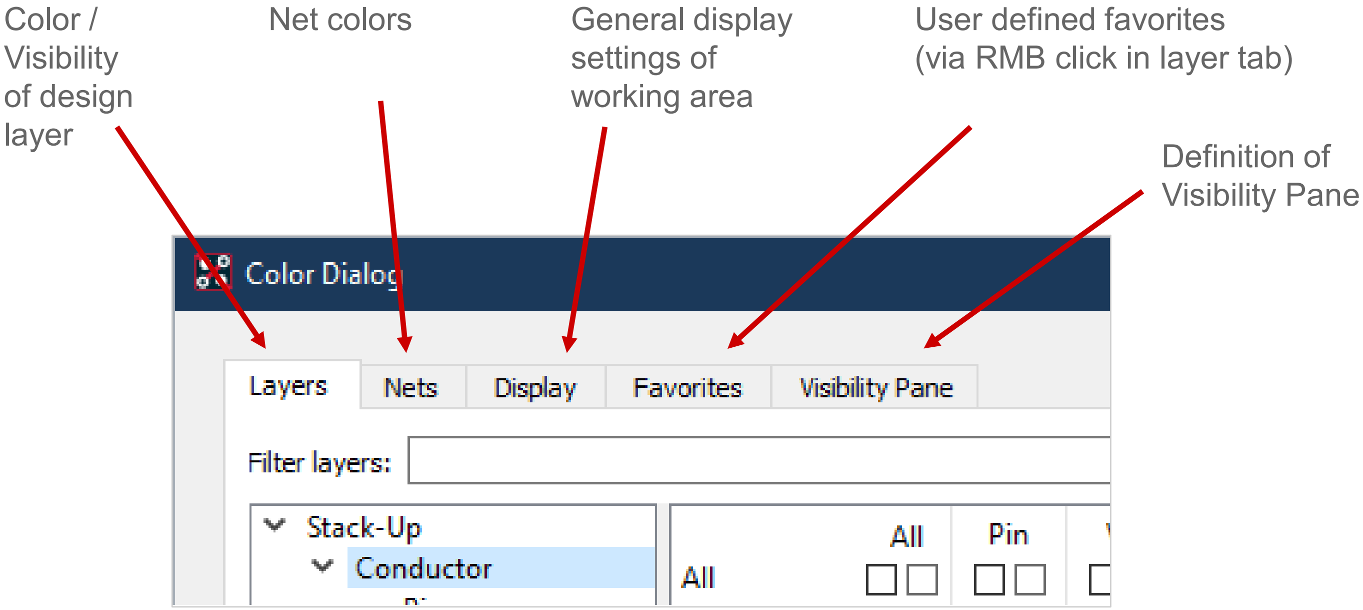
Control of Color and Visibility (I)

Via **Display > Color > Visibility** or visibility and color of individual layers (classes / subclasses) can be set.



Control of Color and Visibility (II)

Via **Display > Color > Visibility** or  visibility and color of individual layers (classes / subclasses) can be set.

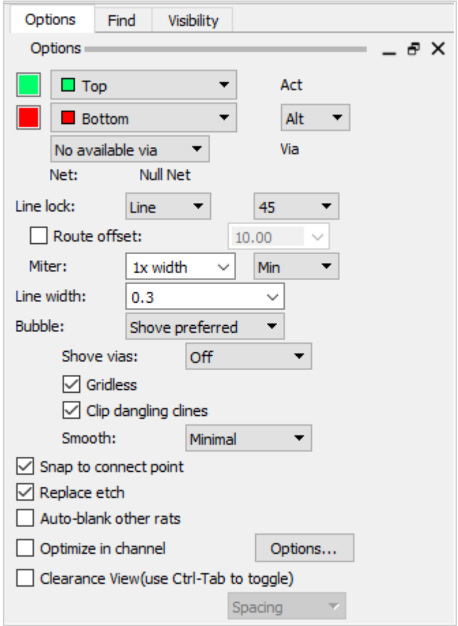


Tip
In display settings you also have functions like shadow mode and transparency for individual appearance of design.

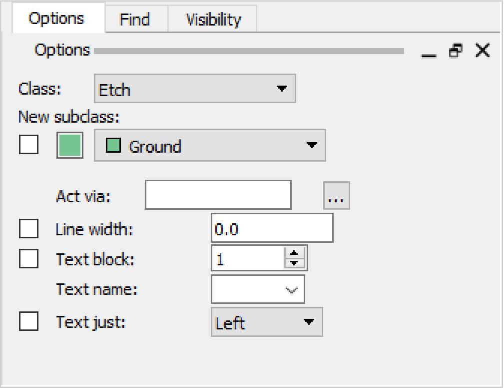
Option Window of Control Panel

The parameters in the option window depend on respective command and offer a variety of options for the commands. You should therefore always keep an eye on the Options window during interactive work.

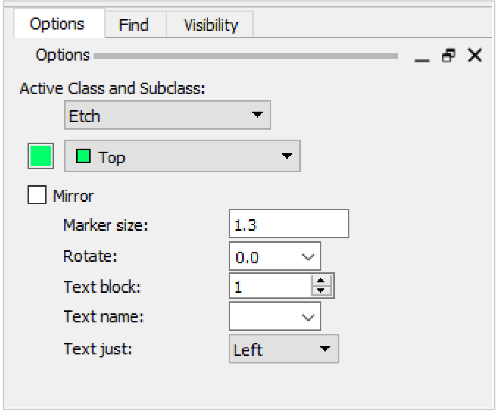
Route > Connect



Edit > Change



Add > Text

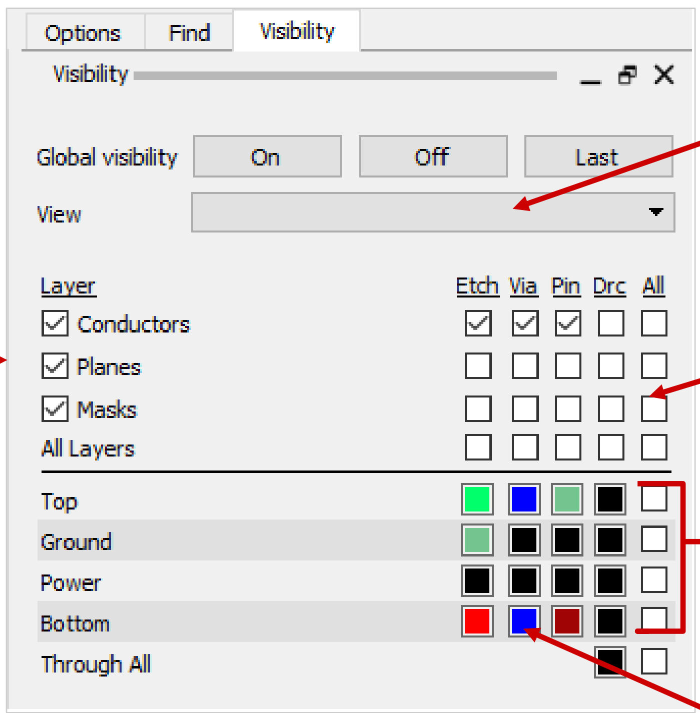


Changes take effect immediately and also overwrite pre-settings made in PCB Editor setup.
For example via **Setup > Design Parameters… > Design > Linelock / Symbol.**

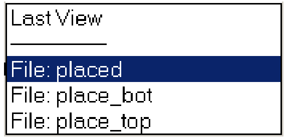
Visibility Control Panel

The Visibility control panel provides a fast method to switch single layers on or off. Layer control related to individual elements applies only to **copper and mask layers.**
For documentation layers, color dialog window  or user defined **color views** can be used.

Exclude / Include Layers



User defined color views



Control conductor, plane and mask layers

Individual layer control

Individual control of elements

User Preferences

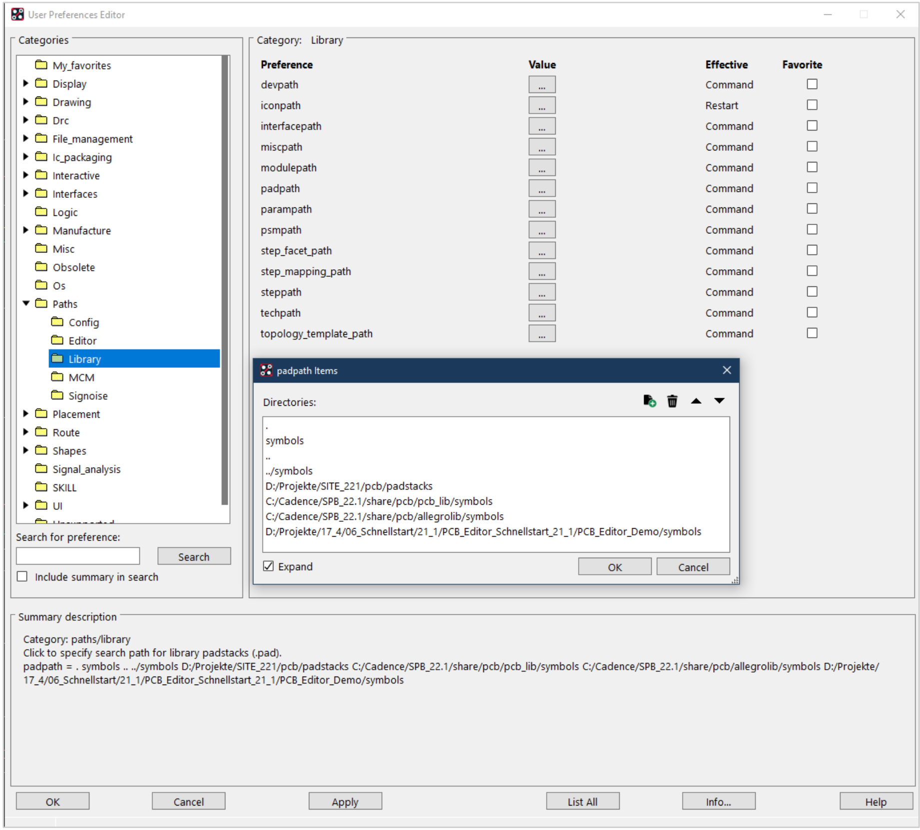
Via **Setup > User Preferences…** behavior and settings of the PCB Editor can be predefined.

The two most important settings are **psmpath** and **padpath**. Only if these are set properly, components can be placed from library.

The Picture shows default settings. These should not be modified at the beginning.

All PCB Editor default settings are stored to a file named **env** located under
< your_Installation > /share/pcb/text.

As soon as you open illustrated menu and perform a modification, a folder named **PCBENV** and a file **env** inside will be created in your home directory.
In this file you can define your individual aliases and function keys. This **env** file will be automatically loaded with every start of the PCB Editor.



Library

Library Elements

The libraries that are required for layout can contain different elements. A short overview and explanation regarding these elements is shown below.

- **Package symbol (.psm)** Footprint (DIP14, SOIC16, etc.), package symbol
- **Padstack (.pad)** Pad and drill definition of pins on each layer
- Mechanical symbol (.bsm) Mechanical symbol, i. e. spacer, predefined outline of a board with mounting holes
- Format symbol (.osm) Drawing frame for documentation, can not have pins
- Shape symbol (.ssm) Predefined Copper shape, i. e. for special pad shapes
- Flash symbol (.fsm) Copper shape for thermal ties on plane layers
- Board template (.brd) Board template with outline, technology (stackup, spacings, …) and more presettings

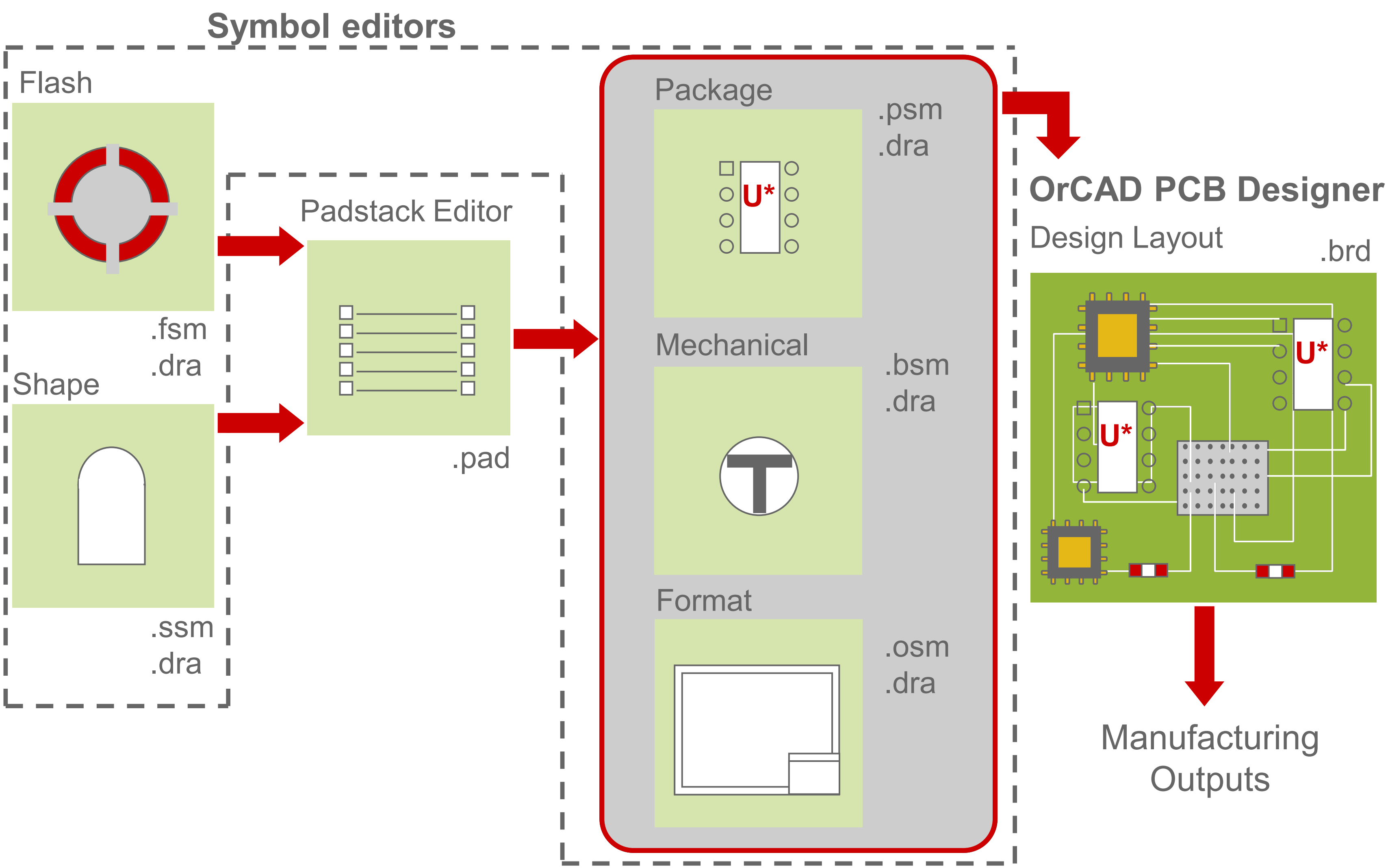
Padstack and package symbol are explained on following pages.

All listed symbols modified with **symbol editors** are edited and saved as .dra.
After compilation .psm, .bsm, .osm, .ssm, .fsm files are available to be used by PCB Editor.

All symbol editors are based on the PCB Editor and have the same use model. Only the function set is different.

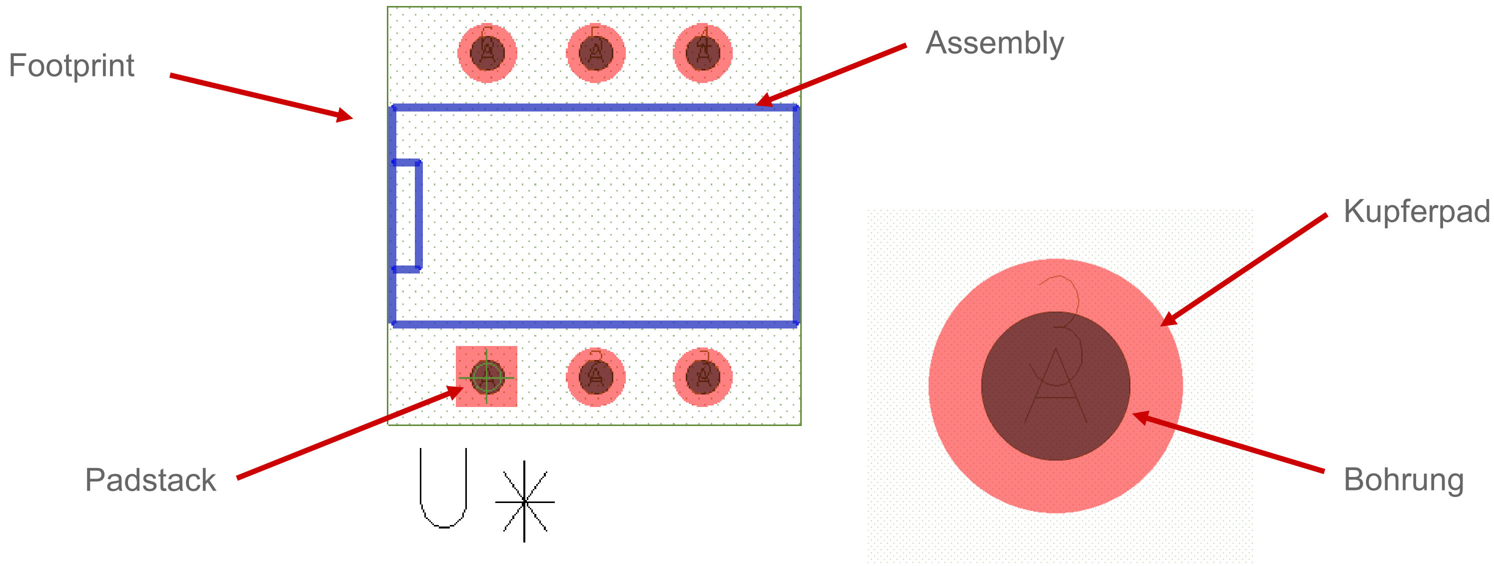
Since symbol type is part of .dra file, correct symbol editor will open for editing. There is a separate **Padstack Editor** for padstacks. You will find an overview of different symbol editors on next page.

Overview of Editors



Footprint as a Basic Symbol

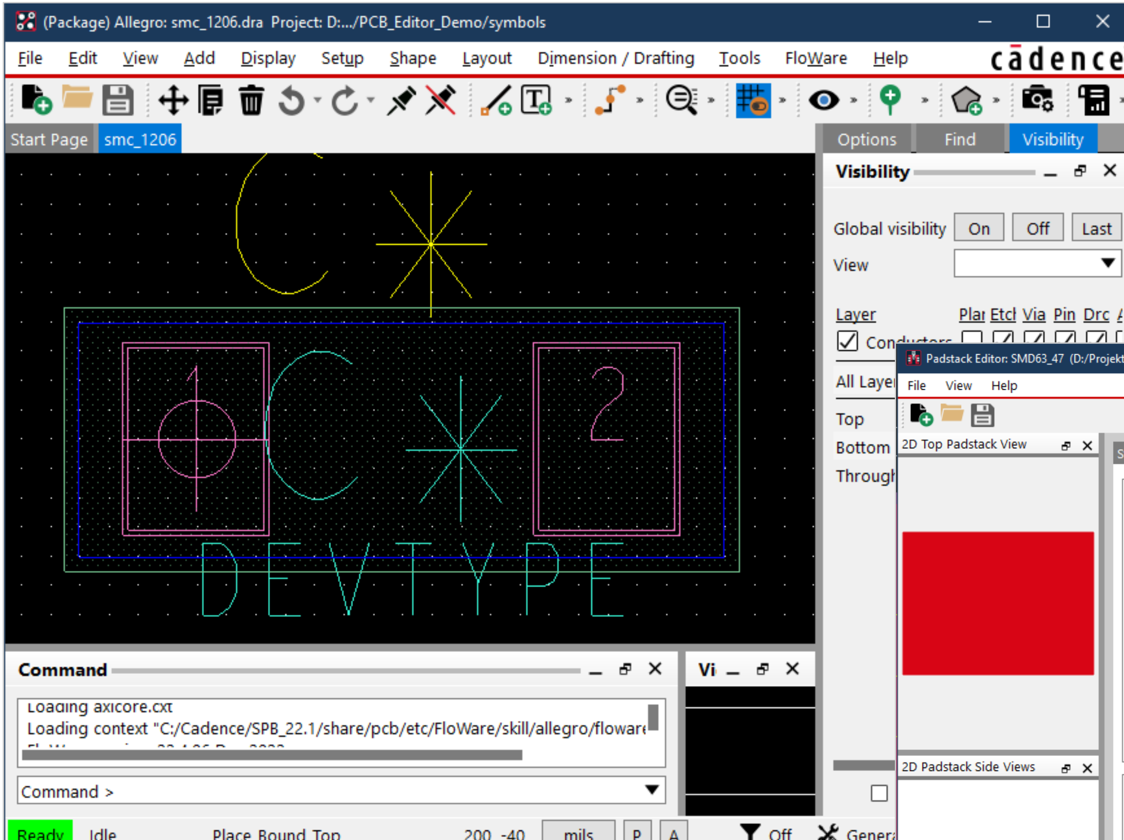
Symbol editors are used to create necessary layout library elements.
Most important element – the **footprint** – will be representative example.



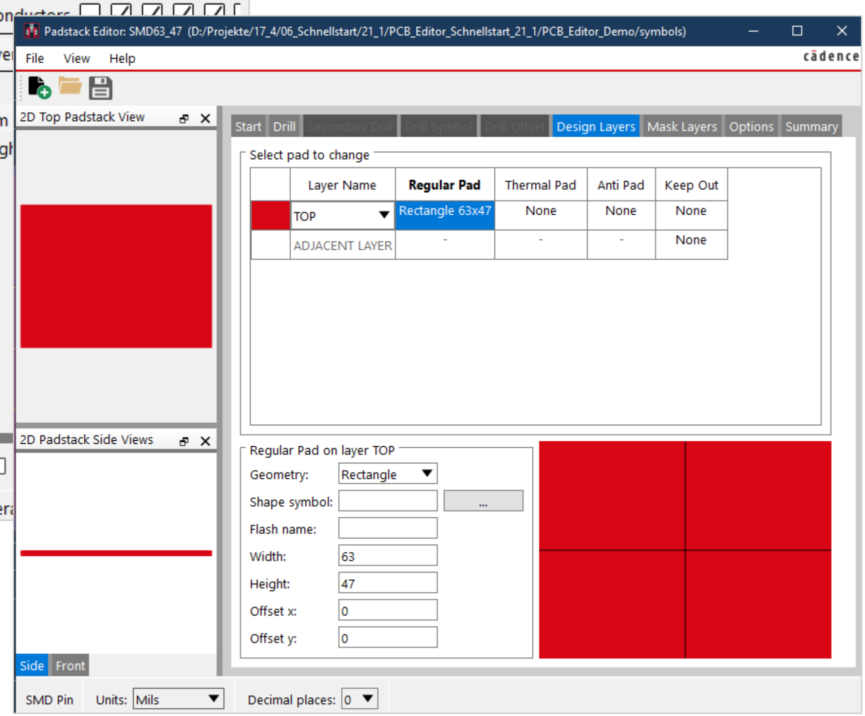
There are also pure graphic symbols for documentation or production purposes (company logos, drawing frames, adjustment markers), which can also be created using one of the symbol editors.

Library Tools

Symbol Editor



Padstack Editor



Padstacks

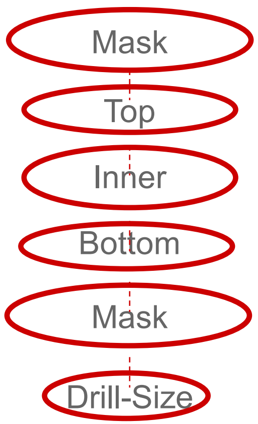
Padstack (Structure)

Most important element of a footprint is padstack.

A padstack contains geometric shape of a pad on every layer of a board as well as drill diameter for thru hole components.

There are basically two types of padstacks:

Through-Hole Padstack



Surface-mount Padstack

Definition of pad size for all layers (electrical or nonelectrical) is done in Padstack Editor. Electrical layers are all signal and plane layers.

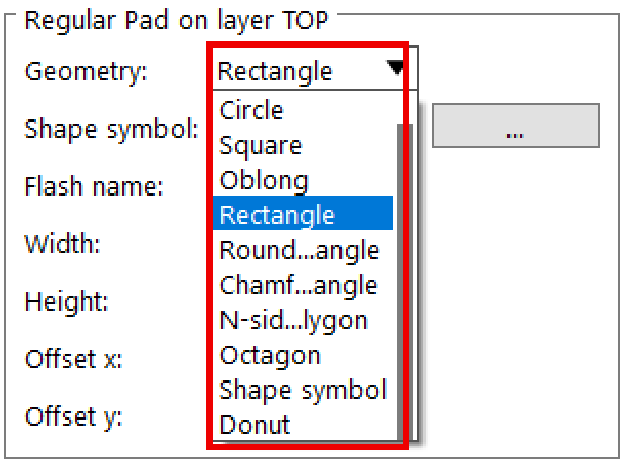
Nonelectric layers are solder mask, paste mask and film mask. Film mask can be used for multiple purpose.

Default routing layers are BEGIN Layer, DEFAULT INTERNAL and END Layer.

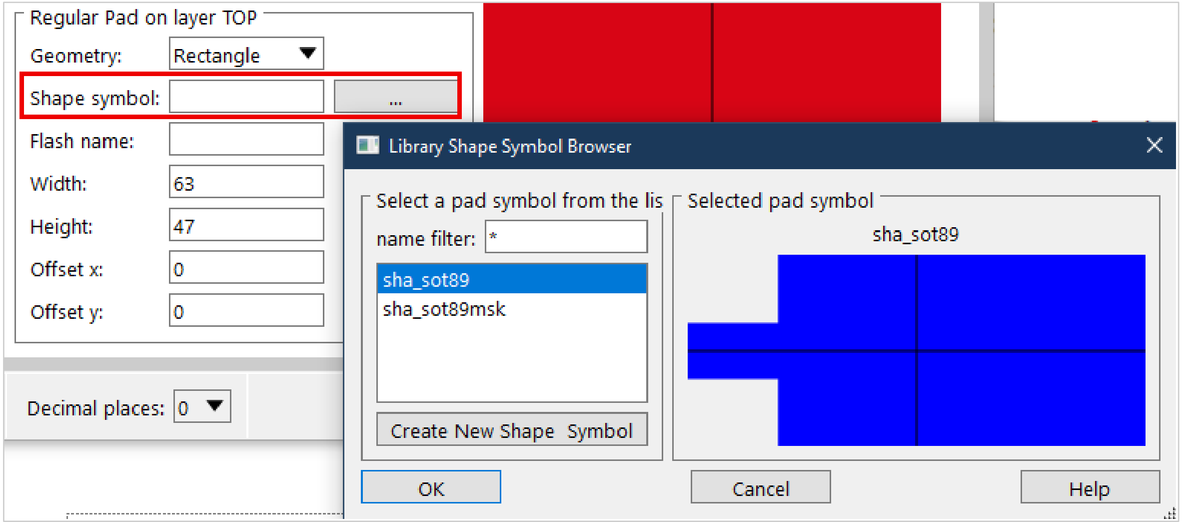
The DEFAULT INTERNAL definition is used for additional inner layers besides top and bottom.

Padstack (Details)

- **Regular Pad**
  A pad with a regular shape (circle, square, rectangle, oblong, octagon) as available in the dropdown.



- **Shape Symbol**
  If pad geometries not available in the dropdown are to be used, they can simply be drawn as a shape.



Pad Designer – Start

There are two ways to start the Padstack Editor:

- **Start > Cadence PCB Utilities > PCB Editor Utilities 2022 > Padstack Editor 2022**

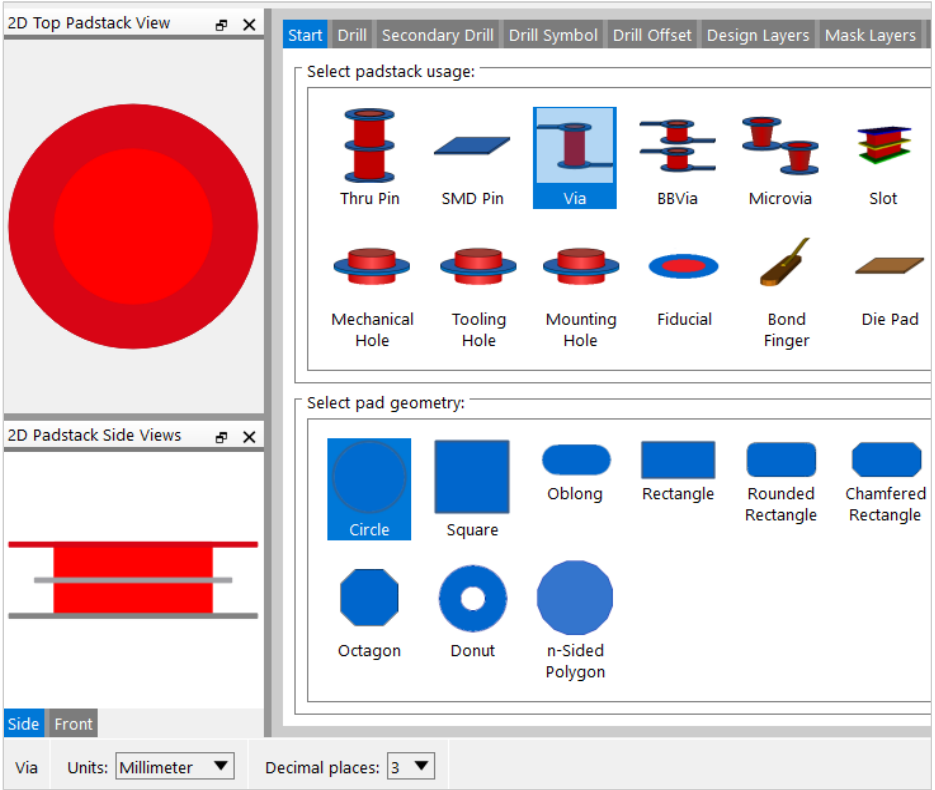
or directly from the PCB Editor resp. symbol editor:

- **Tools > Padstack > Modify Design / Library Padstack…**

On **start** page you can choose different padstack types.
Based on selection next tabs are available and prepared.

Preview top

Preview side view

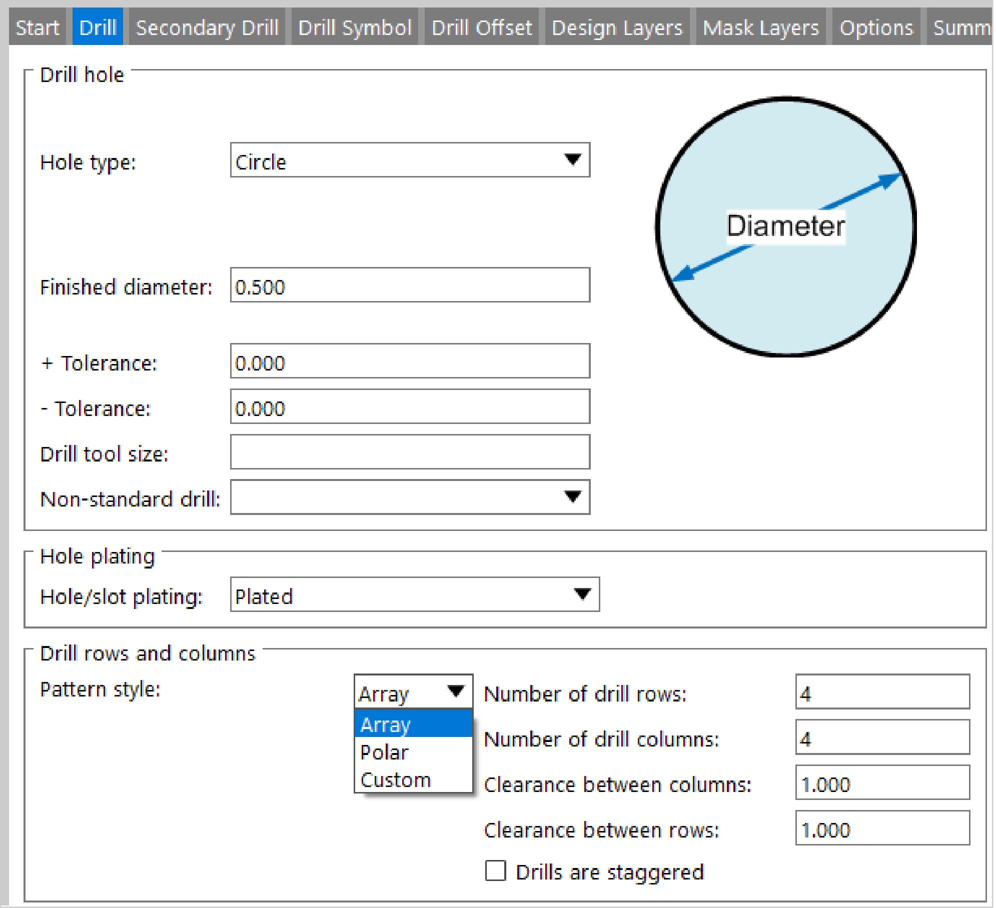


Pad Designer – Drill

In tab **Drill** you have access to all necessary settings to define drill holes.

In addition to drill diameter and tolerances, drill type (e.g. laser) can also be specified.

Furthermore, it is possible to define drill matrices.

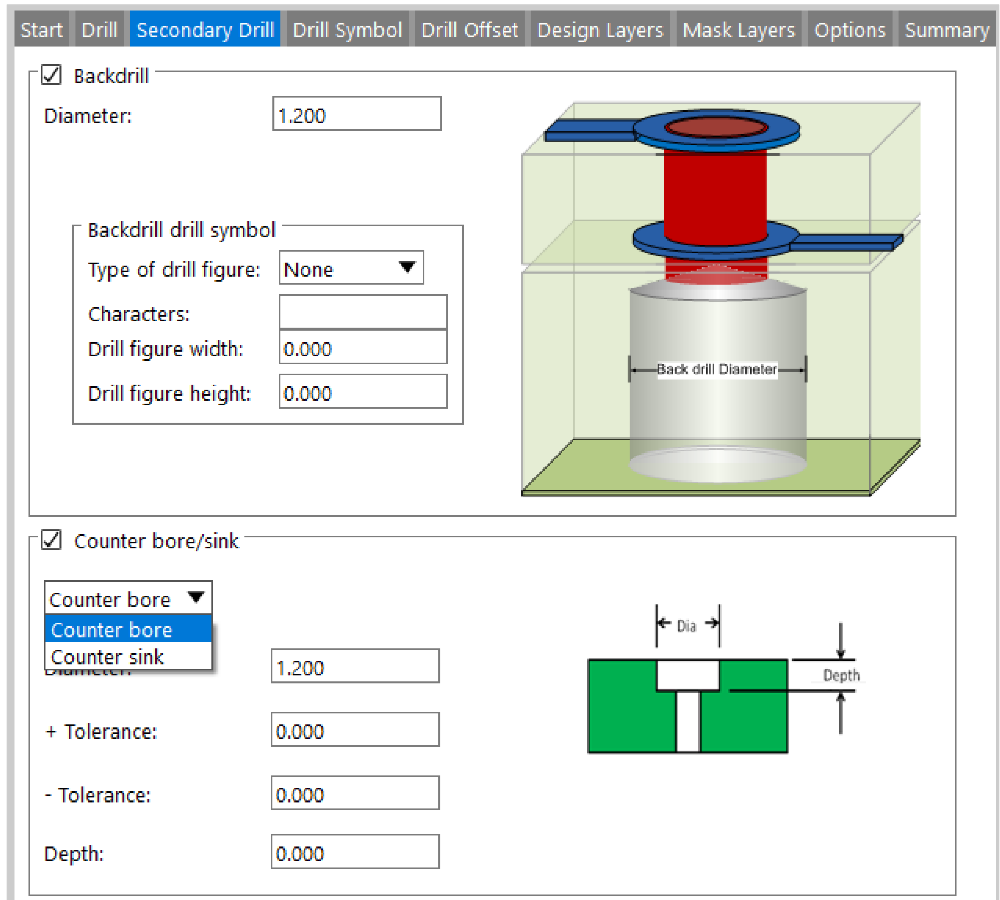


Pad Designer – Secondary Drill

In tab **Secondary Drill** you can define all necessary settings for Secondary Drill and Backdrilling.

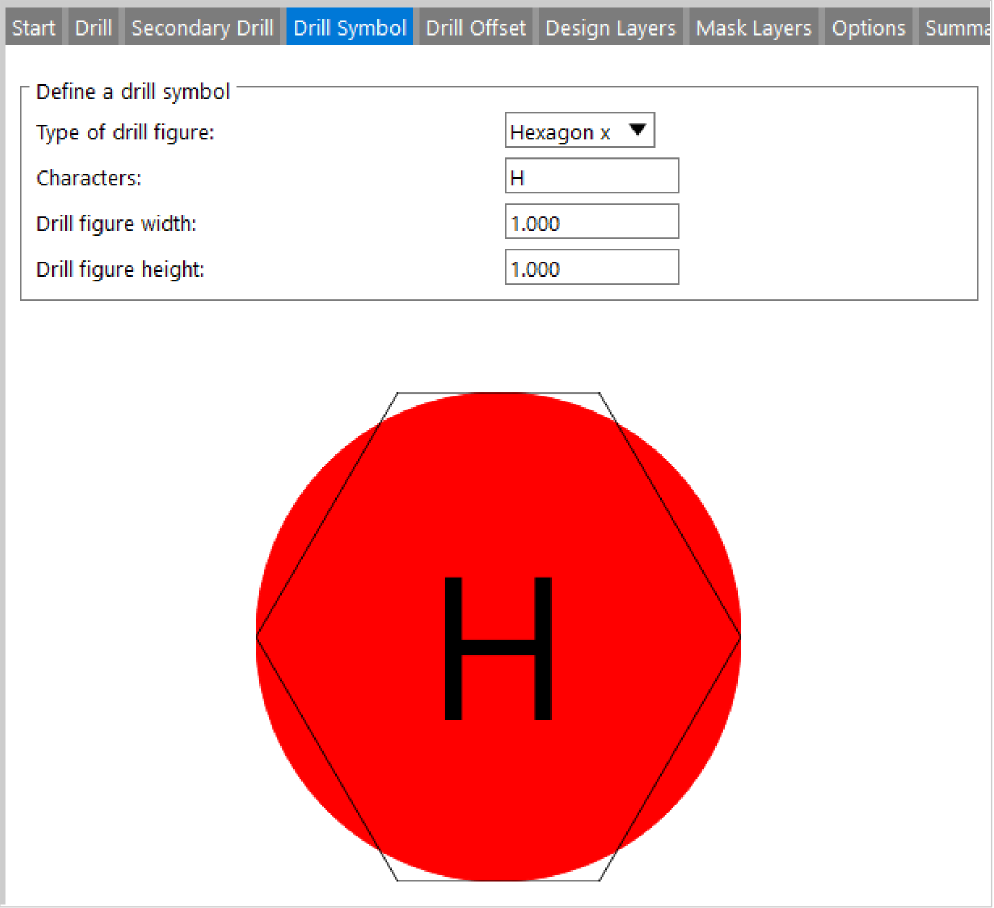
In addition to diameter and tolerances it is possible to define an individual symbol for backdrills.

In addition, as of OrCAD Professional, it is also possible to define backdrilling.
The backdrilling process will not be discussed further in this quick start.



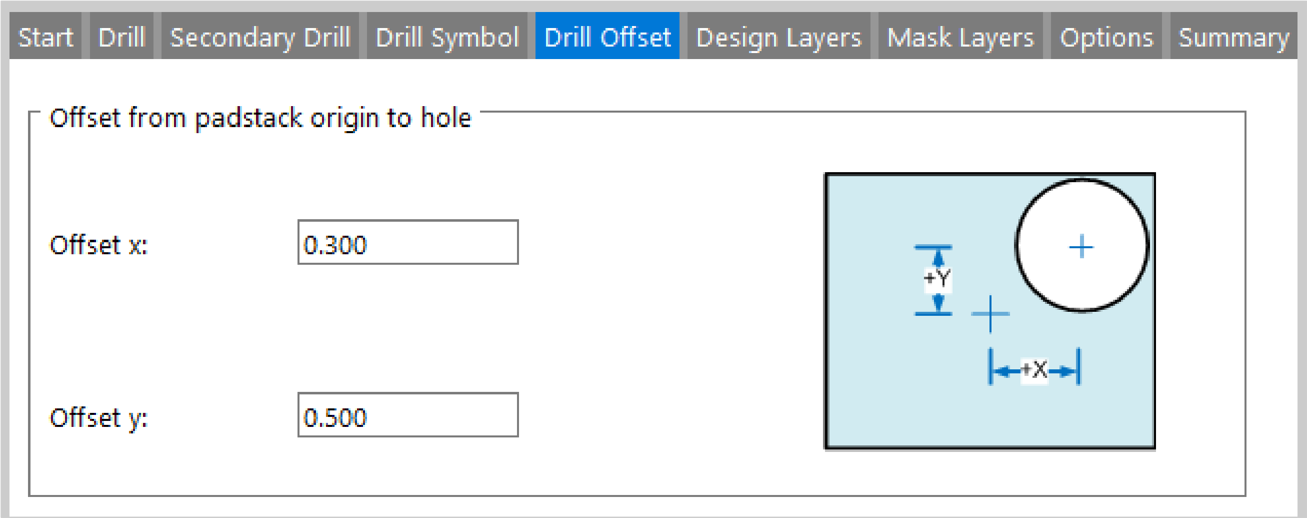
Pad Designer – Drill Symbol

In tab **Drill Symbol** you can define drill symbols for drill table on manufacturing documentation.



Pad Designer – Drill Offset

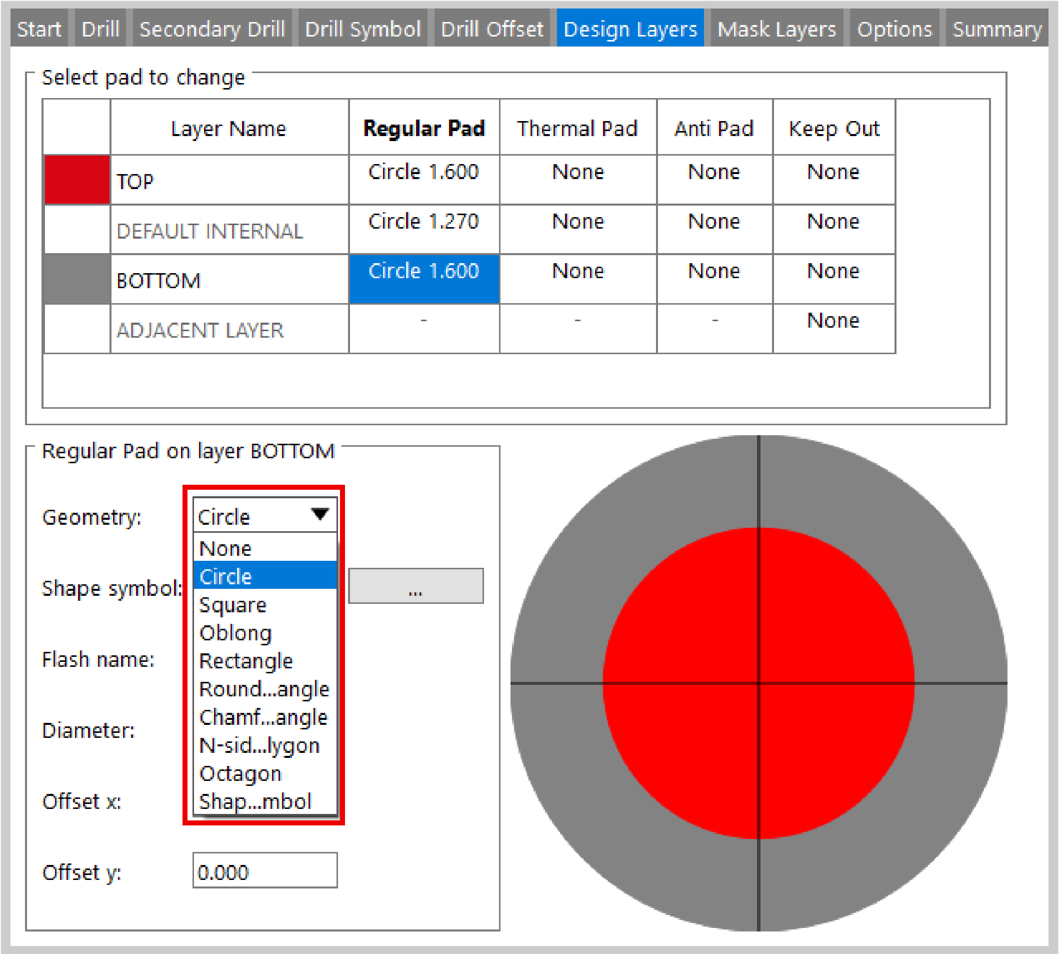
In tab **Drill Offset** you can define an offset between pad and drill hole.



Pad Designer – Design Layers

In addition to tabs for defining holes, **Design Layers** tab is most important in Padstack Editor.

Copper pads are defined here. Different geometries can be selected and the associated dimensions defined.

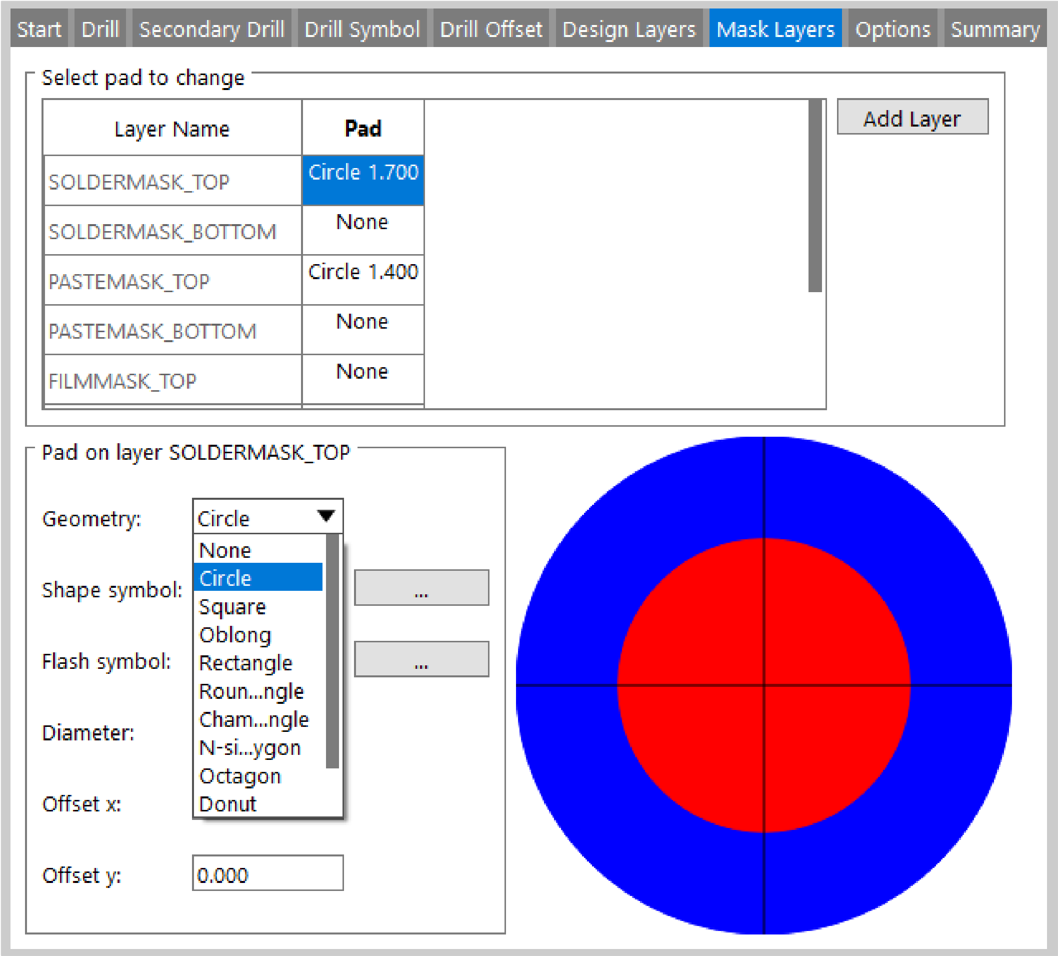


Note
In the Design Layer tab it is also possible to define thermal and antipads. These are no longer needed nowadays because they are only used on negative copper layers.

Pad Designer – Mask Layers

In tab **Mask Layers** you can define different mask layers.

In addition to gap in solder resist, you can define solder paste and if necessary, gaps for other mask layers.



FlowCAD

Pad Designer – Options / Summary

In **Options** tab more additional options are bundled.

Summary tab shows a summary of different layers, drills and additional settings. For documentation purpose this summary can be also exported in html.

Start | Drill | Secondary Drill | Drill Symbol | Drill Offset | Design Layers | Mask Layers | Options | Summary

Design layer pads

Layer: TOP

Pad	Geometry	Width	Height	X offset	Y offset
Regular	Rectangle	63	47	0	0
Thermal	None				
Anti	None				
Keep Out	None				

Layer: ADJACENT LAYER

Pad	Geometry	Width	Height	X offset	Y offset
Regular	None				
Thermal	None				
Anti	None				
Keep Out	None				

Mask layer pads

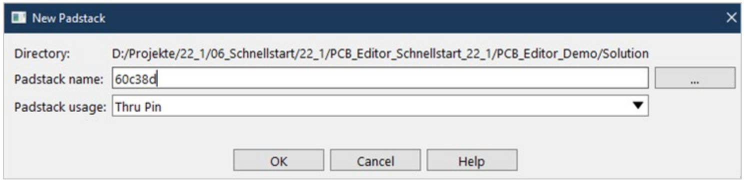
Layer	Geometry	Width	Height	X offset	Y offset
SOLDERMASK_TOP	Rectangle	67	51	0	0
SOLDERMASK_BOTTOM	None				
PASTEMASK_TOP	Rectangle	63	47	0	0
PASTEMASK_BOTTOM	None				
FILMMASK_TOP	None				
FILMMASK_BOTTOM	None				
COVERLAY_TOP	None				
COVERLAY_BOTTOM	None				

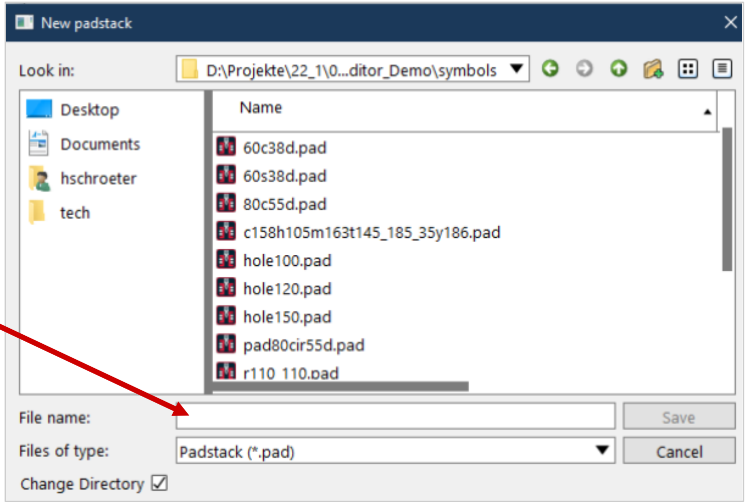
Save | Print

Lab: Padstack (Start)

Next, we will show the steps to generate a through hole padstack.

1. **Start > Cadence PCB Utilities > PCB Editor Utilities 2022 > Padstack Editor 2022**
2. **File > New** in Padstack Editor
3. Browser window on the right will appear.
4. Navigate with browser button to your target folder (in this case **Play**).
5. Enter padstack name **60c38d**.
6. Activate change directory box. The chosen directory will be your working folder.
7. Please **save** new padstack.
   By selecting check box under 5., the Play directory will become the current working folder.
8. Headline of Padstack Editor shows name and path.

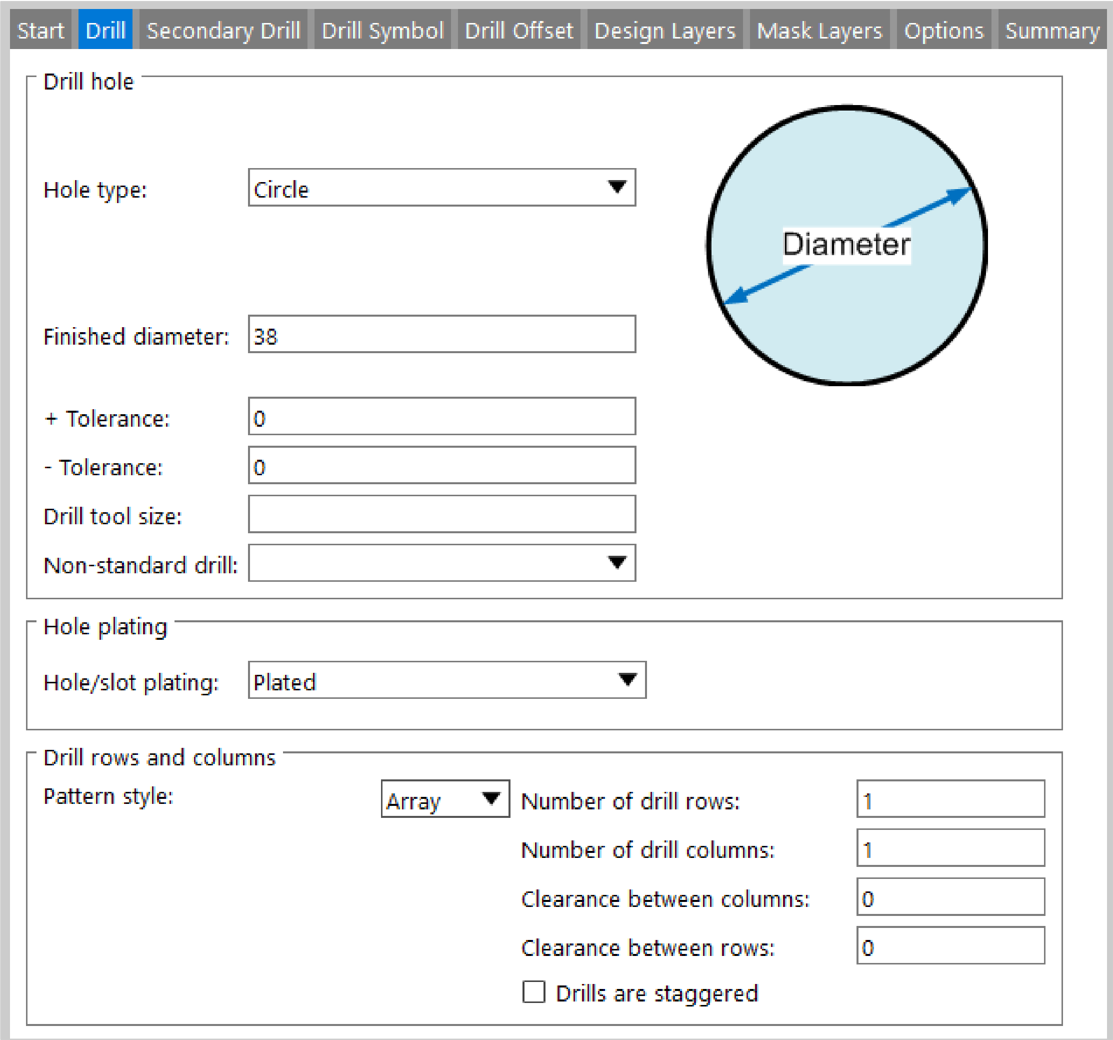




Note
Naming convention of Cadence is referenced to units in mil:
60c = 60 mil circle; **38d** = 38 mil hole (final diameter); in addition: **r** = rectangle; **s** = square; **o** = oblong
This notation is used for all padstacks delivered by Cadence and is easy to recognize.

Lab: Padstack (Drill)

Please enter values from the picture into **Drill** tab.



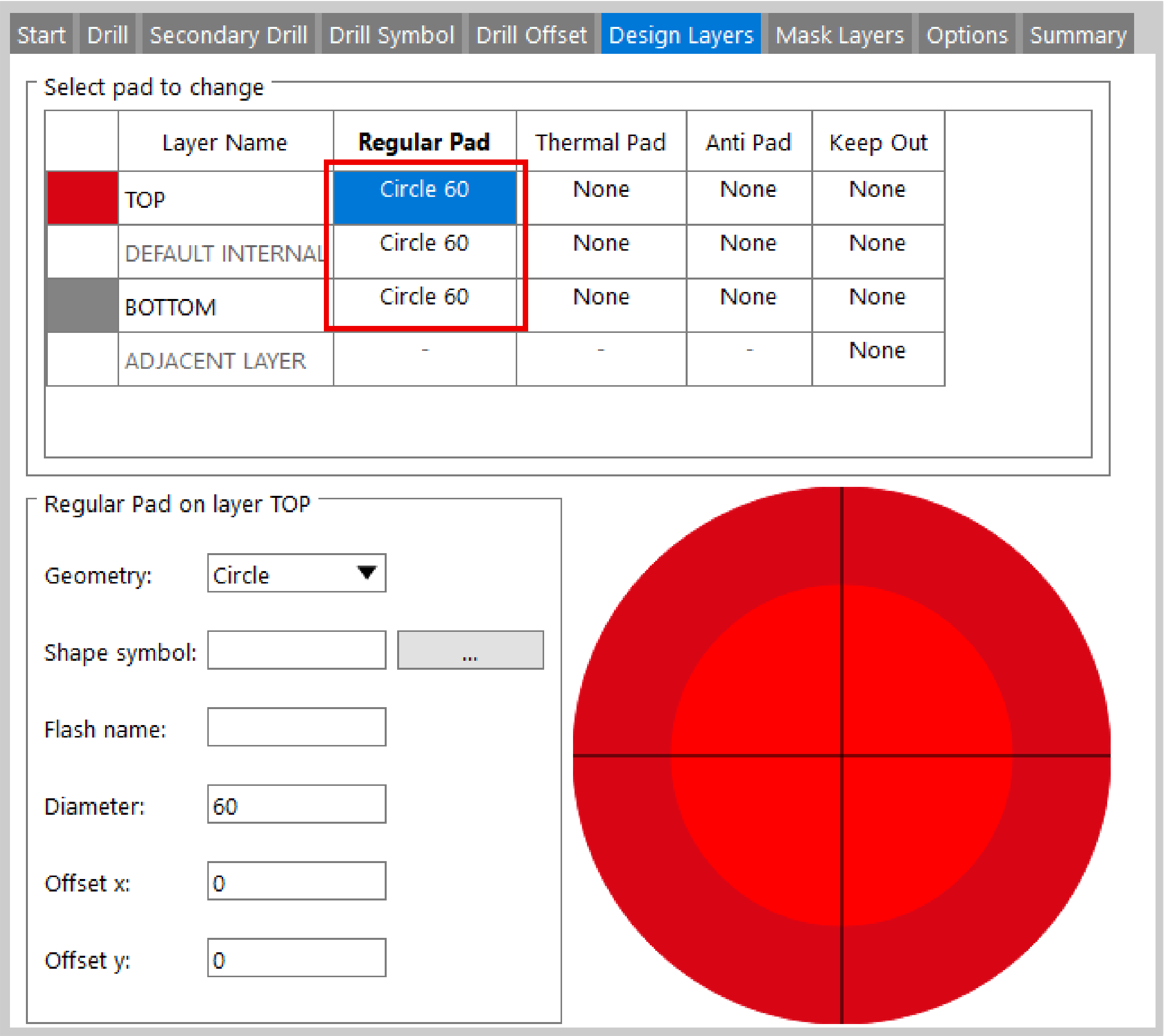
Tip

To ensure to enter all necessary entries, please move from left to right through all tabs.

All unused tabs of a padstack type are grayed out.

Lab: Padstack (Design Layers)

Please enter values from the form into **Design Layers** tab.

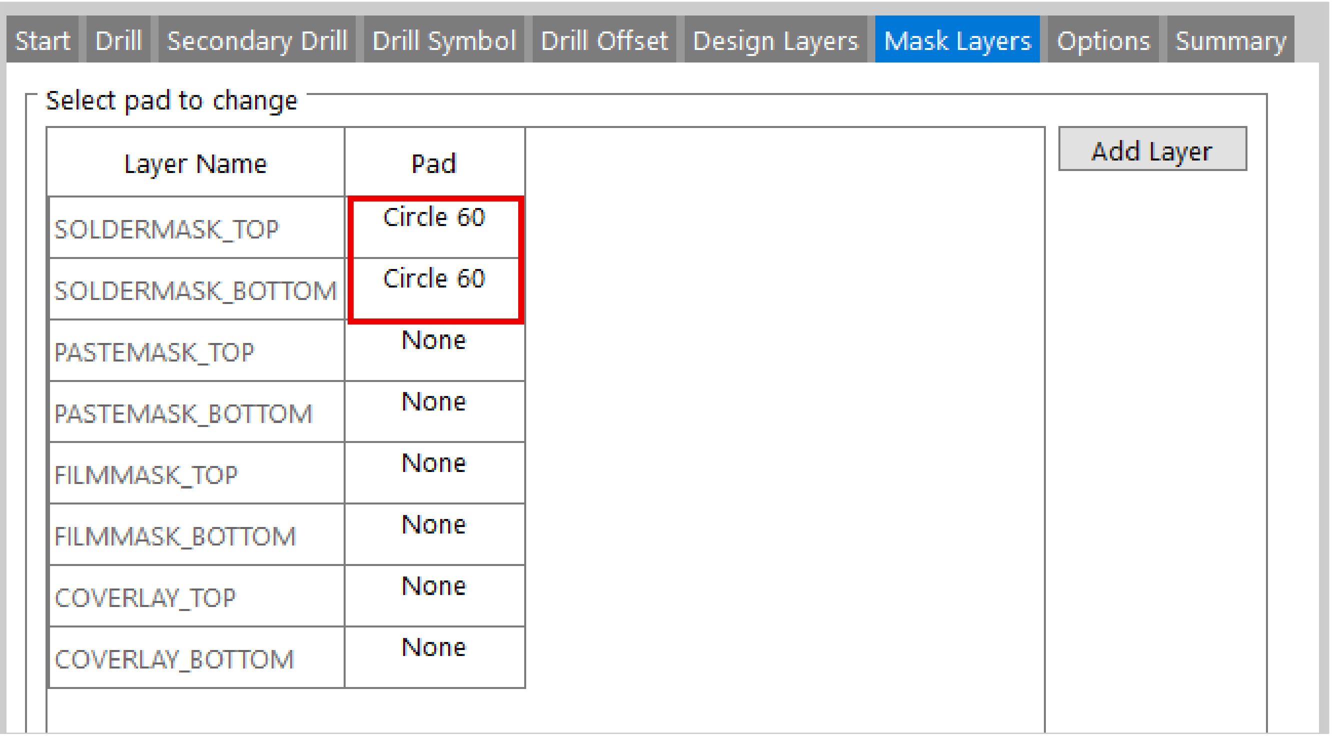


Tip

With right mouse button via copy / paste, pads can be copied from one to another layer within a tab.

Lab: Padstack (Design Layers)

Create corresponding pads also in **Mask Layers** tab.



Symbols

Overview Footprint Design Process

Creation of a new footprint includes following steps:

- Definition of units, decimal places and size of workspace
- Definition of origin. This is typically base point of component during placement
- Grid definition (does support easier curser positioning)
  Via keyboard any complex value can be entered
- Placement of pins (predefined padstacks)
- Assembly and silkscreen outline definition
- Definition of occupied component area for placement (Placebound_Top/Bot)
- Entry of possible height constraints of placebound_Top/Bot
- Addition or modification of component Text like REFDES or DEVICETYPE
- Saving in desired library

These steps are illustrated on next pages. Our example component is a transformer. The data sheet of it can be found in PCB Editor Demo folder and is named **Datenblatt_Trafo.pdf.**

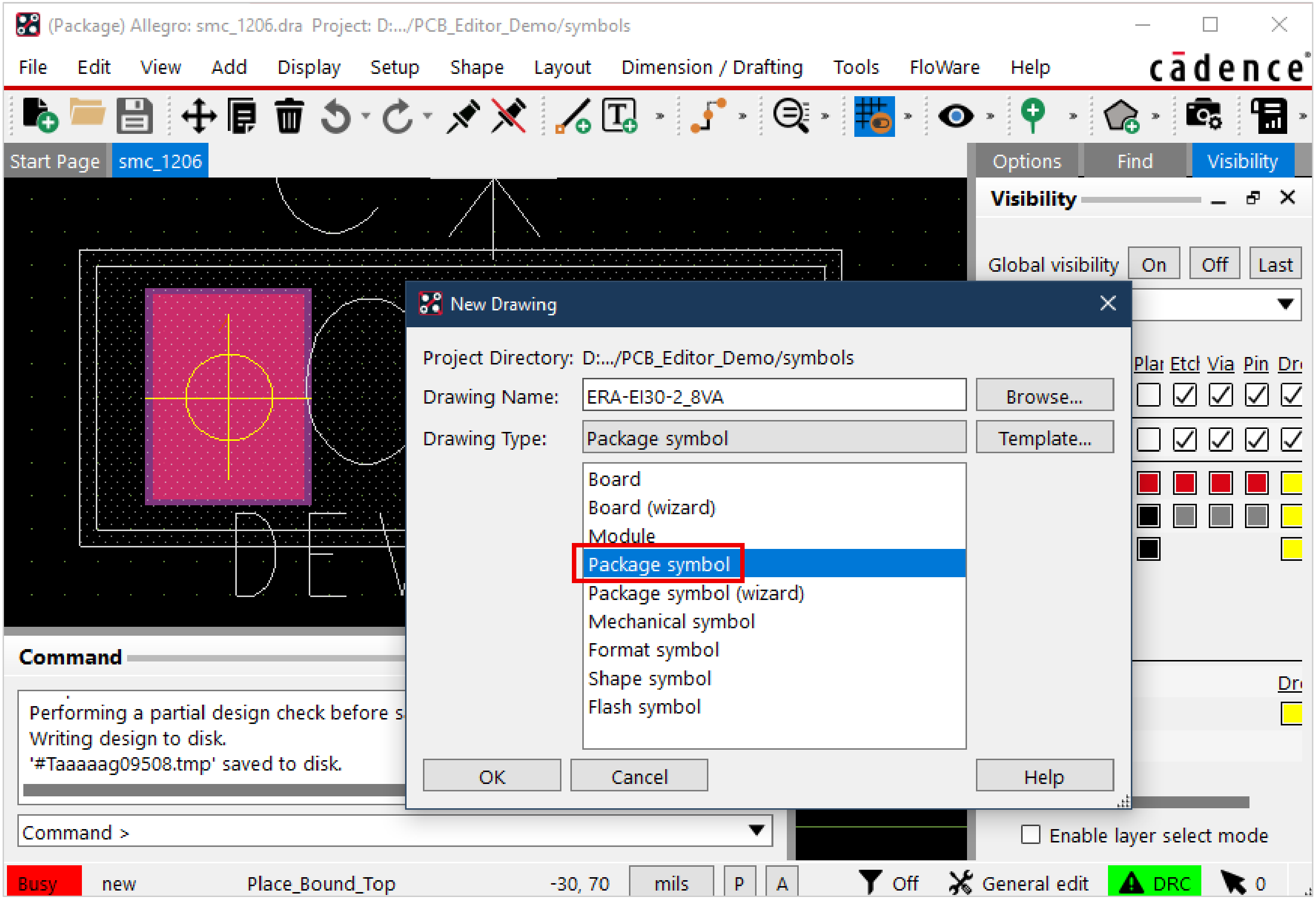
Lab: Symbol (Start)

Package Symbol Editor can be opened from an already opened PCB Editor via **File New > Package Symbol**. In form you can enter name of a new footprint.

Please enter name

ERA-EI30-2_8VA

as an example and use **Browse** to save in folder **Play**.



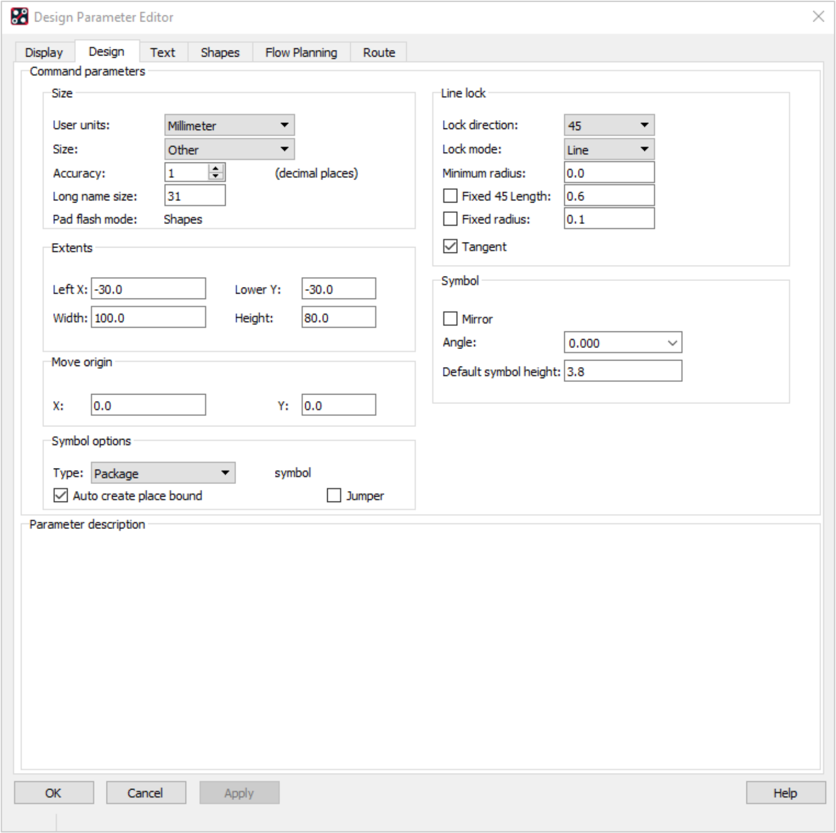
Lab: Symbol (Setup)

In **Setup > Design Parameters…> Design** you can set units, decimal places and size of workspaces as well as origin.

Move Origin allows to move the origin to a different location. The size of the workspace stays untouched. The origin can also be moved with the mouse via **Setup > Change Drawing Origin.**

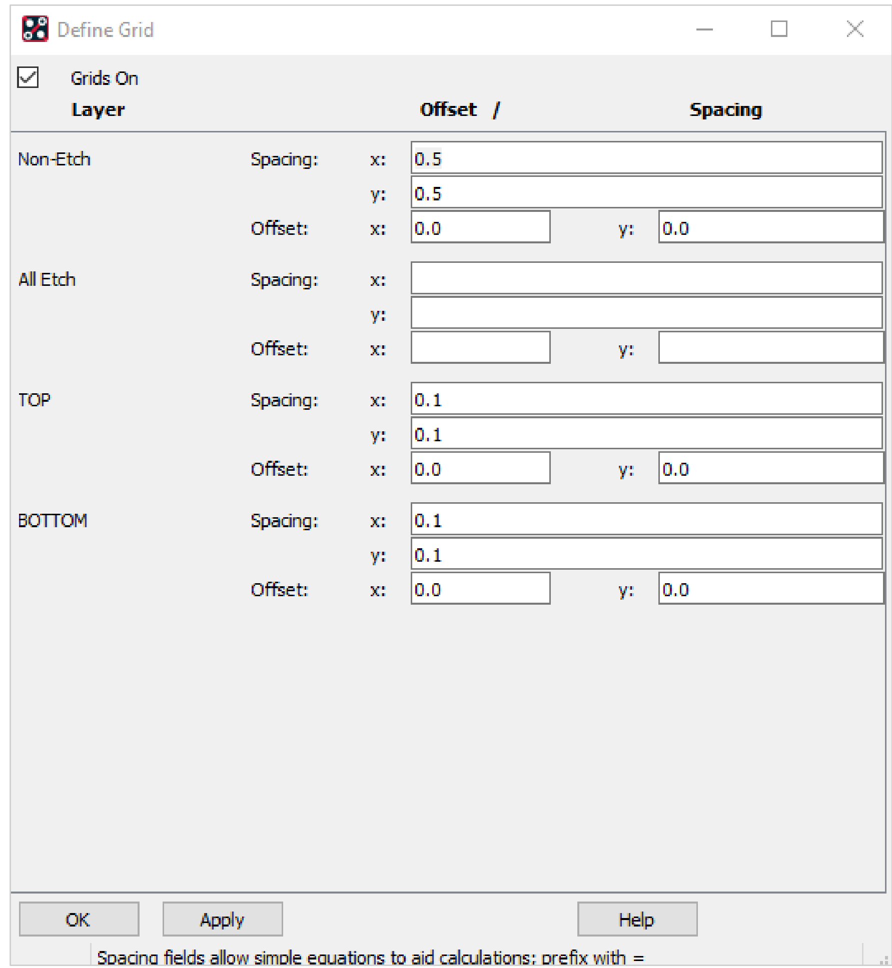
Please use following values for the example:

- Units: Millimeter
- Size: Other
- Accuracy: 1
- Left X: -30.0
- Lower Y: -30.0
- Width: 100.0
- Hight: 80.0



Lab: Symbol (Grids)

With **Setup > Grids…** you can define grid.
For our example please use values from form on the right.



Tip

There are two separate grid definitions:

- **Non-Etch** for documentation layers
- **All Etch** for routing layers

X and Y can be different.

Etch layers (top, bottom and other inner layers) can also use different grids.

Lab: Symbol (Pins I)

Please note that per default Symbol Editor implies top view.

1. Via **Layout > Pins** you can add pins.

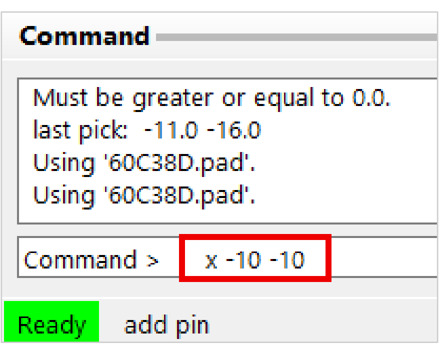
All pins will be added as **Connect Pins** since they have an electrical function.

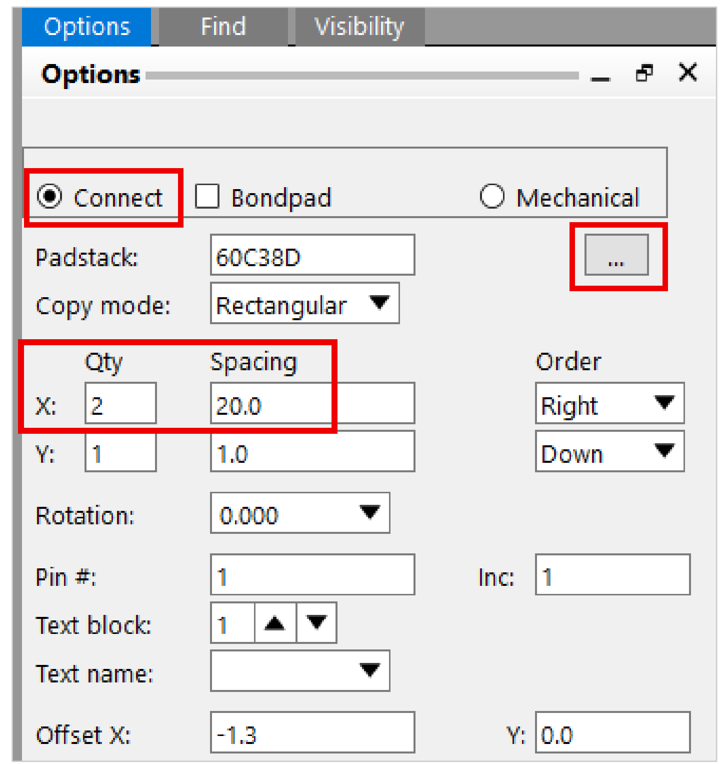
We choose a padstack using the browser from a preexisting library.

A matrix of pins can be set by specifying a quantity and the corresponding spacing. In this lab we limit ourselves to 2 pins.

The pins can be set by clicking in the workspace or by entering coordinates.

The easiest and most accurate way is to enter coordinates **X -10 -10** in the command window and **Enter**.

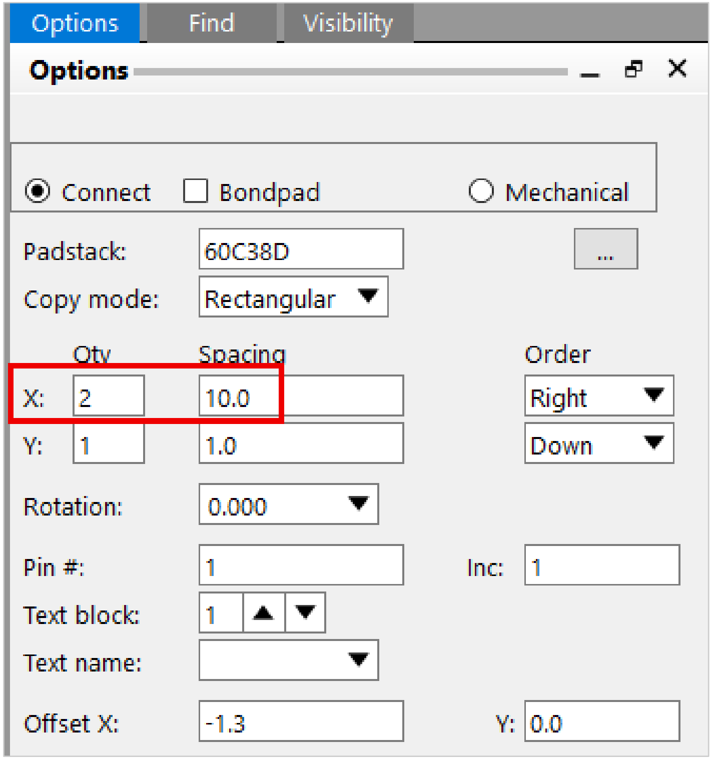




Lab: Symbol (Pins II)

Please follow instructions to place additional pins (2 to 5 and 6 to 10) as mentioned in data sheet.

2. **Add Pin** command is still active and pin 3 is on curser, ready for placement.
3. We repeat the lab for the two upper pins.
4. The first of the two pins is to be set to **x -5 10**.
5. Finish the command with **RMB > Done**.



Lab: Symbol (Pins III)

According to data sheet and schematic, only pins 1, 5, 7, 9 are required for the transformer.

1. Rename the pins according to the data sheet with **Edit > Text**.
   Pay attention to the Find Filter.

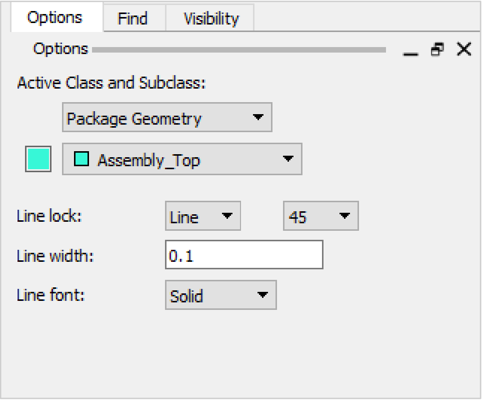
Tip

Another way to get the correct pin numbering is to set complete pin rows and delete the superfluous pins.

Lab: Symbol (Assembly Outline)

In the next step we add an **Assembly Outline** typically used for assembly drawings. To make the drawing task easier, the grid should not be chosen to large or to small.

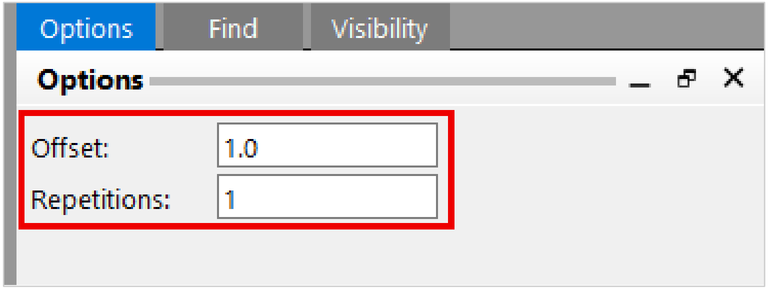
1. **Setup > Grid**, Grid window will appear.
2. Please enter in Non-Etch section for **x** and **y** e.g. **0.5**. Please note that values represent chosen units of editor. We work with millimeter.
3. Click **OK.**
4. Zoom out to see entire work area for assembly outline.
5. Please choose **Add > Line** to draw a polygon. Please ensure that correct active layer is chosen in options window. Value for line width stands for line width in the later documentation. Line width 0 would not appear in output. Please enter a meaningful value, e. g. 0.1.
6. Draw a rectangle with dimensions X=33 und Y=28 (0.5 mm got added for assembly tolerance).
7. Click after another **LMB** on **-15 -13, 15 -13, 15 13, -15 13, -15 -13**
8. Click **RMB** and **Done**.
9. You can enter values via command line, **x -15 -13, x 15 -13, …**

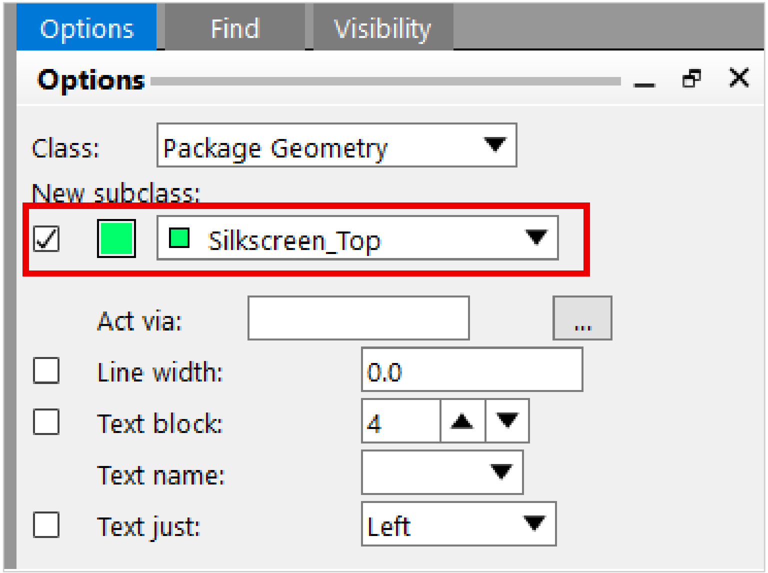


Lab: Symbol (Silkscreen Outline)

In the next step we will add the **Silkscreen Outline**.

1. Easiest way to do this is via **Dimension / Drafting > Add Parallel Line**.
2. Set the desired offset and the repetitions in the options.
3. Then we change the layer via **Edit > Change** to the correct subclass. Please make sure that only the check mark **New Subclass** is set.



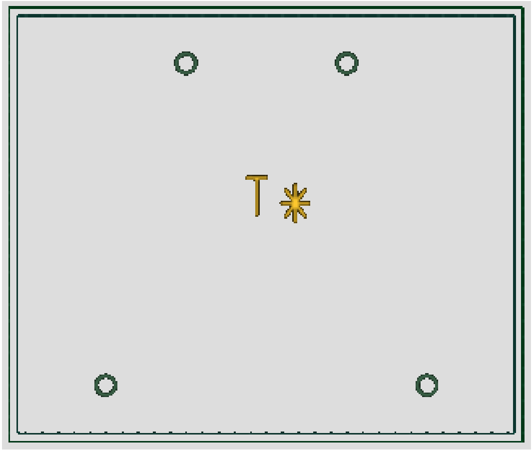


Lab: Symbol (Placeholder)

The label **REFDES** is required for every footprint.

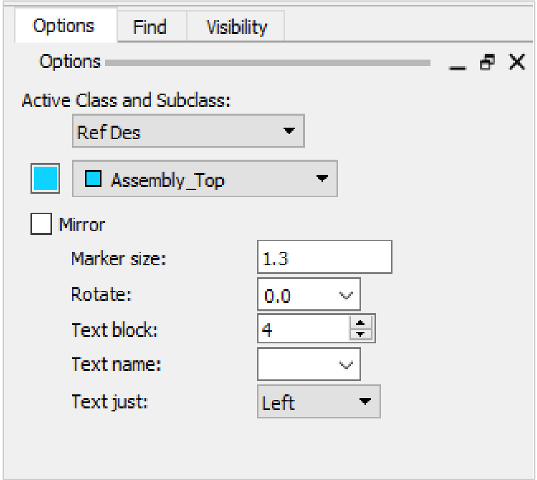
Definition of multiple placeholder for labels does make sense. They are used to show logic information. In PCB Editor it is possible to define five labels max.:

- REFDES (reference no. of component, R1, C2, etc.)
- DEVICE (device name from Packager)
- VALUE (value of component, e. g. 10 K for a resistor)
- TOLERANCE (tolerance, if provided)
- PART NUMBER (part number for BOM)



1. **Layout > Labels > REFDES**

   Please notify settings for necessary layers.
   System will ask for desired position.
2. Click inside of assembly outline.
   System will ask for a text string.
3. Enter as an example a **T*** .
   This string will be replaced by the real REFDES later.

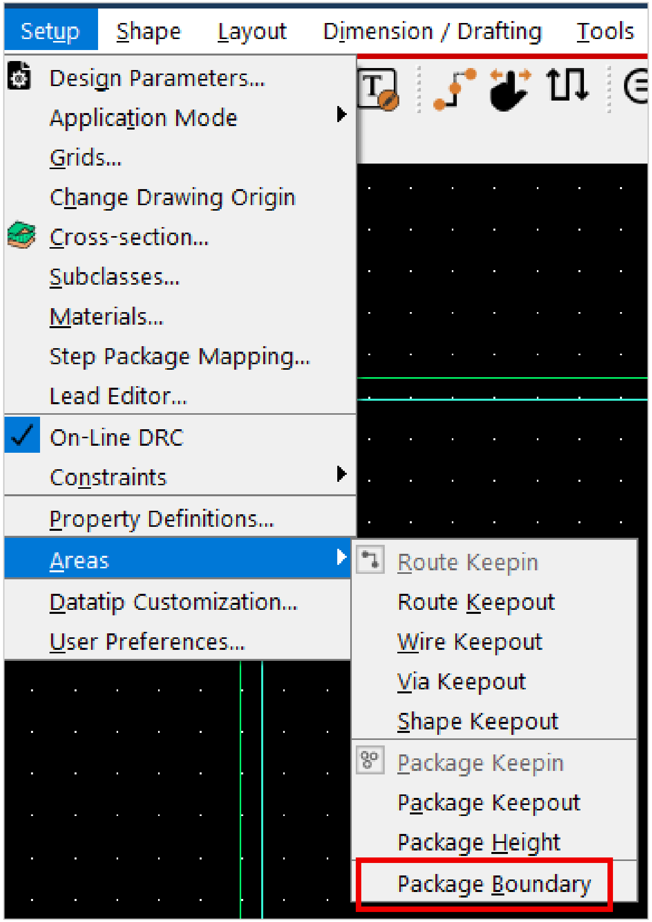


Tip
Please note options for Marker Size, Rotate, Text Block, Text Just. They are important for size and adjustment of text string.

Lab: Symbol (Package Boundary)

The Design Rule Check (DRC) is using package boundary to verify overlapping components and show an error. This also avoids placement of components in restricted areas (Keep Out Areas).

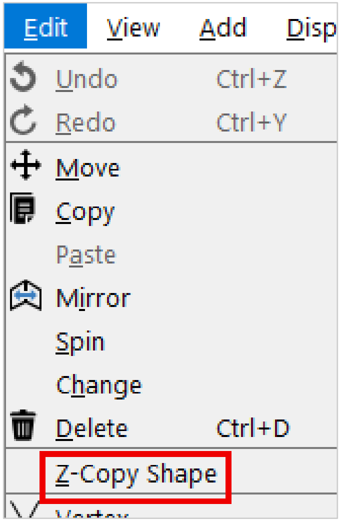
1. **Setup > Areas > Package Boundary** from main menu
2. Package_Geometry und Place_Bound_Top are automatically set.
   Define size based on **worst case** from data sheet.
3. Click **LMB,** to enter polygon for placement boundary.
   To finalize polygon press **RMB > Done.**
   Polygon will be solid displayed.

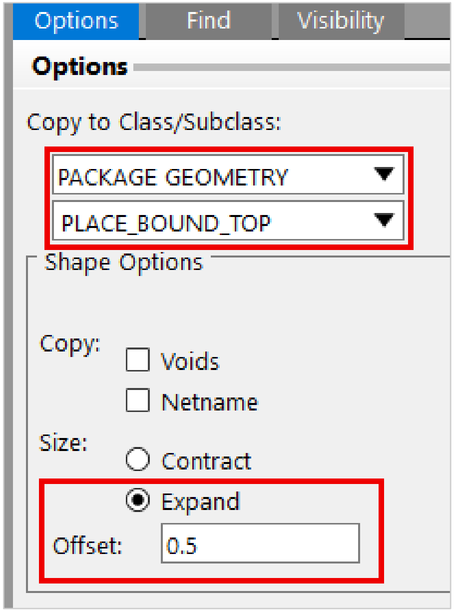


Symbol (Package Boundary)

Some tips about package boundary:

- If you do not generate the package boundary yourself, the system generates it itself when saving. However, this does not necessarily take the real tolerances into account.
- Another way to generate the package boundary is to derive it with **Edit > Z-Copy Shape**.
- You can set the new subclass in the Options and also an expansion under **Expand**.





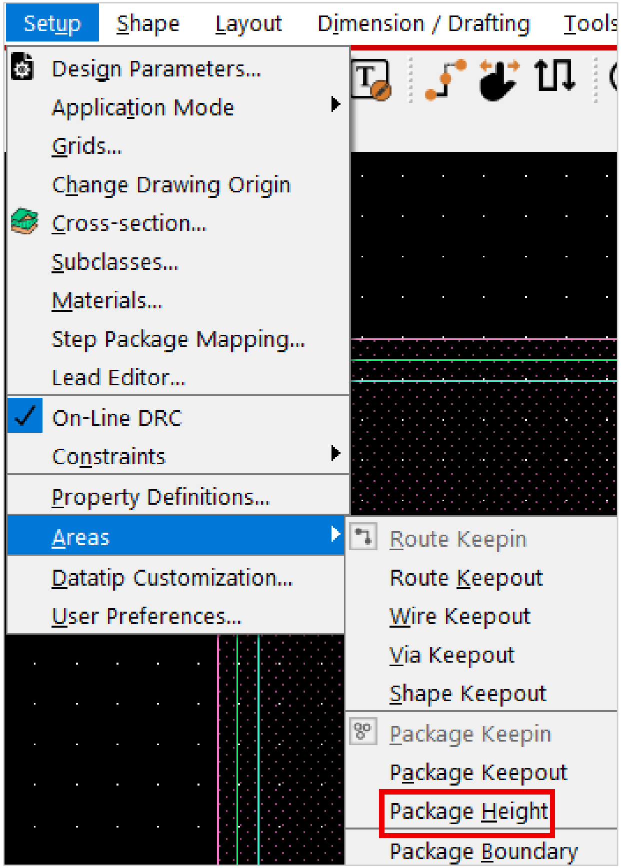
Lab: Symbol (Package Height I)

DRC program is using **Package Height** info to check component placement against predefined height restrictions. The package height is assigned to package boundary as **Max Height** or **Min Height**.

It is **not** mandatory to define a height for every component.

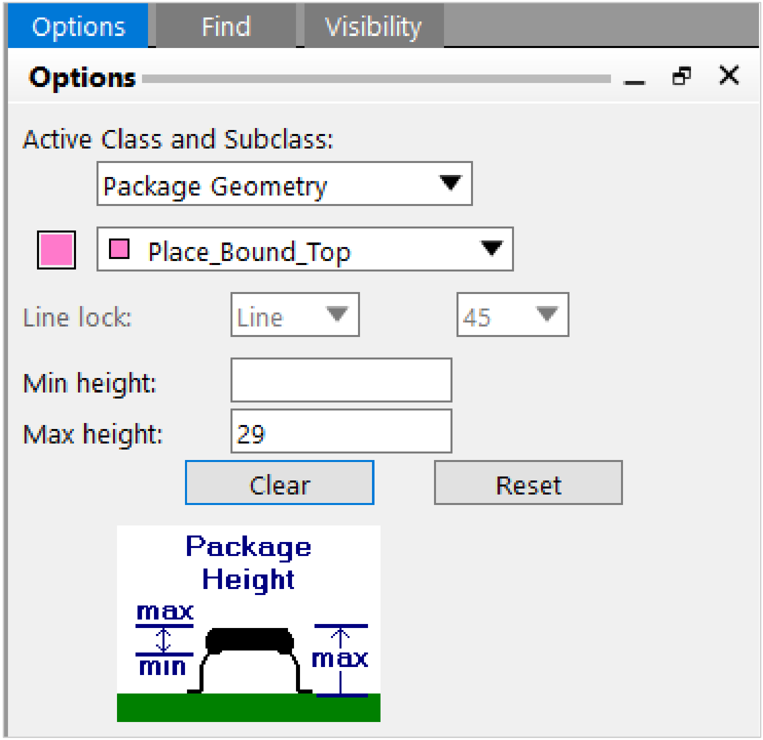
It is possible to define a default height in PCB Editor (**Setup > Design Parameters… > Design > Symbol**).

1. **Setup > Areas > Package Height** from main menu.



Lab: Symbol (Package Height II)

2. Select Package Boundary (filled polygon).
   Enter a height of the transformer of **29** mm in the **Max Height** field.
   Min Height is not relevant here. If a minimum height is also entered, components can be placed on top of each other if their heights allow this.
   RMB > Done to complete the command.
3. Save the part with **File > Save**. The system saves a **.dra** file, and a **.psm** file.
   .psm file is used in the Editor during placement.



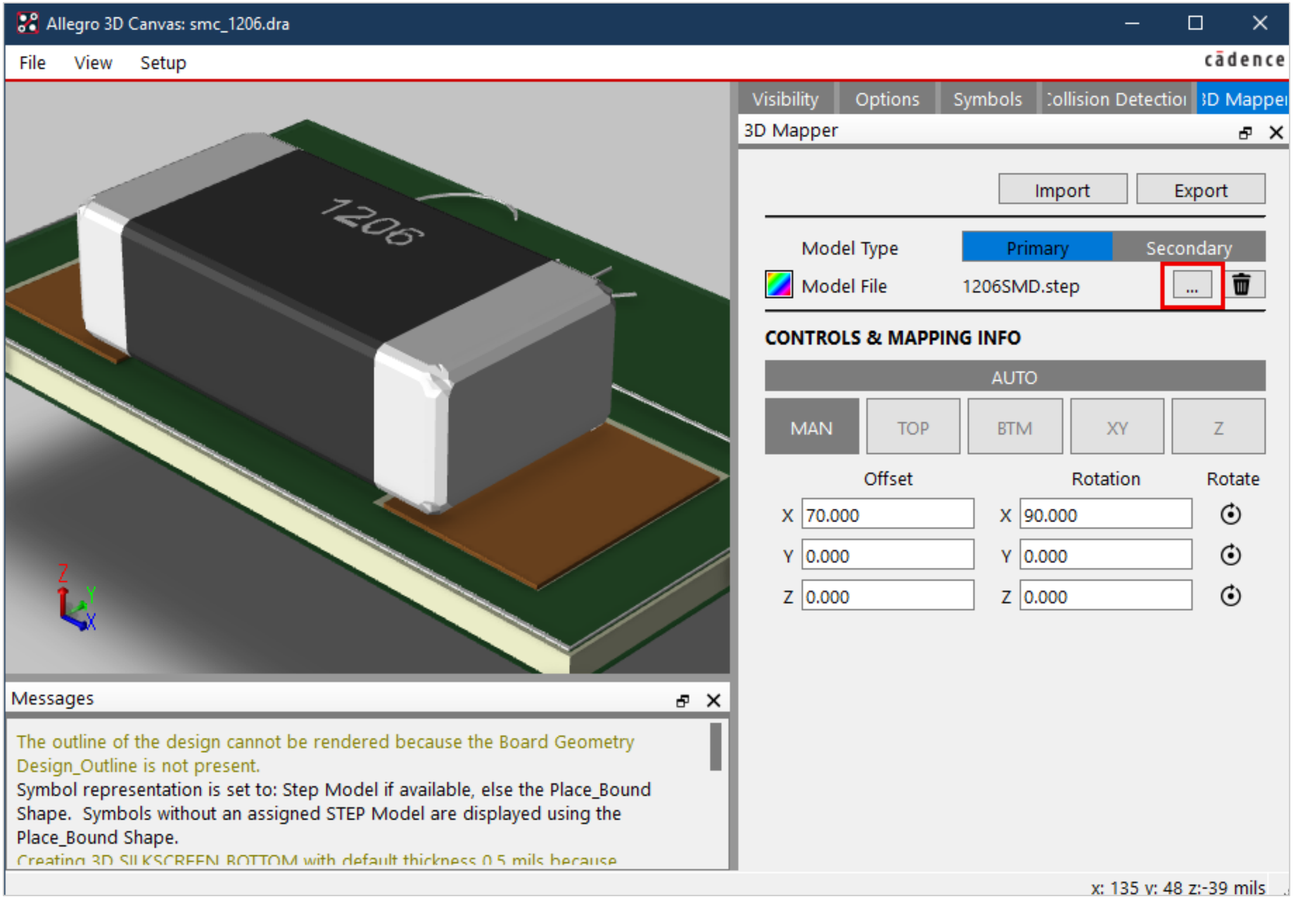
Step Mapping

In addition to the height information that is attached to the place bound, it is possible to map a step model to the part in the 3D canvas.

Selection of the step model is done with the Browse button.

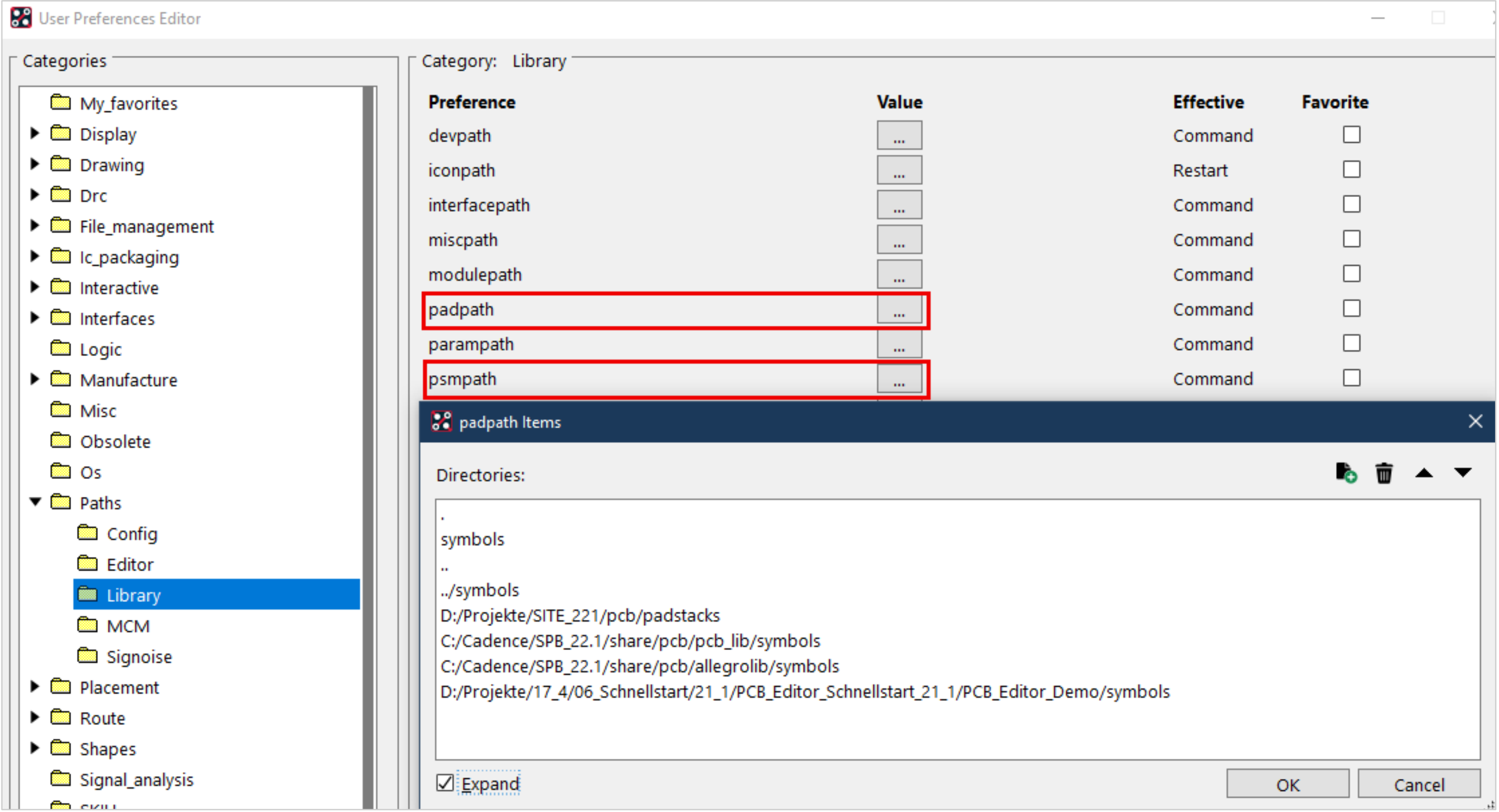
Mapping is done automatically and can be edited manually if necessary.

In the picture the step model of a 1206 capacitor is mapped.



Save Location for Pads and Symbols

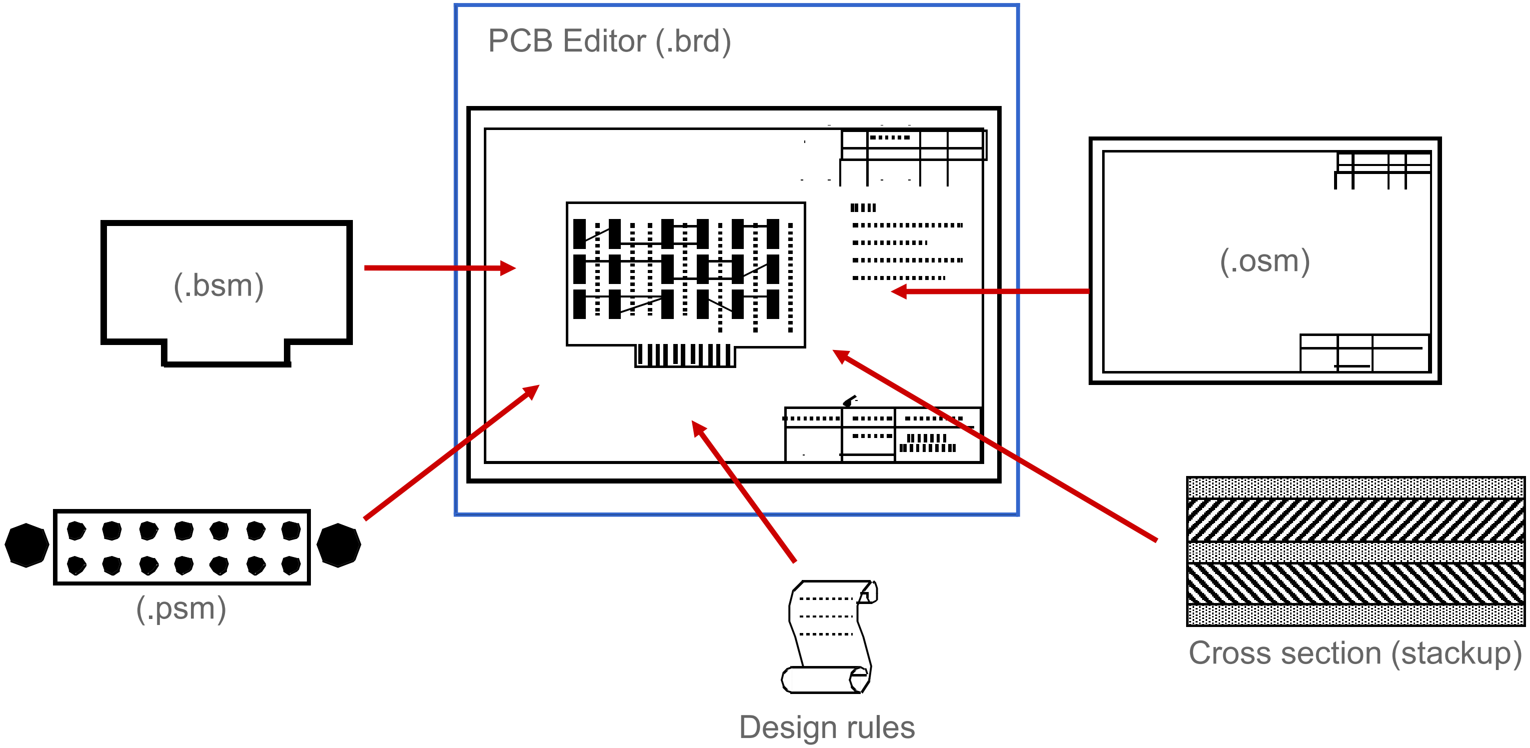
Files generated in Symbol Editor (.dra and .psm) as well as files generated by Padstack Editor (.pad) must be saved in psm and pad path. PCB Editor needs the files to find pads and symbols for placement.



Board Setup

Board Overview

In a board all elements are used which were created by other editors. Image below shows an overview of elements used. How to create board templates will be described in a later capture.

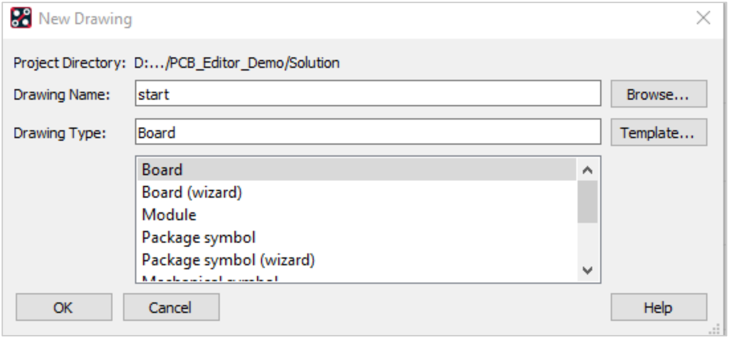


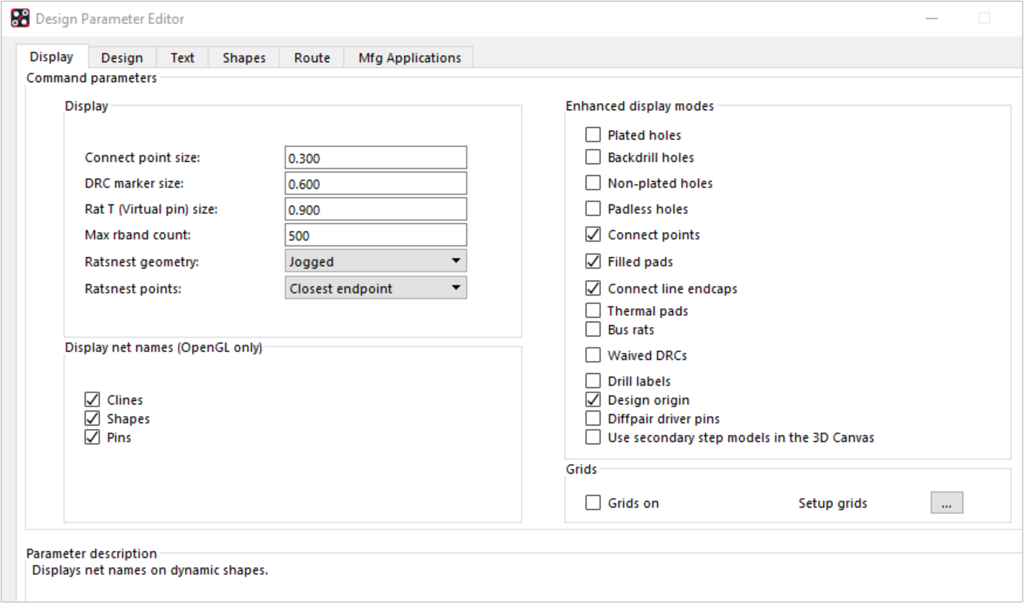
Tip
Different versions of lab boards are available in solution folder.

Lab: Board Setup

Following pages describe the most important steps how to setup a board.

1. **File > New** from main menu
2. Please enter **master** into Drawing Name field.
3. Choose Drawing Type **Board.**
4. **OK**
5. **Setup > Design Parameters… > Design**
6. Please change values as shown in drawing parameter box on the left.
7. **OK**





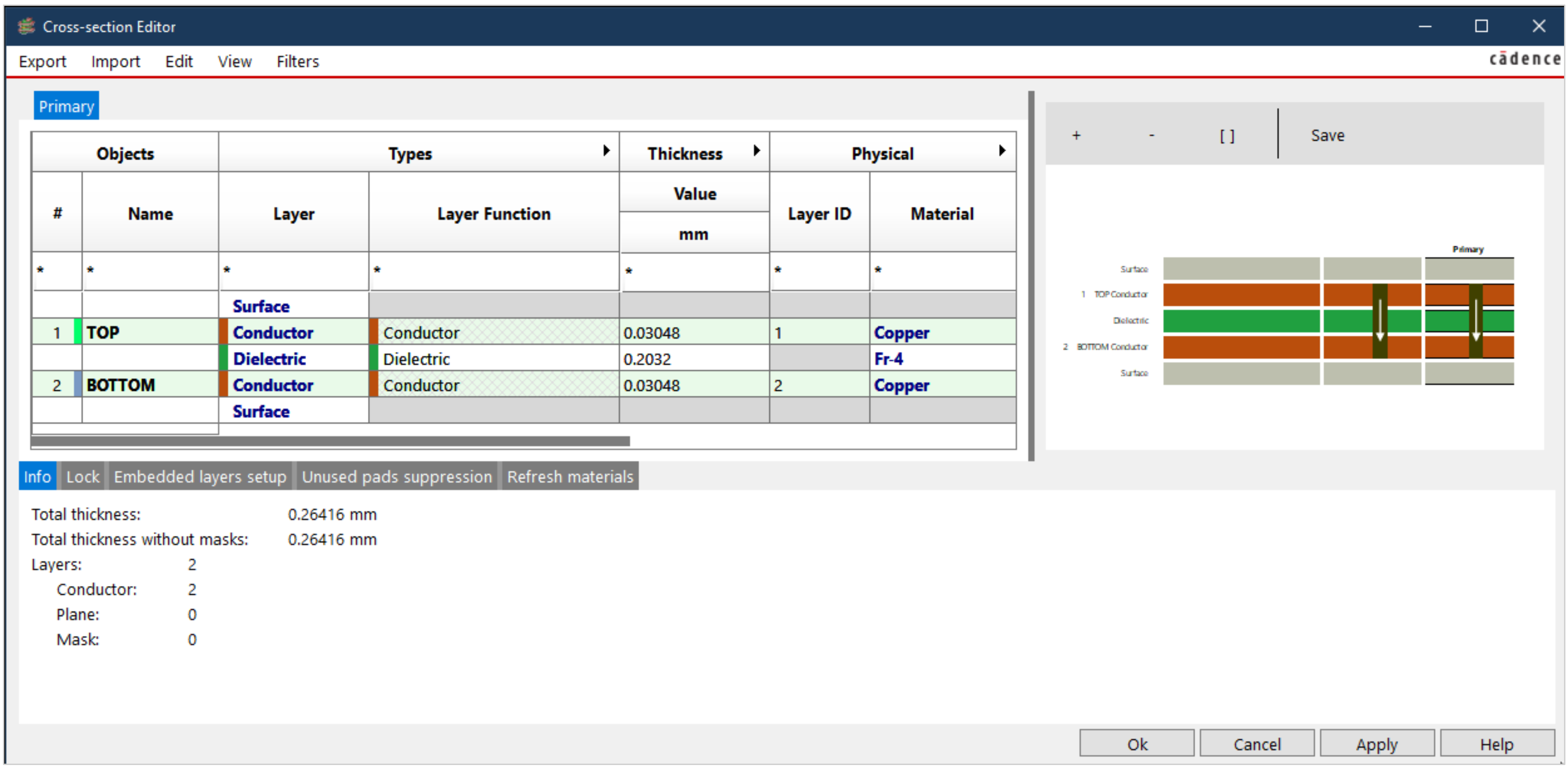
Tip

Drawing Extents should be large enough to include additional elements like drawing frame, title block.

If there is not enough space, you will get an error message.

Lab: Layer Stackup

The layer stackup of the board will be defined with Cross Section Editor. To open, click **Setup > Cross Section** or . Via RMB on an existing layer you can add or remove layers.



Name of layers TOP or BOTTOM cannot be changed. Additional layers can have any name. Chosen names appear also in visibility window.

Lab: Board Outline

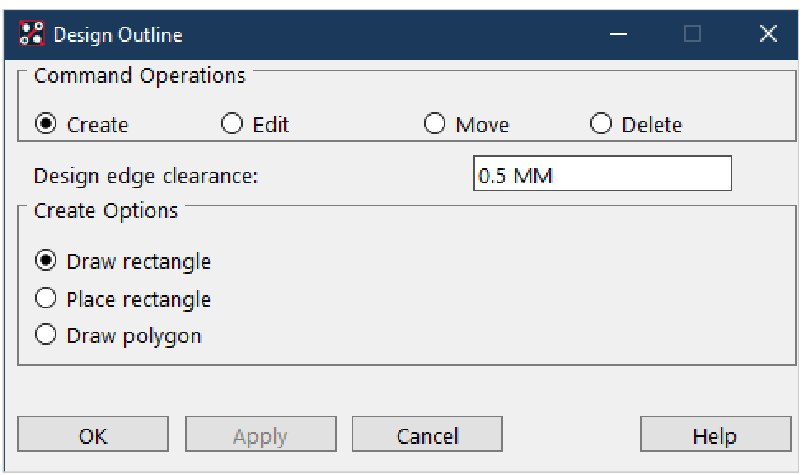
Via **Setup > Outline > Design Outline** the contour of the board can be defined.

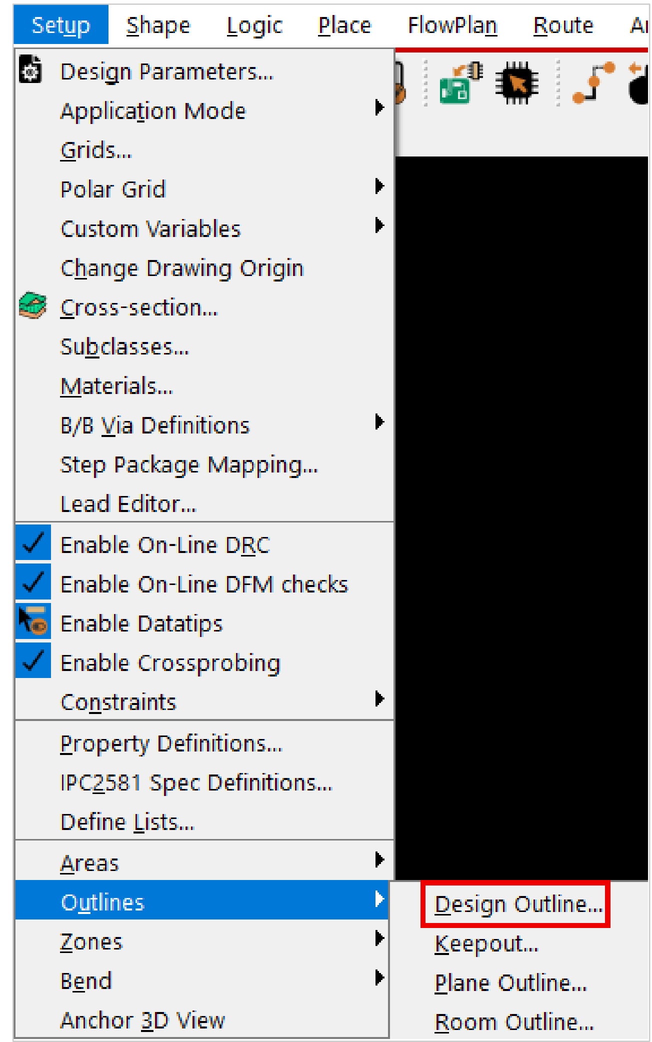
Design edge clearance is the offset (smaller than board contour) for Package Keepin and Routing Keepin.

Keepins can be modified manually later.

On the next pages we use a predefined board template.

If you don't want to create the board outline yourself, you can reuse a predefined one.



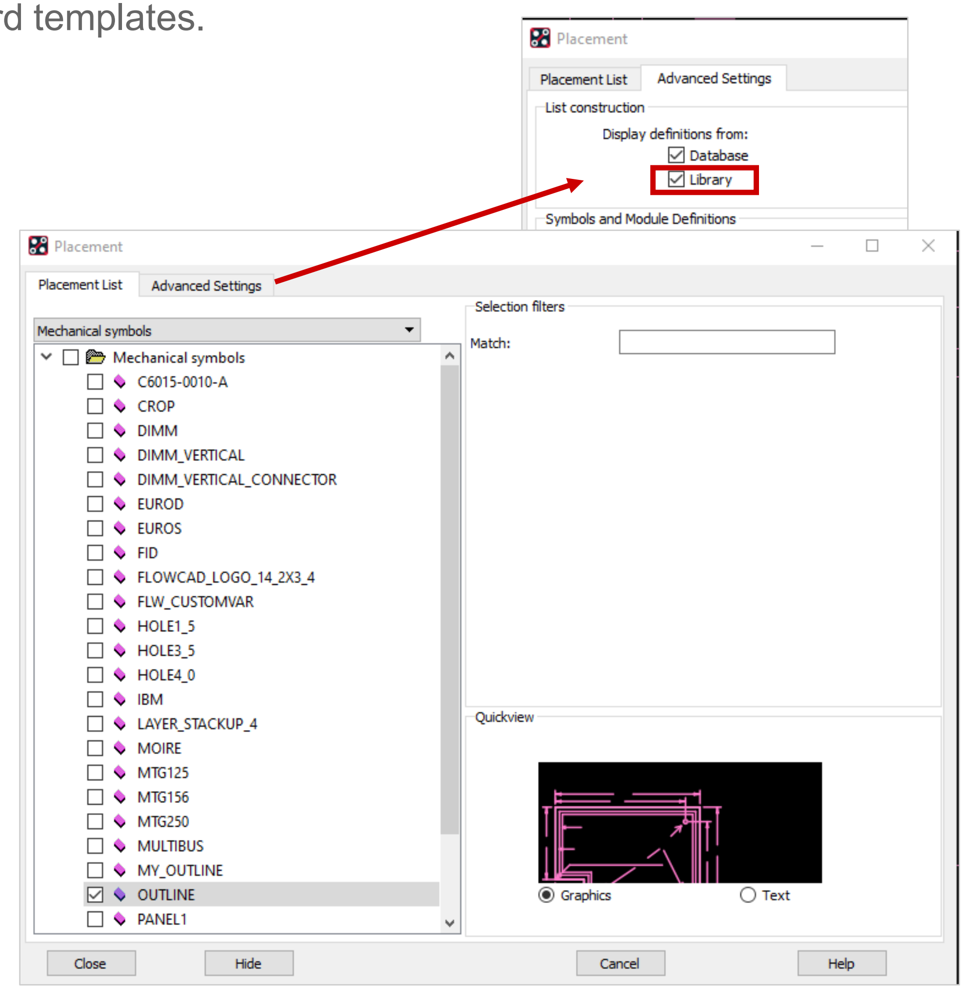


Lab: Board Symbol Placement

In the demo data set a board symbol is available. This board symbol can be used for the next lab. In a later chapter we explain how to create board templates.

Load the board symbol into the still open master board **start.brd** as described below.

1. **Place > Manually** from main menu. Placement Box will appear.
2. In **Advanced Setting** tab select both options, **Database** and **Library.**
3. In the Placement list expand mechanical symbols and select **Outline** (or yourself defined symbol).
4. Type **x 0 0** in the command line and press **Enter**.
5. **RMB > Done**. Mechanical symbol is placed.
6. **File > Save As**. **master.brd** file will be saved.
7. Please **do not** close PCB Editor yet.



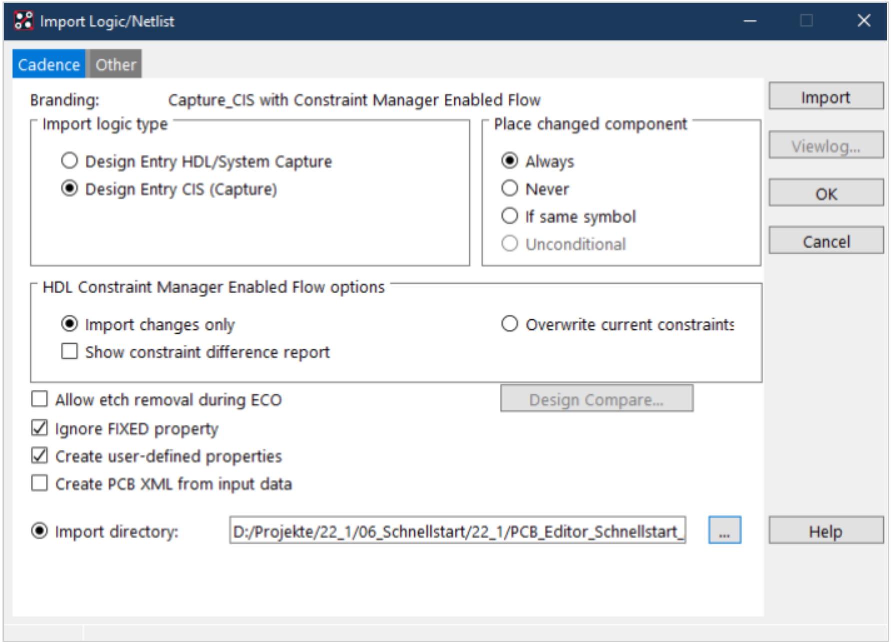
Import of Logic Data

Lab: Import of Logic Data

This chapter explains how to import schematic data into PCB Editor. Some important information regarding the next lab:

- The Schematic is completed.
- The necessary transfer data as well as the schematic are available in folder **Project2.**

1. Load logic data into **start.brd** file via **File > Import > Logic.**
2. Select import logic type **Design Entry CIS**.
3. Configure correct import folder **<Path>\PCB_Editor_Demo\project2.**
4. **Import Cadence** (maybe an incorrect import is reported).
5. **File > Save As… (netlist.brd) Do not close!!**



Design Constraints

Design Rules

Before we start to place components, we should define some basic rules to control placement. In addition we will define some necessary design rules for routing task. Availability of rules and definition options are driven by the used license.

All design rules are managed in Constraint Manager. They are divided in the categories below:

- Electrical Rules: Design rule, to categorize electrical attributes like impedance, topology, …
- Physical Rules: Definition of physical rules like trace width, vias, …
- Spacing Rules: Clearance rules between design objects like traces, pads, vias, copper areas, …
- Same Net Rules: Clearance rules between objects related to same net
- Manufacturing: PCB manufacturing rules like component clearance, mask clearance or minimum copper rings

Rules are separated into two levels:

- Standard Rules: Always available (default) rule set. This rule set is used for majority of nets. Typically for all nets without a specific rule requirement.
- Special Rules: User defined rules sets. These rules are different from standard definition and get assigned only to specific nets, like power or critical signals.

Next to design rules there are assigned properties and DRC violations listed.

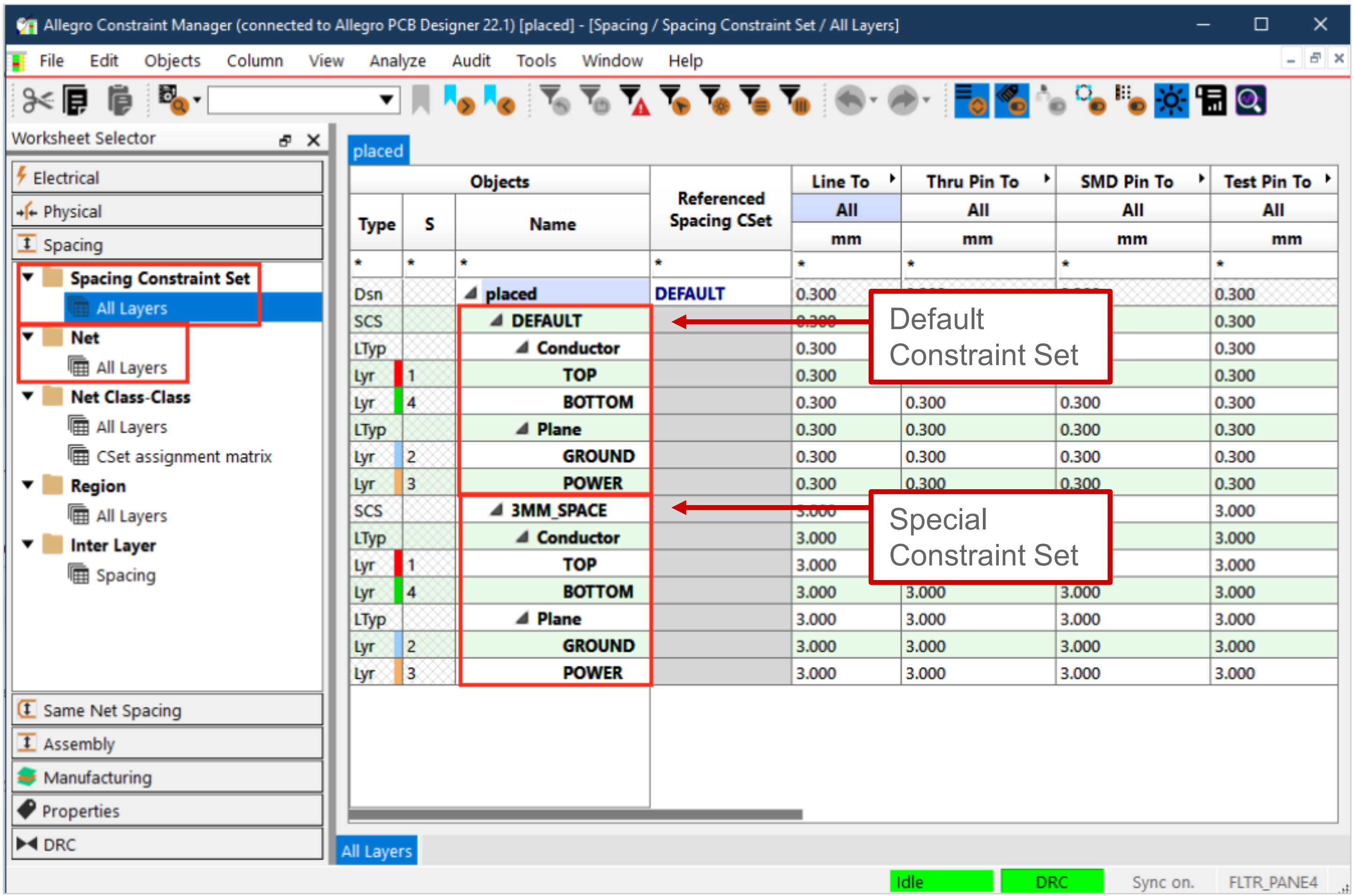
Constraint Manager Overview

Start Constraint Manager via **Setup > Constraints > Constraint Manager…** or

Constraint Domains

Constraint Sets

Constraint Assignment



Standard (Default) Design Rules

Standard rules should be entered in Cset **default**.

In the spacing domain, spacing rules can be assigned for all objects with respect to all other objects. This can also be done on each layer individually.

All nets without a separate assignment from an additional Cset or a direct entry will be checked against the **default** Cset.

power_supply

Objects			Referenced Spacing CSet	Line To										Thru Pin To
Type	S	Name		All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Finger	All
				mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		power_supply	DEFAULT	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
SCS		DEFAULT		0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
LTyp		Conductor		0.300	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	0.300
Lyr	1	TOP		0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Lyr	4	BOTTOM		0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
LTyp		Plane		0.300	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	**0.300**	0.300
Lyr	2	GROUND		0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Lyr	3	POWER		0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
SCS		3MM_SPACE		3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000

Special Design Rules

If you work on a more complex design, you need to assign separate rules to **dedicated nets** which differ from default values. Some nets need modified spacing to each other.

This requires usage of Extended Design Rules. Please note next necessary steps for spacing and physical rules.

- **Step 1:** Creation of a new Constraint Set (CSet)
- **Step 2:** Creation of net classes, where same constraints apply
- **Step 3:** Assignment of Constraint Sets or Net Classes

Lab

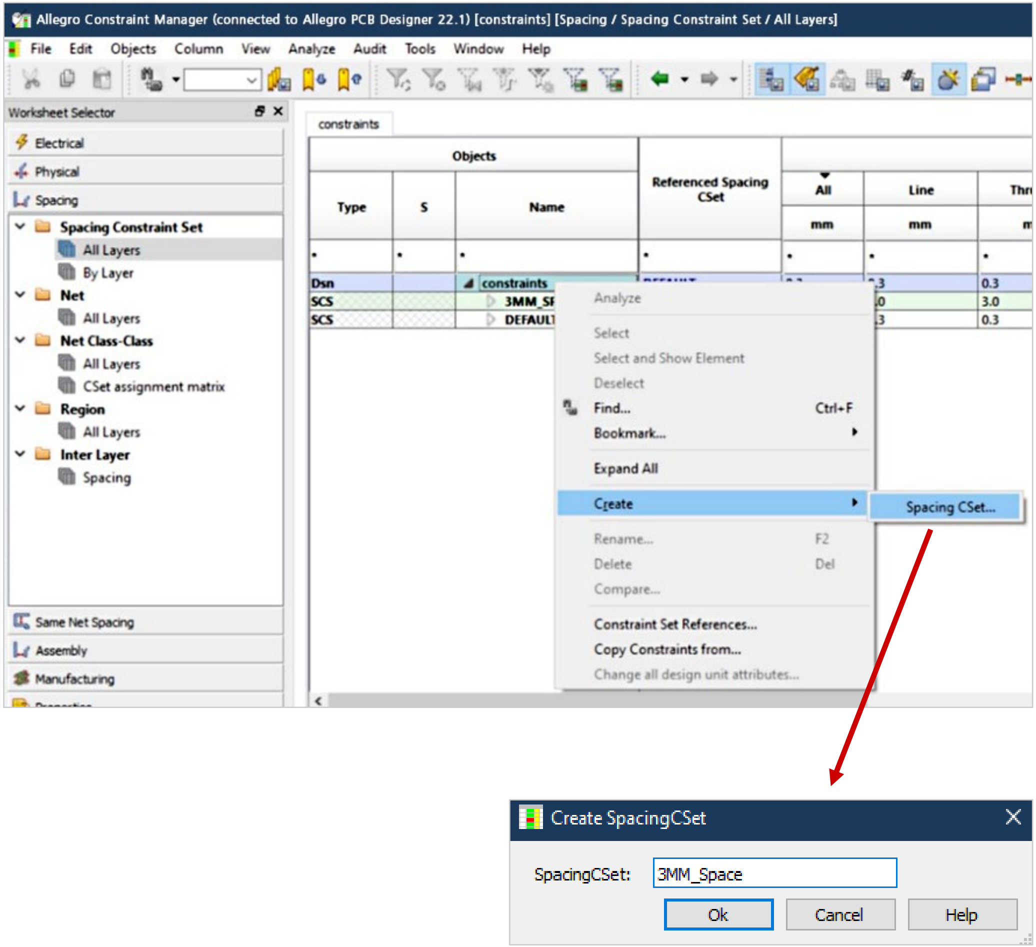
The next pages will guide you through essential steps in the next lab. We will use the **netlist.brd** file.

Lab: Step 1 – New Rule Set (I)

Creation of a new rule set (CSet)

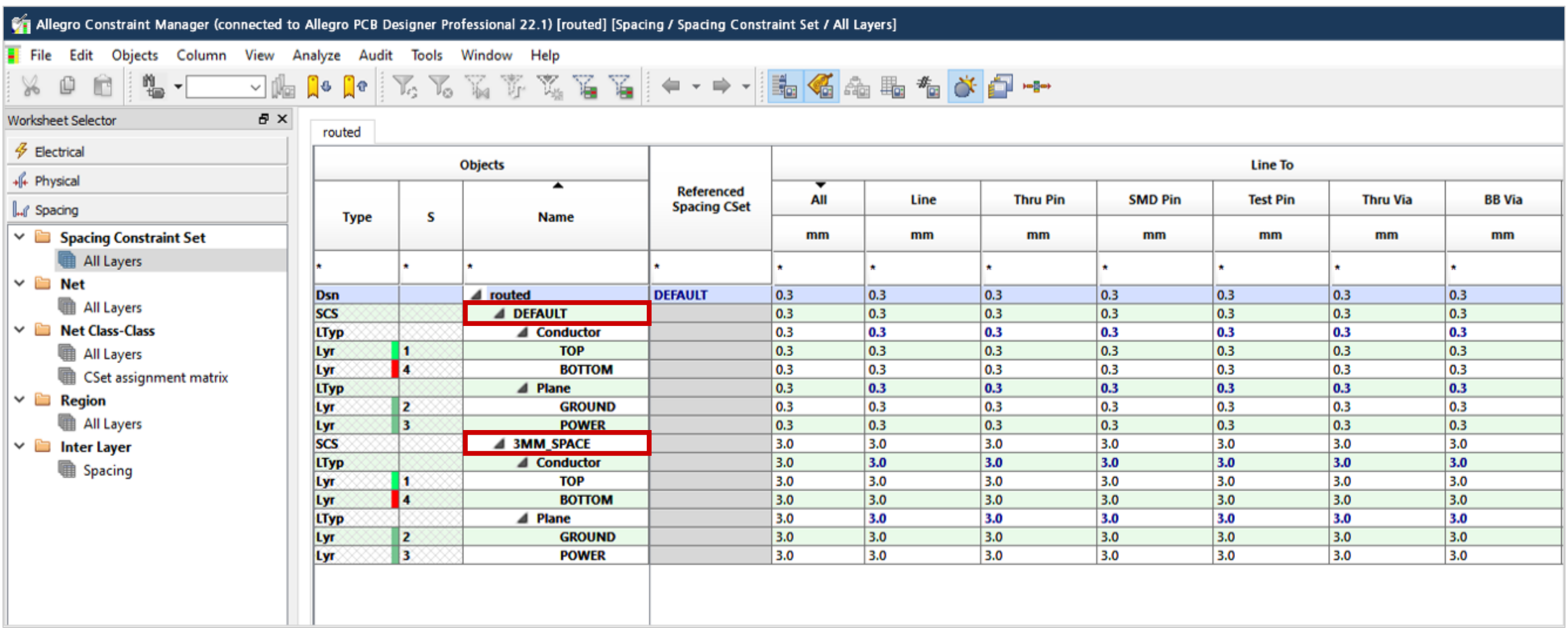
If possible, all rules should be organized in **CSets.** This will simplify the assignment to multiple nets. Each rule can be assigned individually too.

1. Creation of a new **Spacing CSet:** Select section **Spacing > RMB** on **Design Name** click **> Create > Spacing CSet…**
2. Enter name **3mm_Space** and click **> OK.**



Lab: Step 1 – New Rule Set (II)

3. Please choose **Spacing Constraint Set > All Layers > All.**
4. Change all values of **DEFAULT** rule to **0.3 mm.**
5. Change all values of **3MM_SPACE** rule to **3 mm.**

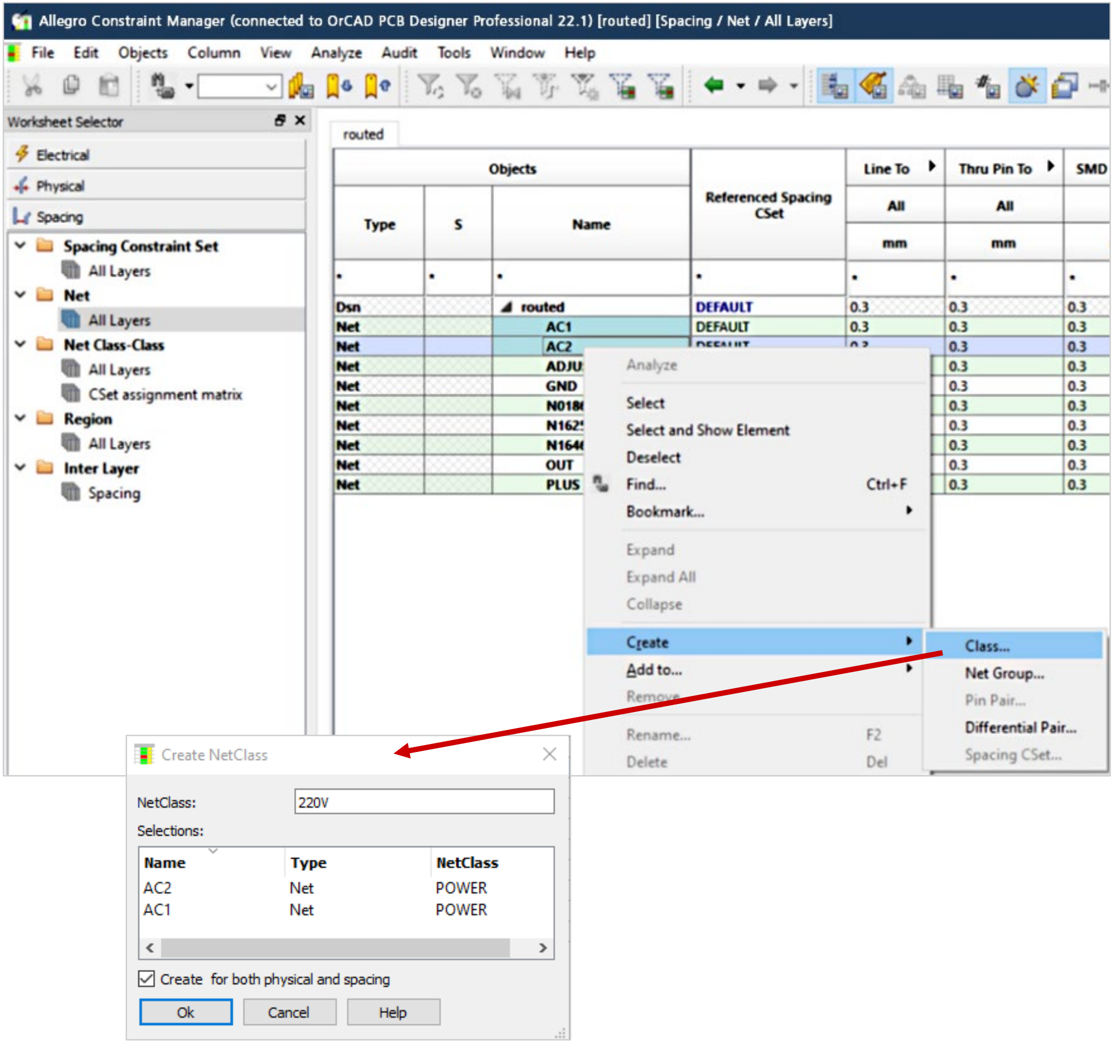


Objects			Referenced Spacing CSet	Line To						
Type	S	Name		All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via
				mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*
Dsn		routed	DEFAULT	0.3	0.3	0.3	0.3	0.3	0.3	0.3
SCS		DEFAULT		0.3	0.3	0.3	0.3	0.3	0.3	0.3
LTyp		Conductor		0.3	0.3	0.3	0.3	0.3	0.3	0.3
Lyr	1	TOP		0.3	0.3	0.3	0.3	0.3	0.3	0.3
Lyr	4	BOTTOM		0.3	0.3	0.3	0.3	0.3	0.3	0.3
LTyp		Plane		0.3	0.3	0.3	0.3	0.3	0.3	0.3
Lyr	2	GROUND		0.3	0.3	0.3	0.3	0.3	0.3	0.3
Lyr	3	POWER		0.3	0.3	0.3	0.3	0.3	0.3	0.3
SCS		3MM_SPACE		3.0	3.0	3.0	3.0	3.0	3.0	3.0
LTyp		Conductor		3.0	3.0	3.0	3.0	3.0	3.0	3.0
Lyr	1	TOP		3.0	3.0	3.0	3.0	3.0	3.0	3.0
Lyr	4	BOTTOM		3.0	3.0	3.0	3.0	3.0	3.0	3.0
LTyp		Plane		3.0	3.0	3.0	3.0	3.0	3.0	3.0
Lyr	2	GROUND		3.0	3.0	3.0	3.0	3.0	3.0	3.0
Lyr	3	POWER		3.0	3.0	3.0	3.0	3.0	3.0	3.0

Lab: Step 2 – Net Class (I)

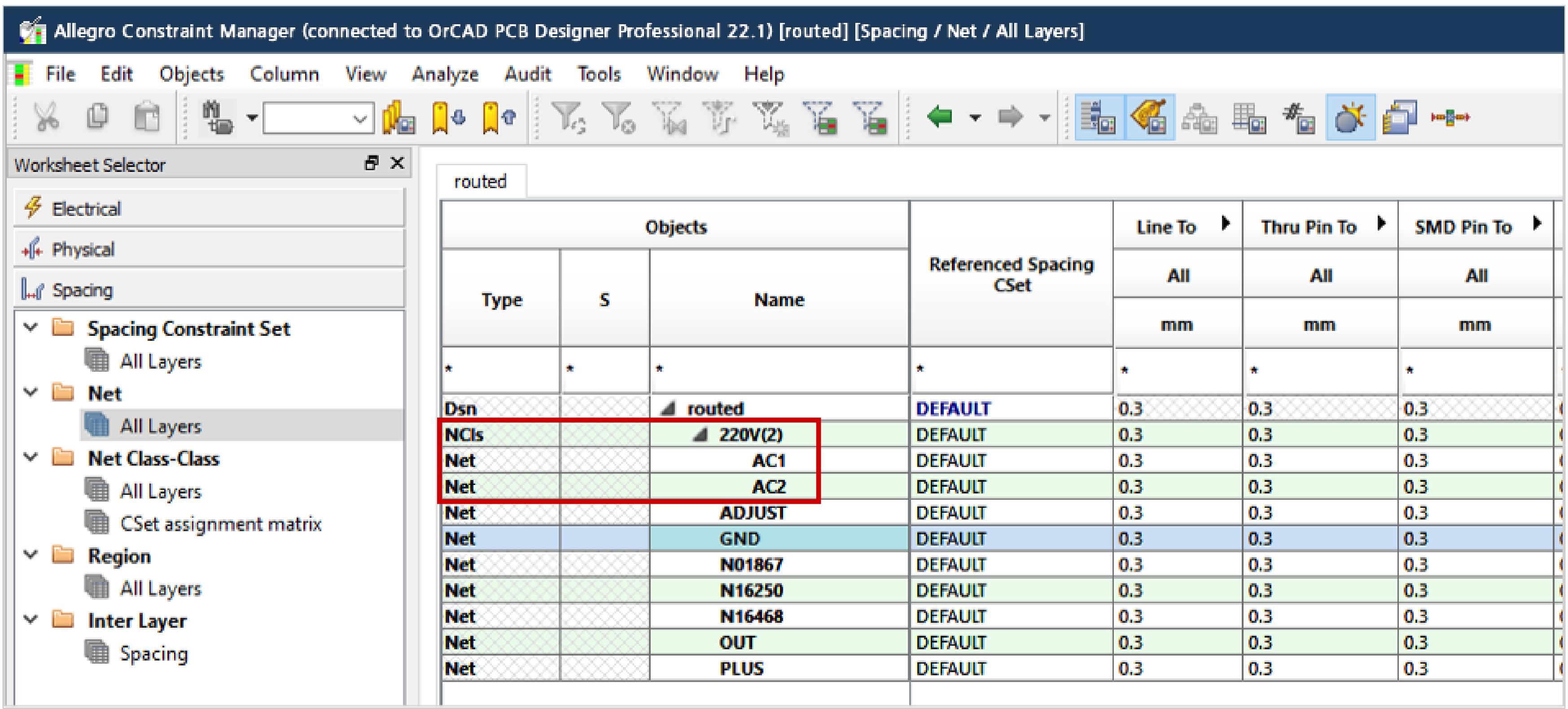
Creation of a net class

1. Select nets AC1 and AC2 and click **RMB > Create > Net Class… >**
2. Enter name **220V** and click **OK.**



Lab: Step 2 – Net Class (II)

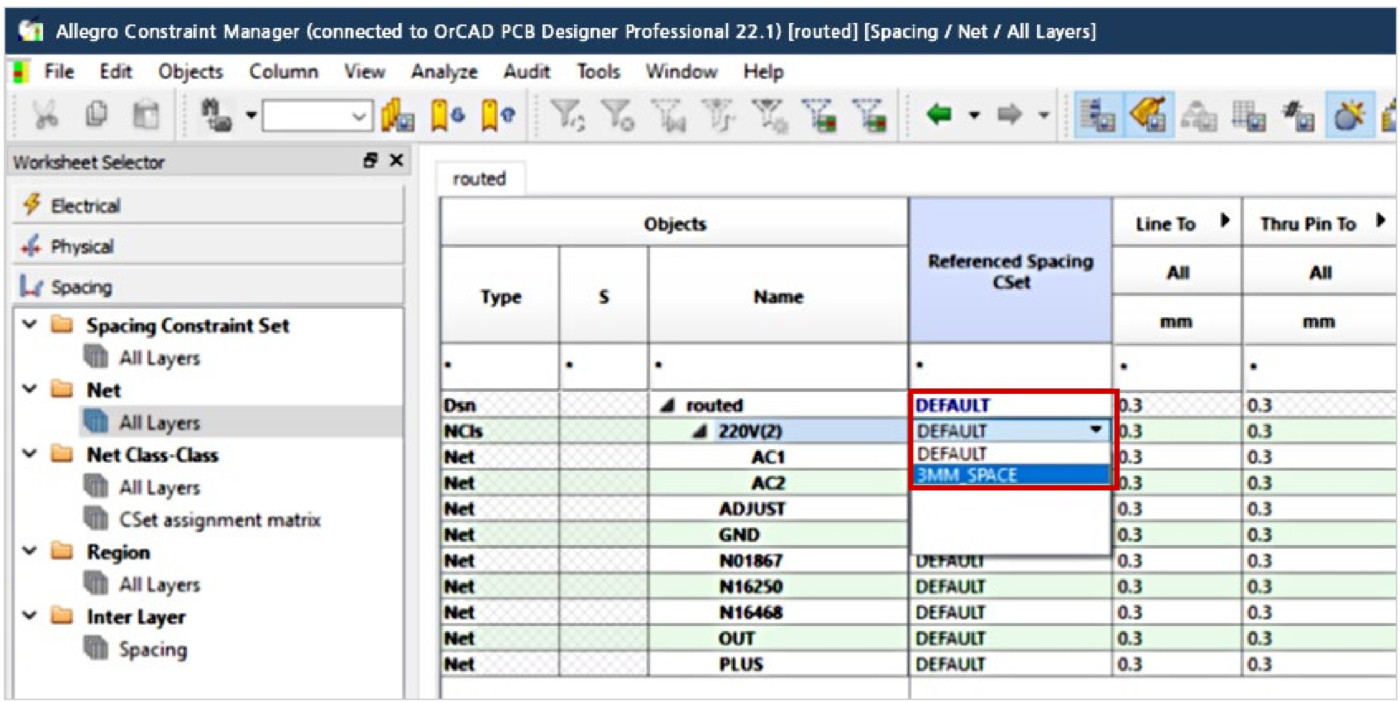
3. Now nets **AC1** and **AC2** are members of **Net Class 220V.**



Lab: Step 3 – Assignment

Assignment of rule sets to net classes

1. Chose **Spacing > Net All Layers > Line**.
2. Select the field on the right next to net class name **220V.** A selection window will open.
3. Select **3MM_SPACE.**
4. Now the 3MM_SPACE rule set is assigned to net class 220V.



Physical and Same Net Rule Sets

Handling of rule sets in **Physical Worksheet** and in **Same Net Spacing Worksheet** are identical to steps 1 to 3 of **Spacing Worksheet** in previous lab.

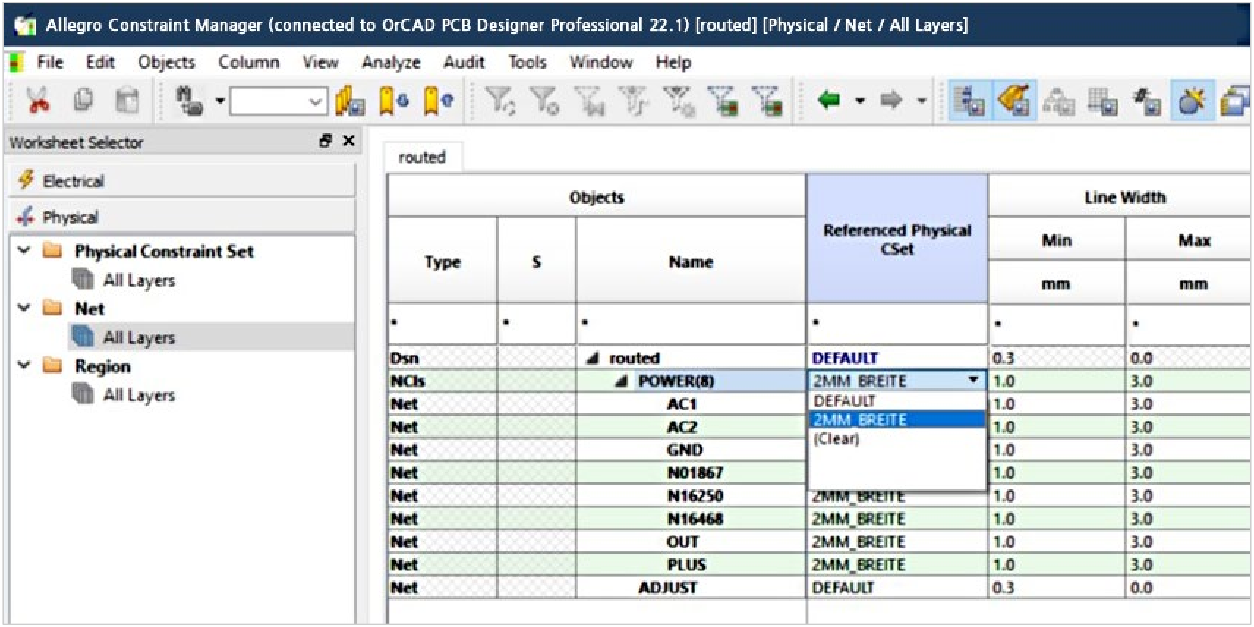
You just need to select desired category in the **Worksheet Selector** of the CM on the left side.

Tip

Rule sets of worksheets

- **Physical**
- **Spacing**
- **Same Net Spacing**

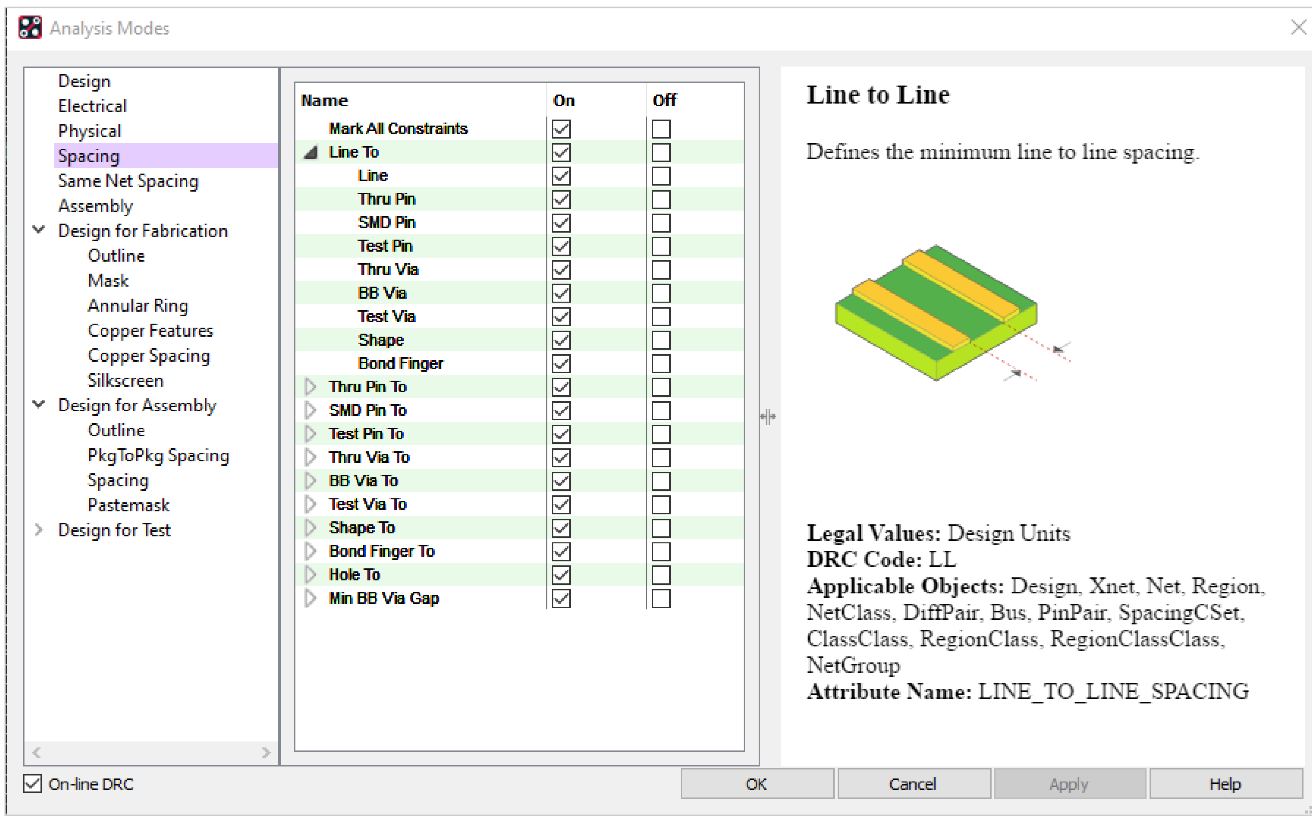
are completely independent and must be created separately and assigned separately.



Constraint Modes (I)

Defined and assigned rules in Constraint Manager must be activated.

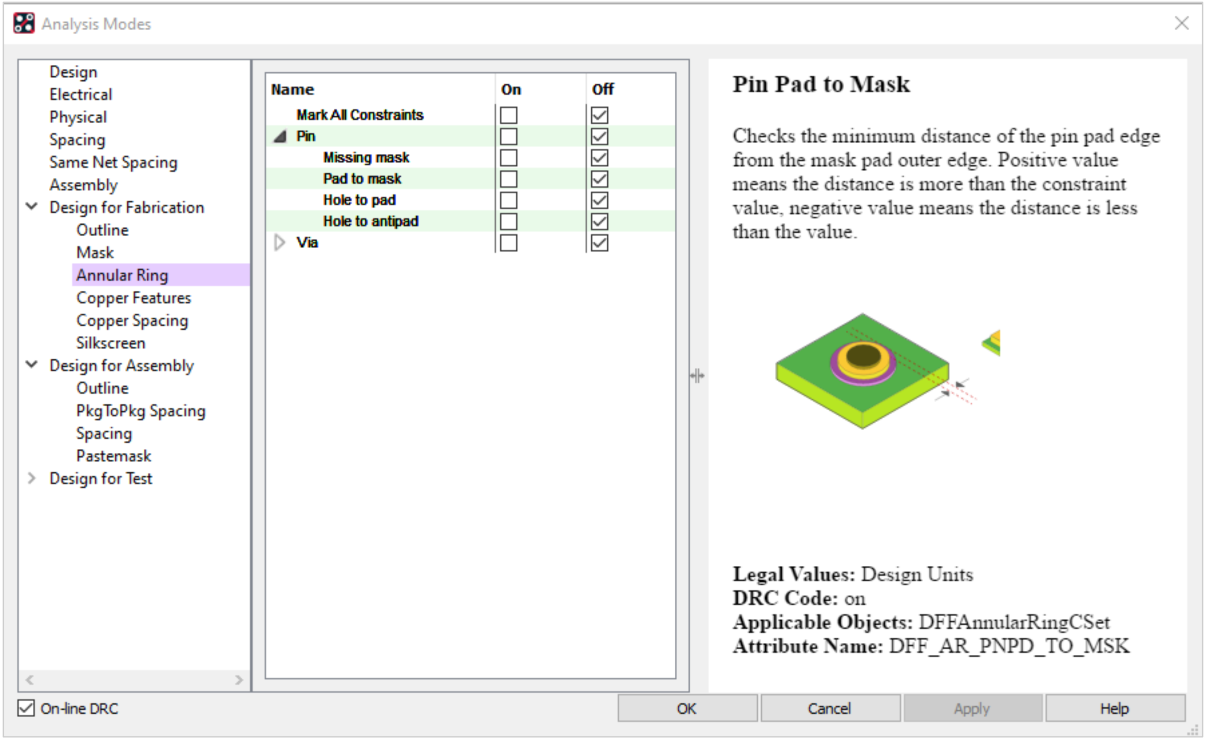
This can be done in Constraint Manager under **Analyze > Analysis Modes** or in PCB Editor under **Setup > Constraint > Modes**



Constraint Modes (II)

Constraint Manager allows to configure many additional checks. In this quick start document we don't take this into consideration.

In **Analysis Mode** you can find many notes to different checks.



Constraint Manager Webinar Series

The FlowCAD Webinar Series provides further information on the various topics related to the Constraint Manager:

- Optimized Usage of Constraint Manager (EN)
- High Speed Constraints (EN)
- Physical / Spacing Constraints (EN)
- Manufacturing Rules (EN)

Part Placement

Part Placement (In General)

After setup of Design Constraints we focus on multiple options for part placement in this chapter. The lab is based on our known example.

The PCB Editor needs the data below for part placement:

- Netlist
- Package Symbol (footprint)
- Padstack
- Shape definitions (for specific pad geometries)

Footprints and padstacks (including shapes) must be available for placement in libraries.

The paths to the libraries are defined via **PSMPATH** and **PADPATH** and stored in **env** file.

Complementary elements for placement are:

- Floor planning (can be pre-defined in schematic using ROOM property).
- Package keepouts (prevents to place components in restricted areas).
  Can be defined in **Setup > Areas > Package Keep out.**

Part Placement (Type)

We differentiate three types of placement:

1. Manuel placement (**Place > Manually**): From the list of unplaced components, components get selected and manually placed.
2. Quickplace (**Place > Quickplace**): Semi-automatic placement of component groups based on selected criteria.
3. Auto placement (**Place > Autoplace**): Automated placement of components. There are additional definitions required, like an additional placement grid.

We will focus on manual placement and quickplace only.

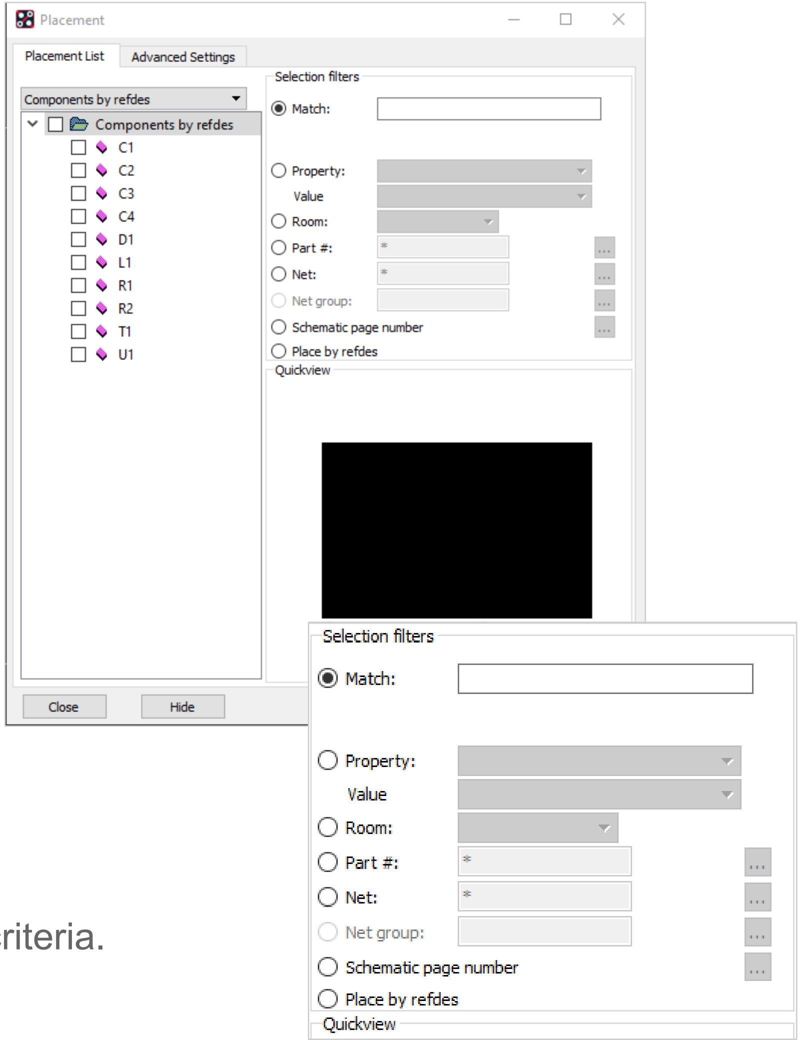
Especially for manual placement, placement grid (**Setup > Grids**) has to be set appropriately.

Place Manually…

Start manual placement with **Place > Manually** or

There are **five** options available:

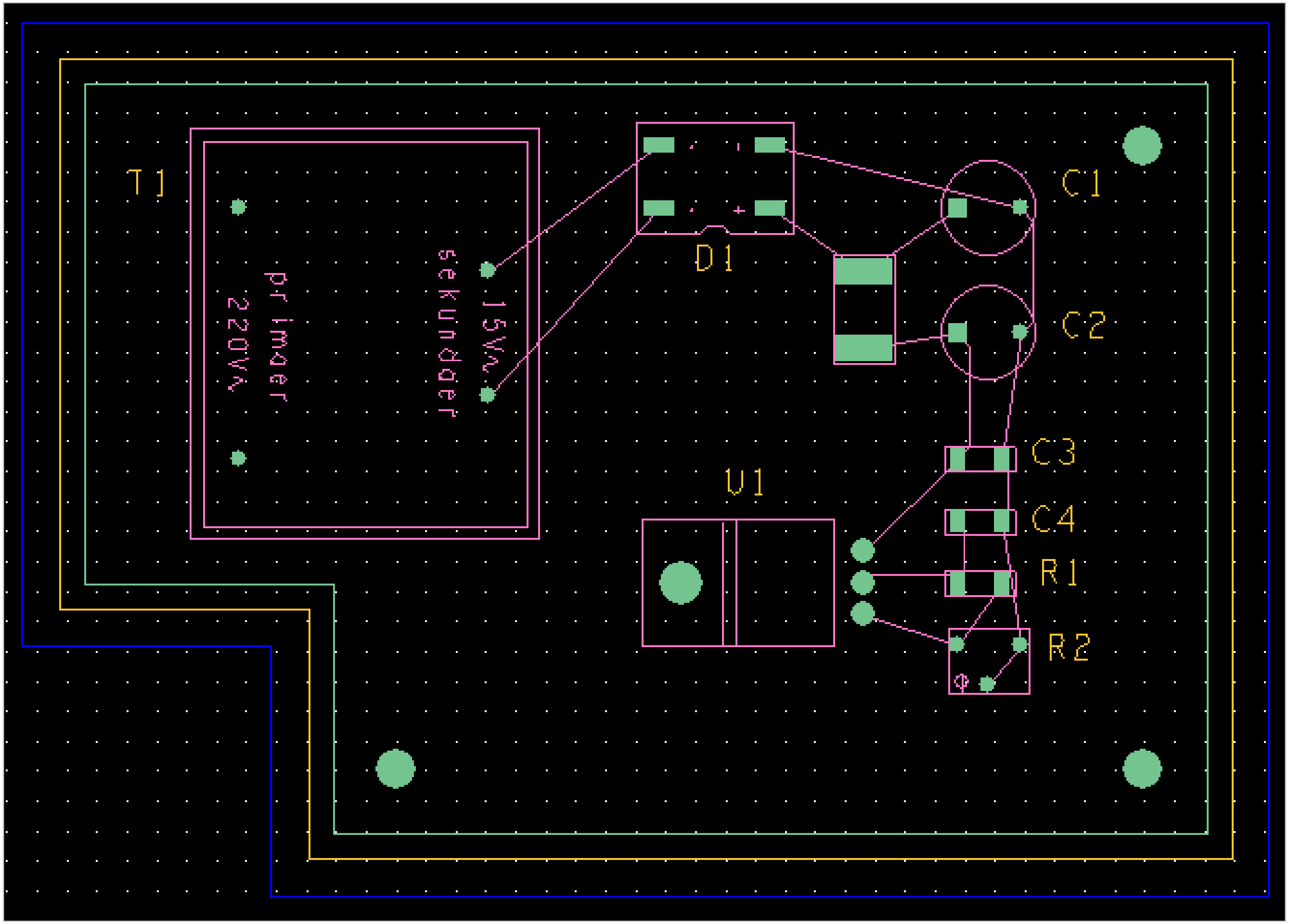
- **Components by refdes**
  Select components by REFDES, based on loaded netlist
- **Components by net group**
  Based on net group definition in Constraint Manager
- **Package Symbols**
  Placement of packages (footprints) without considering electrical information or netlist
- **Mechanical Symbols**
  Placement of mechanical elements like mounting holes or additional outline data
- **Format Symbols**
  E. g. drawing frame for documentation



Selections Filter provides a variety of practical selection criteria.

FlowCAD

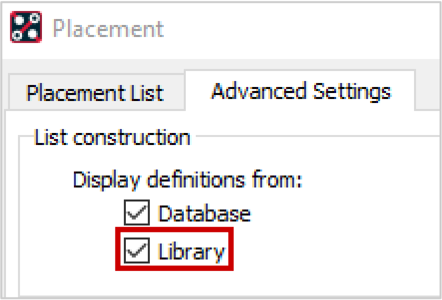
Placement Template

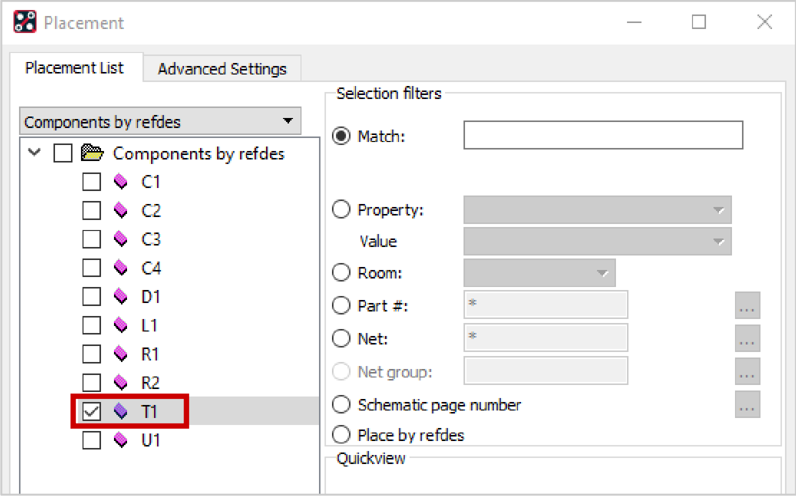


Lab: Place Manually (I)

In this chapter we will have a look at the flow and options for component placement. We will use the **constraints.brd** generated in the previous chapter**.** We will place the components according to the picture on the previous page. After loading the netlist (Import > Logic) information into the design. With the placement the footprint will also be loaded into the board file.

1. Please open **constraints.brd**
2. **Place > Manually…**
3. Select library under **Advanced Settings**
4. Chose transformer **T1.**
5. **RMB > Rotate** (Pin 1 and 5 to the left)
   Alternative **Short Key R** as defined in Chapter 2.
6. **LMB** to position T1.
   Please place transformer in top left corner of the board. Please note the **P** in updated placement list right after placement.
7. Close the placement window with **OK.**
8. Don't place any further components yet.





Filter Parameters

Before we complete placement, we would like to focus on different options of the selection filter. Especially for larger boards multiple filter criteria are very useful during manual placement.

The selection filter limits the number of components which are available for placement.

Please test above mentioned options with our test example **before** you have completed placement. Some options will not be available after a placement is completed.

Choose the option which fits best to your needs.

Match	Via REFDES and wildcard “*” followed by TAB key you can select for example capacitors only
Property	Defined properties and values including user properties
Room	Placement by room property for floor planning
Part #	Placement by part number
Net	Placement of parts which are connected to a specific net.
Schematic page number	Only available for Design Entry HDL
Place by refdes	Additional selection criteria like class property or pin count

Additional Commands (I)

During or after placement there are additional functions required to realize or modify a PCB design.

Below you can find the most important functions accessible via **Edit > …** or by illustrated icons.

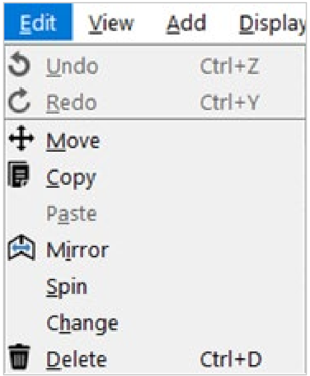
Move → Move of components

Copy → Copy of elements

Mirror Move parts from top layer to bottom layer

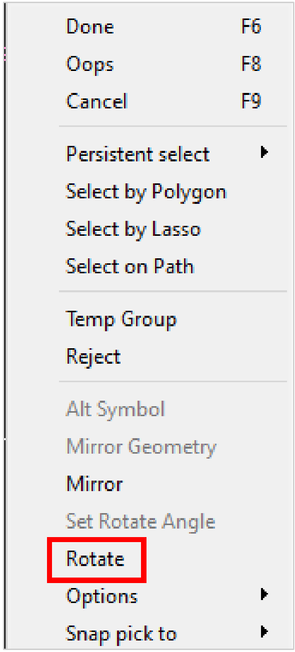
Spin Rotate elements

Delete → Delete elements



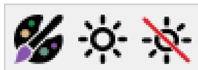
Tip
Please pay attention to **Find Filter** and extensive options in **Option Control Panel** for all functions.

Many functions are accessible by right mouse button.
E. g. **Rotate** is a sub function of **Move** or **Place**.



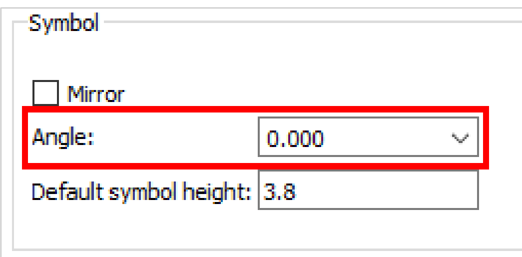
Additional Commands (II)

Ratsnet OFF / ON  Guidelines on / off (**Display > Show / Blank Rats >…)**

Assign Color  Permanent color assignment of any elements

Highlight / Dehighlight Usage of Find Filter and Option Panel
Also via **Display > Assign Color / Highlight / Dehighlight**

Setup > Design Parameters…



Mirror and **Angle** allow a presetting under
Place > Manually > Design related to placement
TOP / BOTTOM and rotation.

Complementary elements for placement:

- By using room property a floorplanning could already be prepared in schematic
  ➔ **Setup > Outlines > Room Outline…**
- Package Keepout / Keepin / Height are restrictions for components
  ➔ **Setup > Areas > Package Keepout / Package Keepin / Height**

Quickplace

Start Quickplace via **Place > Quickplace…**

Quickplace is a very flexible and universal tool to make component placement more efficient.

With one click you can verify if all library elements for parts in the netlist are available. To do so, use the commands below:

- Placement Filter set to **Place all components**
- Placement position to **Around package keepin**

and then: **Place**

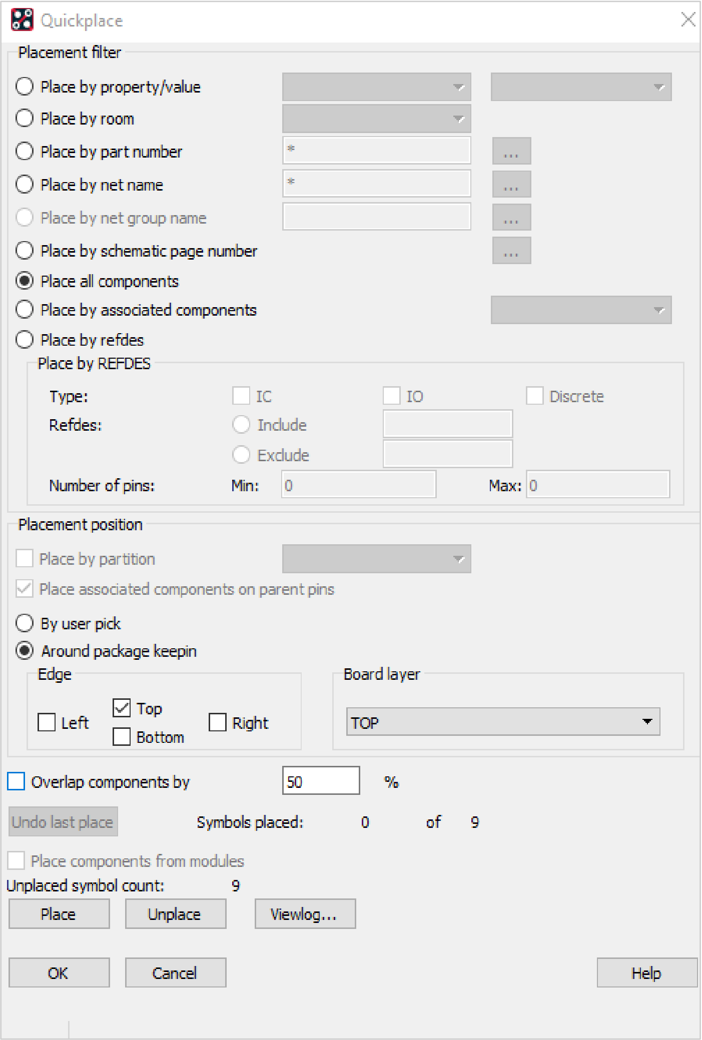
Unplaced Symbol count gives a message if components could not be placed because of missing library elements or an incomplete library path.

Place Manually function is used to check which parts these are.

All other options are self-explanatory, although some of them require definition of corresponding properties in schematic.

Tip

Unplace is only possible as long **Quickplace** has not been confirmed via OK.



Lab: Place Manually (II)

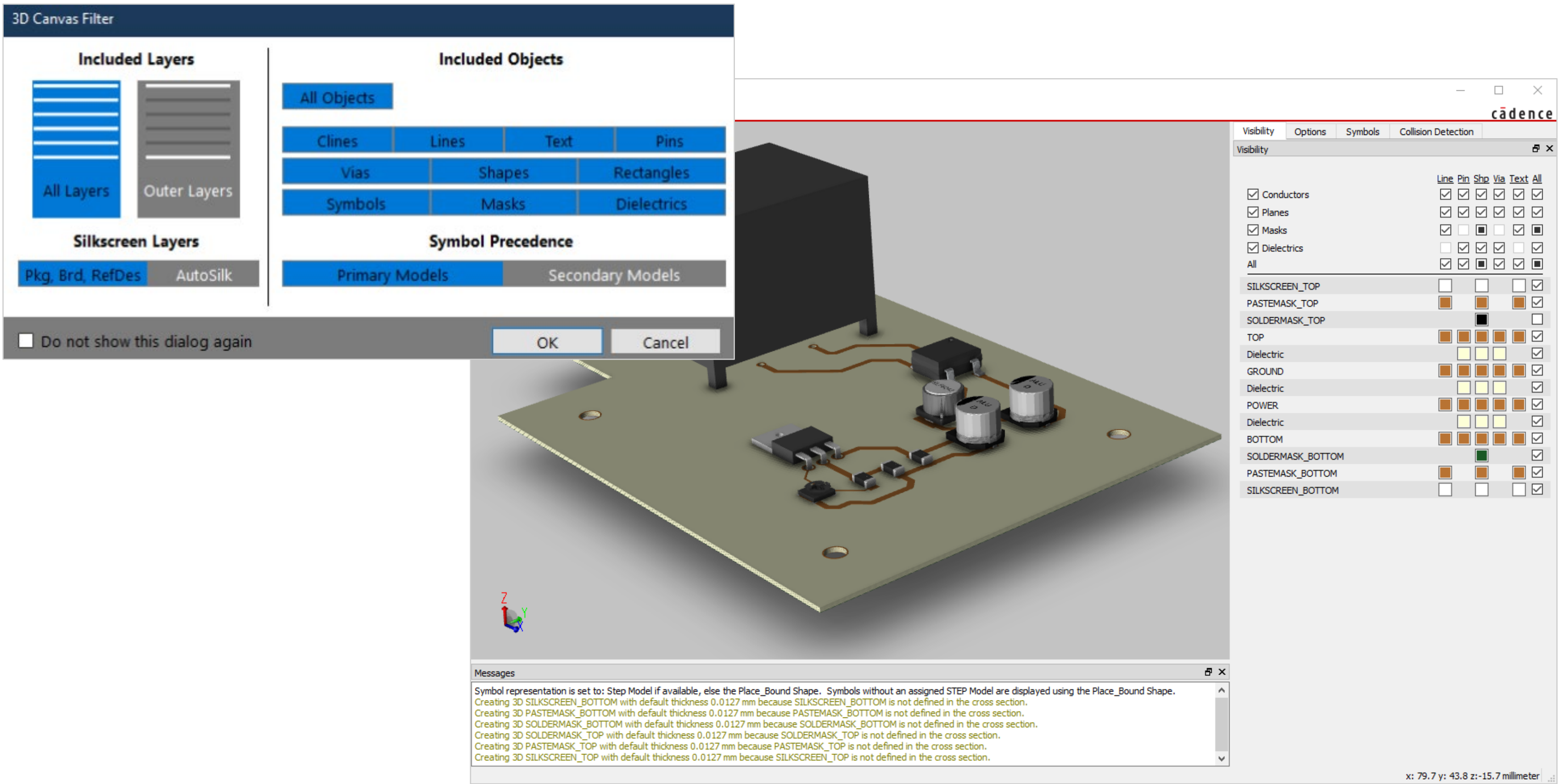
1. Choose **Place > Manually…**
2. Please note that T1 is not listed anymore.
3. In selection filter please select ROOM and chose Room Gleichrichter.
4. Parts C1, C2, D1 and L1 are listed in selection window.
5. Select **D1** and rotate by 180 degree.
6. Place via command line. Enter: **x 30 45** and **Enter.**
7. Select capacitors and place them with pin 1 to the left (270 degree) to position: 45 45 and 45 35.
8. Select L1 and place coil with pin 1 to the top (270 degree) to position: 37.5 40.
9. Now select **ROOM** in selection filter and chose **U-Regler** as room.
10. All remaining components are listed. Please select all.
11. Place one after another at: 45 25; 45 20; 45 15; 45 10 (90 degree); 37.5 12.5 (90 degree), **RMB > Done.**
12. Once again **Place > Manually.** List for **Comp by Refdes** is empty. All components are placed now.
13. Close placement window with **OK.**
14. **Edit > Change** and select in Option Panel **Text Block + 6**, set Find Filter to **Text only**.
15. Click on each REFDES or drag a rectangle over a group. All REFDES have now **same** size.
16. **Edit > Move** and set Find Filter to **Text only.**
17. Move all REFDES as illustrated and use rotate command (e. g. RMB).
18. Save result as **placed.brd**.

3D Canvas

3D Canvas I

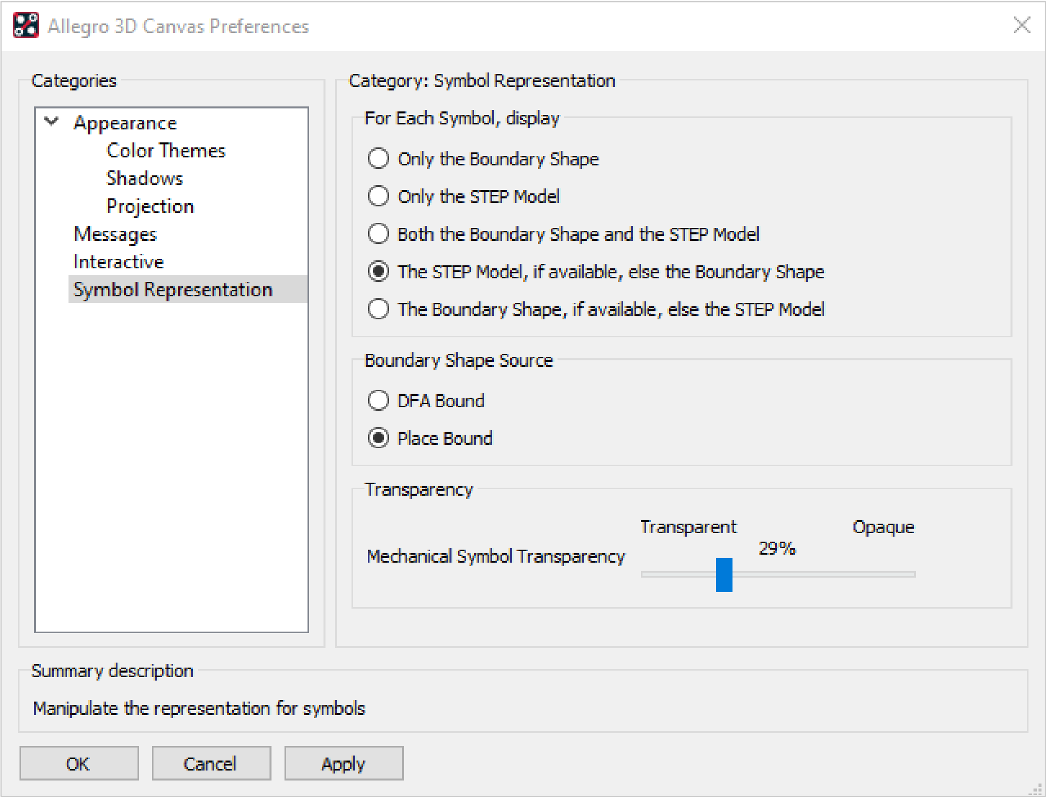
By **View > 3D** or  you get access to 3D Canvas.

With the 3D Canvas Filter, it is possible to select what should be displayed in 3D Canvas.



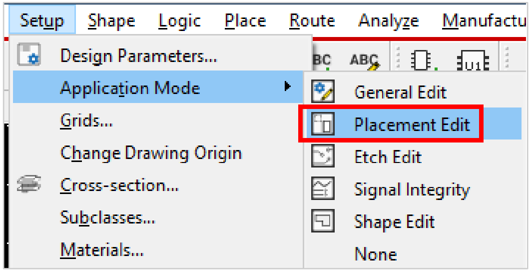
3D Canvas II

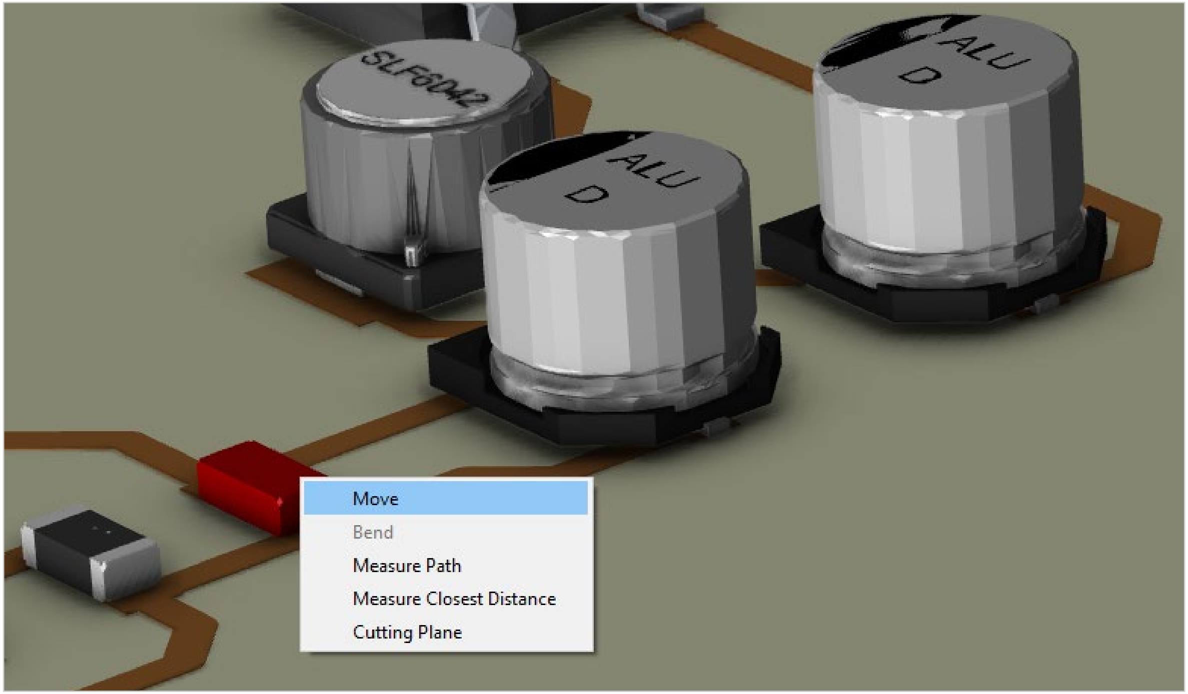
Define visual representation of parts under **Setup > Preferences > Symbol Representation**.



3D Canvas III

When PCB Editor is in **Placement Edit** Application Mode, parts can be moved in 3D Canvas using **RMB > Move**.





Routing

Routing

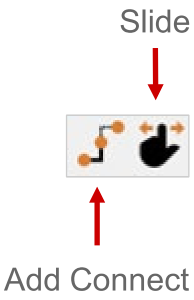
Routing is adding copper traces to the PCB based on the netlist. It can be performed interactively or automatically (with appropriate license).

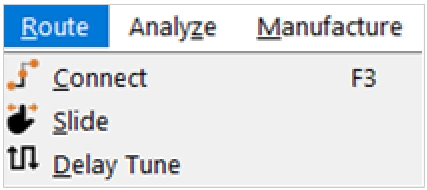
Both methods are available by icons or pull-down menus.

Add Connect (**Route > Connect**):	Manual routing of electric connections
Slide (**Route > Slide**):	Movement of existing traces
Create Fanout (**Route > Create Fanout**):	Creation of Fanout / Pin Escape
Custom Smooth (**Route > Custom Smooth**):	Trace optimization
Edit Vertex (**Edit > Vertex**):	Add / delete vertices of traces

Auto Route Param / Route (**Route > PCB Router > Route Automatic**):
Opens parameter form and start PCB routers in background.

In this tutorial we will focus on interactive routing.





Routing Grid

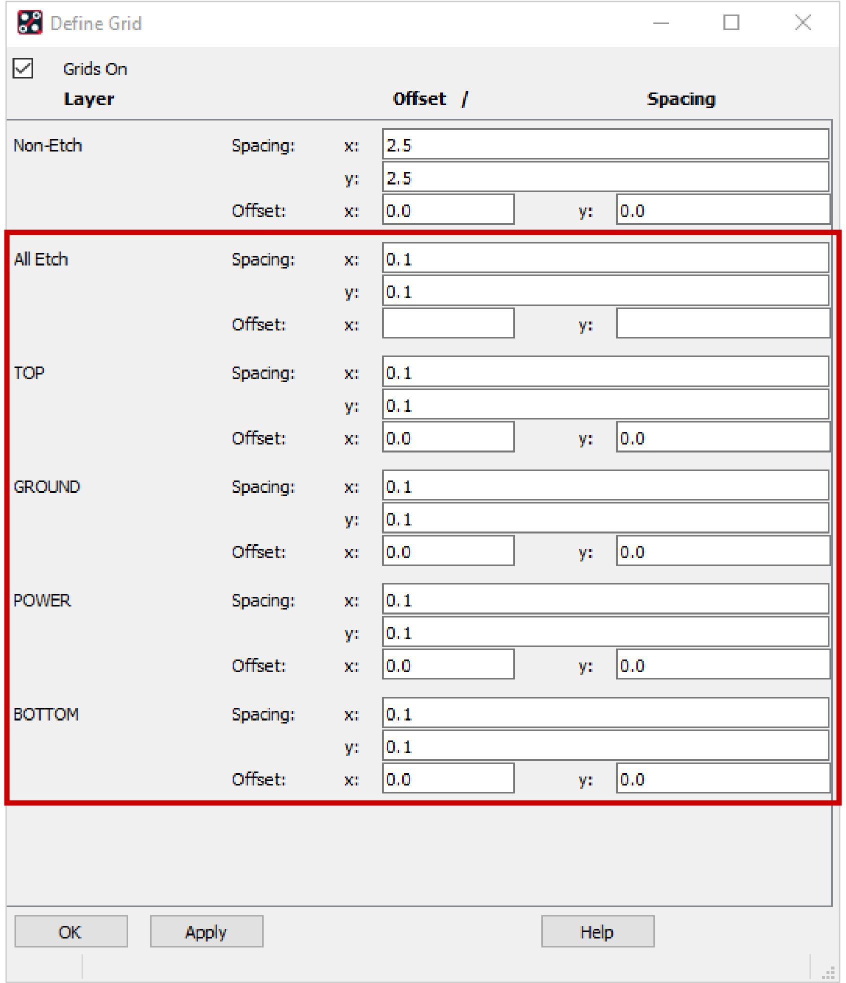
Etch grid will be immediately displayed if a route command like **Route > Connect** is executed. During interactive routing with the mouse it is used as snap grid.

Choose **Setup > Grids** and enter all values in section All Etch as displayed.

Grids On box does control visibility of grid.

Entries in **All Etch** apply to all layers.

If different grids on different layers are desired, you can enter grids for each layer.

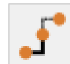


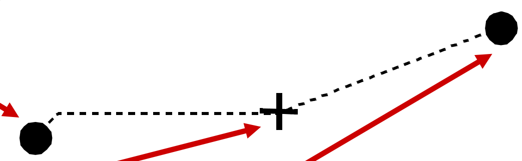
Attention

With different grids on different etch layers a via is only possible on a common multiplier grid.

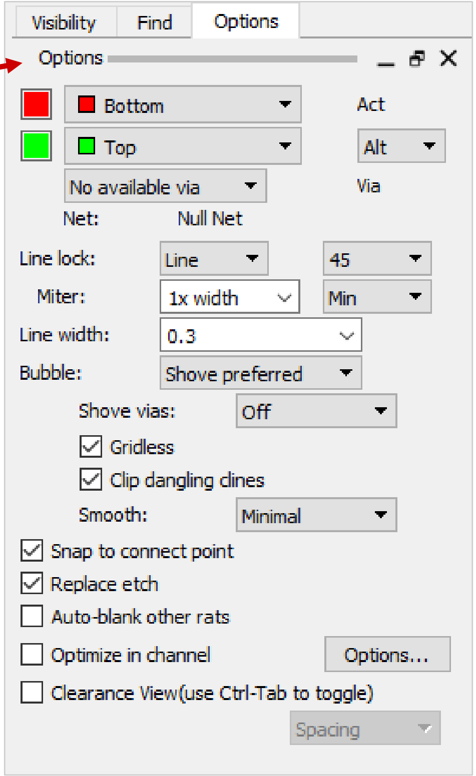
Lab: Routing

Routing:

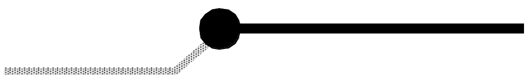
- Routing start via: **Route > Connect** or 
  - Routing behavior is defined on Options panel.
- Select start point with **LMB,** i. e. T1 Pin 9.



- **LMB** to fix planned path.
- **LMB** on endpoint to finalize trace.
- Another connection via **RMB > Next.**
- Finish connect command by **RMB > Done**.
- **RMB > Oops** undoes last step.
- **RMB > Cancel** will finish command without saving changes.



Adding Vias:

- **RMB > Add Via** or double click 
- Setting of used via and target layer will be defined in Options panel

Routing Options

In the chapter design rules we already discussed some pre-settings like trace width or trace spacing. When we start routing traces and online DRC is active, we already get support from the tool. The predefined trace width will be directly set as a parameter in the Options. We can change the trace width within defined tolerance. If tolerances are violated, we will immediately get a DRC warning from the system.

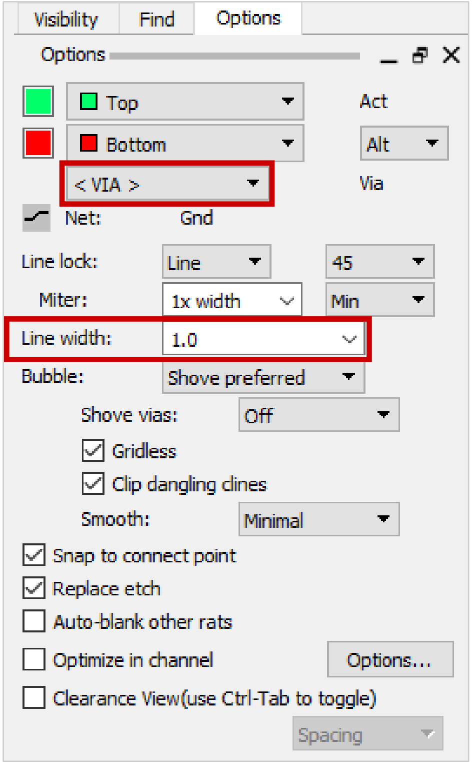
If command **Route > Connect** was started without a selected pin or guideline, Options panel will show default values:

Via: No available Via (because there is no net selected)

Net: Null Net (because there is no net selected)

Line width: 0.3 (default value, if there is no net selected)

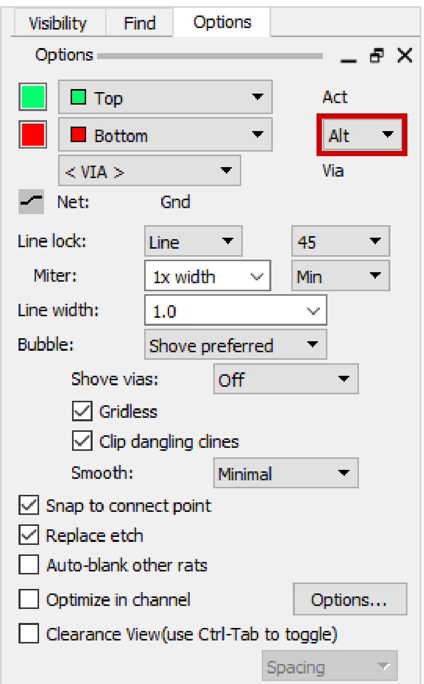
As soon as a net is selected (e.g. by clicking on a pin), the valid values for this net will be used.



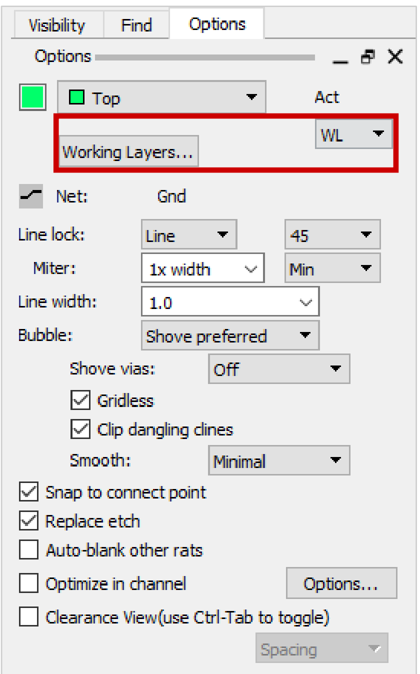
Alternate Mode / Working Layer Mode

In the **Alternate Mode** we select two layers in the Options panel. During routing it is possible to switch between these two layers.

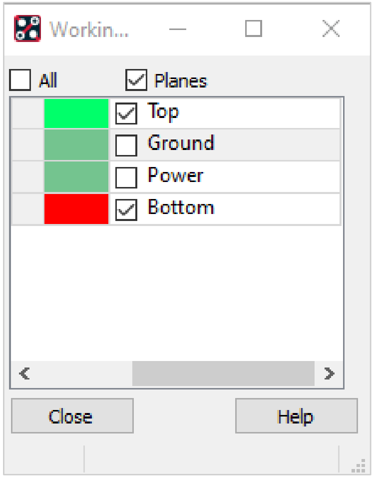
Working Layer Mode is useful for working interactively in high layer count multilayer boards. If this mode is activated, you can select the desired layer during interactive routing. If multiple layers are enabled a form will appear while setting a via to choose desired target layer. Plane layers can be completely excluded and disabled.



Alternate Mode



Working Layer Mode



Net and Line Options

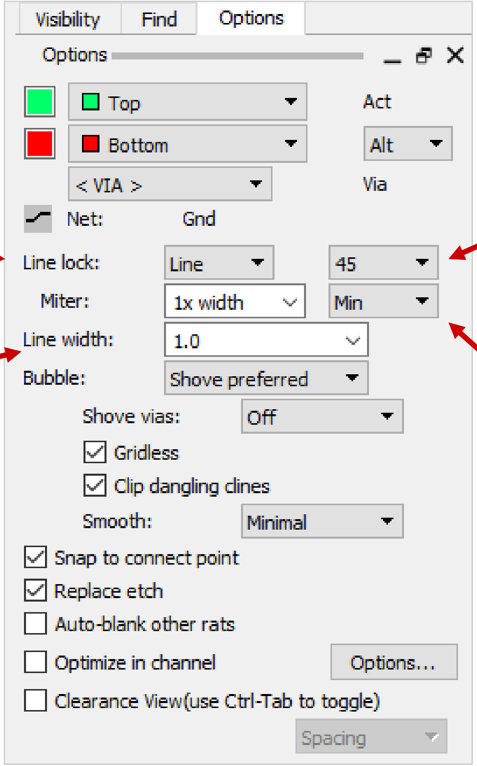
Line lock:

Line: Routing of straight lines

Arc: Routing of arcs

Line width:

If the net has a special **CSet** assigned, these values will be used. Otherwise default values from default Constraint Setup will be used.



Angle:

45 / 90: Fixed angle

Off: Any angle

Chamfer corners:

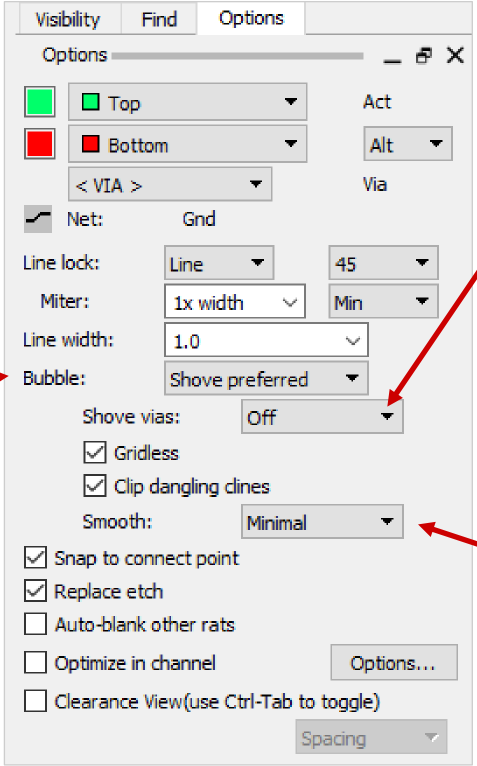
Min = no length limitation

Fixed = left value will be used (1 x width)

Tip

Please note that settings of parameter Line Lock and Miter influence each other. Also arcs can be impacted by Miter settings.

Push, Smooth



Bubble:

Setting defines behavior with existing traces.

Off: It will route over existing traces.

Hug Only: Line will align next to an existing trace.

Hug preferred: Line will prefer to align with existing traces.

Shove preferred: Other traces will be pushed.

Shove vias:

Off: Vias will not be moved.

Minimal: Vias will moved just a bit.

Full: Vias will be moved.

Smooth:

Off: Existing traces will not get touched and smoothened.

Minimal: Minimum smoothening of existing traces.

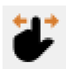
Full: Better smoothening

Super: Maximum smoothening

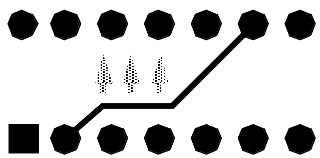
Editing of Existing Traces (I)

There are extensive possibilities to modify existing traces in PCB Editor.

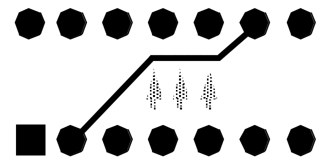
Route > Slide: Movement of traces adjacent to chosen settings

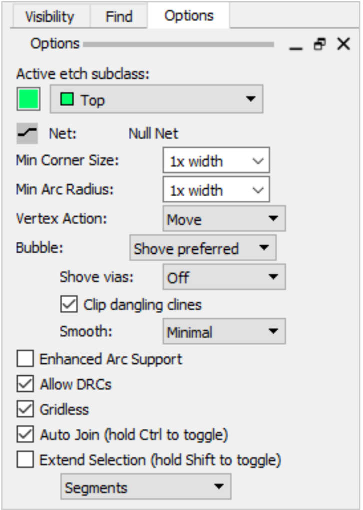


Before



After

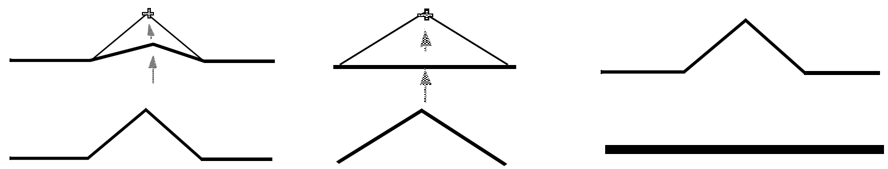




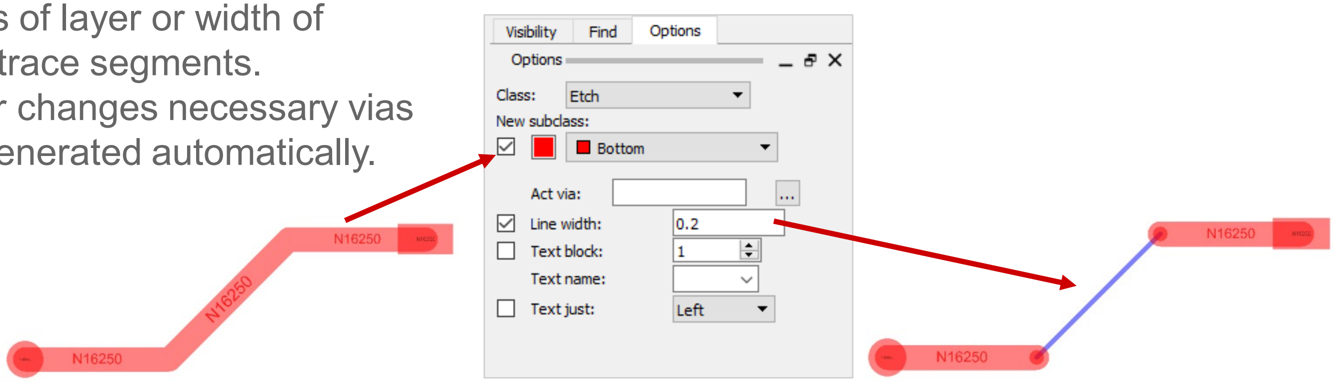
Edit > Vertex: New vertices or movement of existing vertices

Before

After



Edit > Change: Changes of layer or width of existing trace segments. For layer changes necessary vias will be generated automatically.



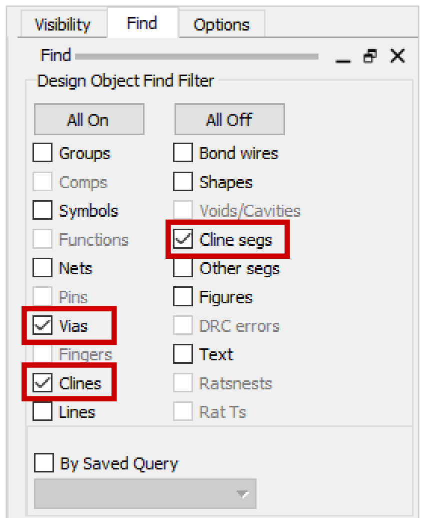
Editing of Existing Traces (II)

Delete: Deletes traces and vias

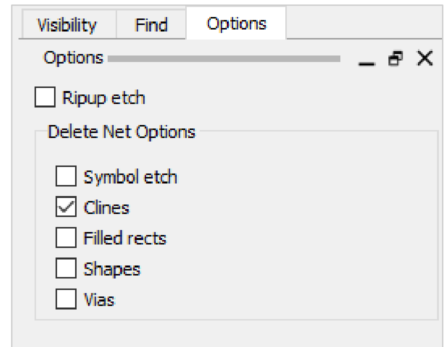
Cline Segs:
Deletes segments of a net

Clines:
Deletes all segments of a net with exception of vias

Vias:
Deletes vias



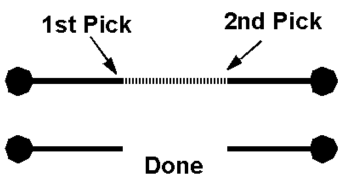
Ripup Etch:



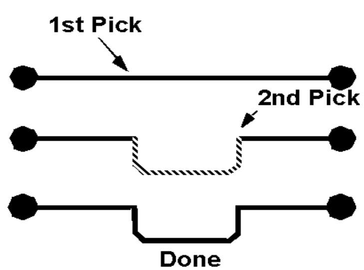
Use **Ripup etch** and **Clines** to delete all segments and vias between pins across multiple layers.

Cut option (**RMB > Cut**): Allows to select dedicated sections of a segment

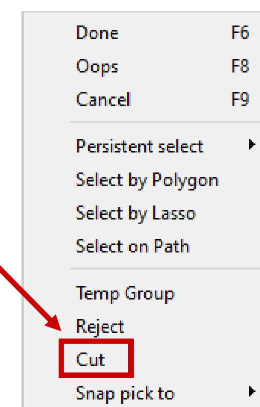
Edit > Delete



Route > Slide



Edit > Change (width)

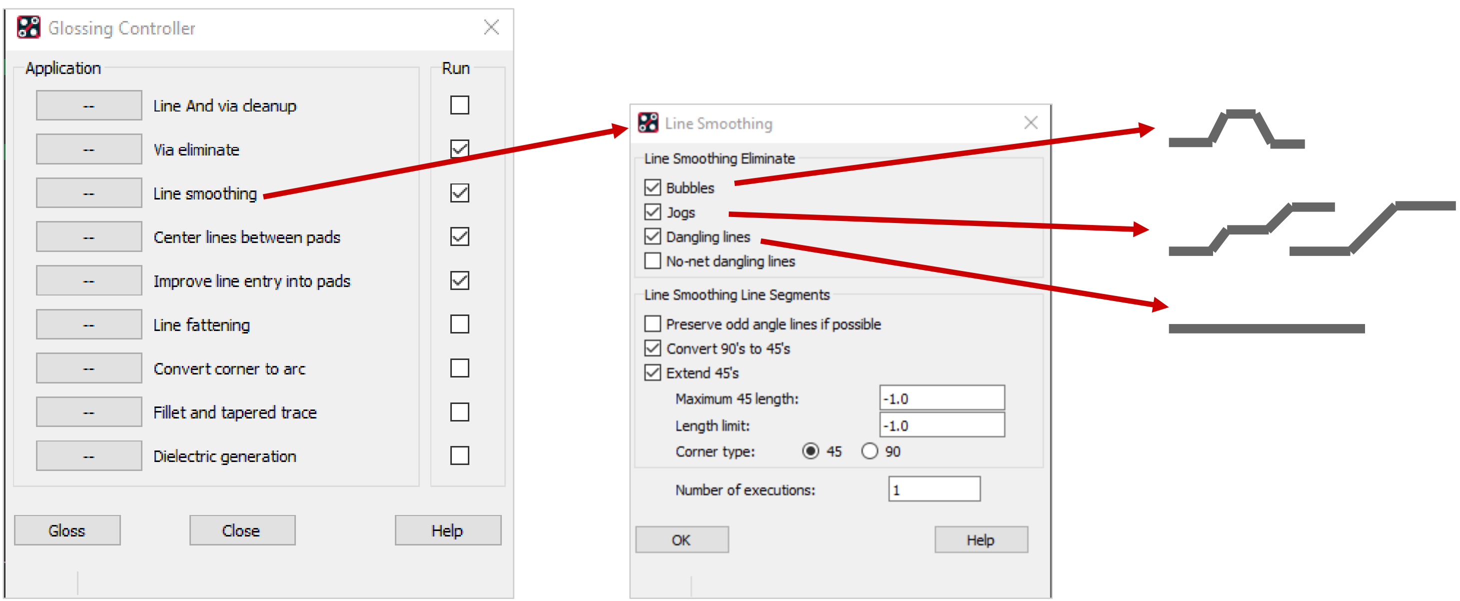


Glossing

Glossing is improving traces for manufacturing. Glossing can remove redundant bubbles, jogs and dangling lines automatically.

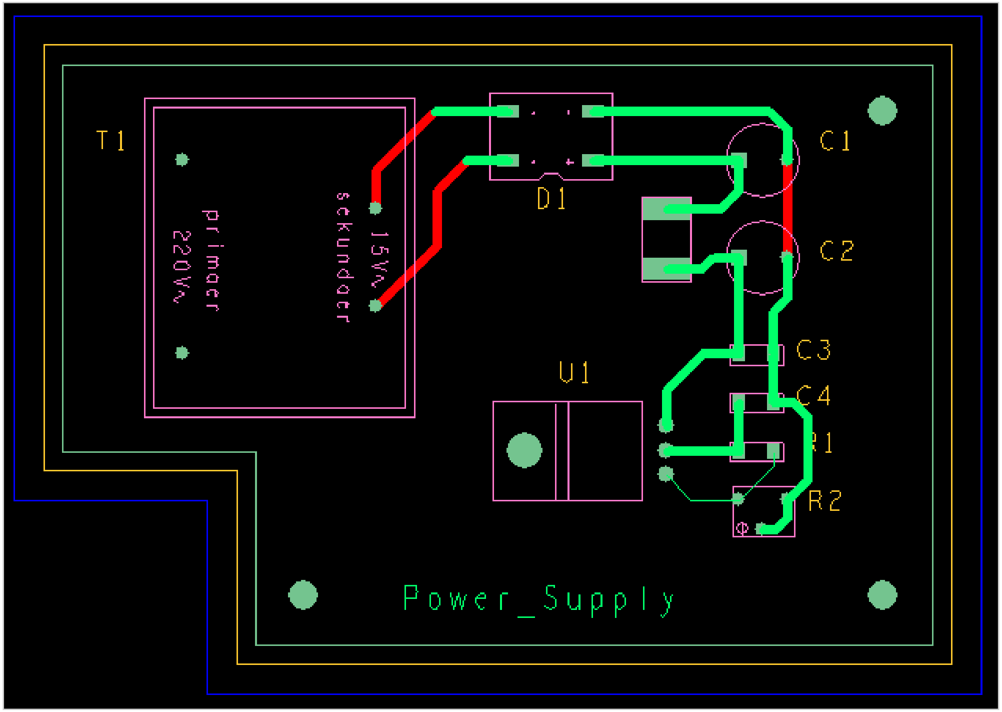
In addition OrCAD provides much more glossing capabilities which are not mentioned in this tutorial.

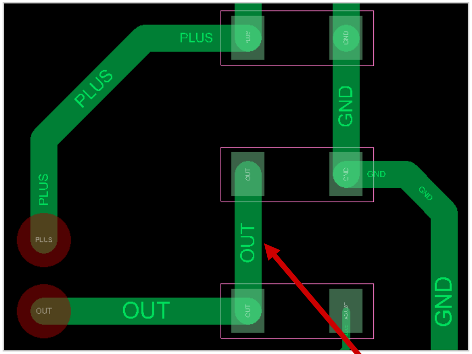
Route > Gloss > Line Smoothing…



Lab: Routing

1. Please load **placed.brd** from previous exercise and use learned skills to route the board according to the template.
   Red is Top
   Green is Bottom
2. Place the text **Power_Supply** on top layer.
3. Save the routed board under **routed.brd**.





Net names can be displayed under:
Setup > Design Parameters > Display > Display Net Names.

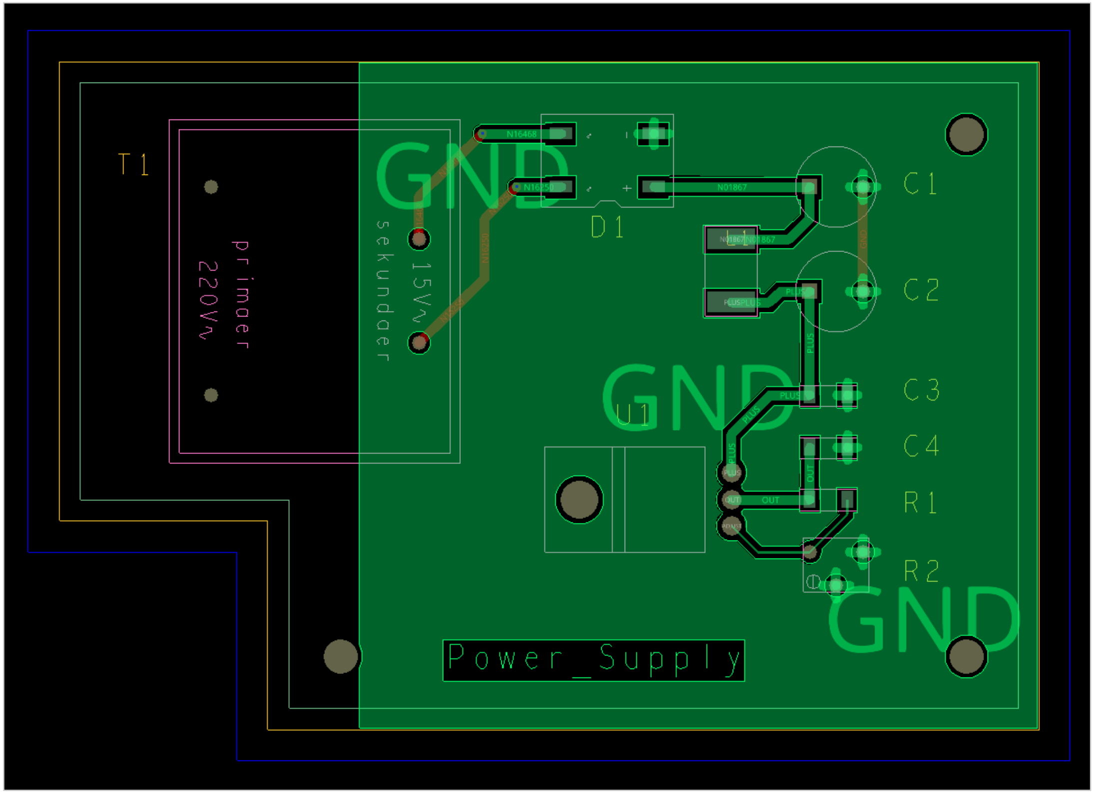
Copper Areas

FlowCAD

Copper Areas (Shapes)

Copper areas, in OrCAD called shapes, play an important role for power distribution and shielding.

PCB Editor can handle both, static and dynamic shapes. Dynamic shapes are recalculated in real time by any modification.

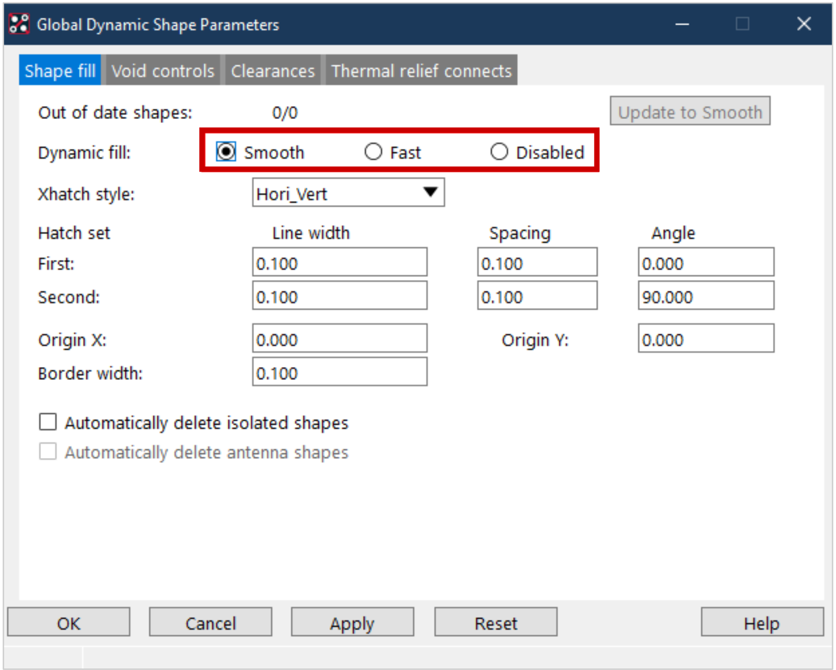


Tip

Usage of dynamic shapes is much more comfortable and safer.

Global Dynamic Parameters: Shape Fill

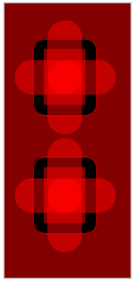
Under **Setup > Global Dynamic Params…** you can define ordinary parameters for all new shapes. If necessary, you can adjust parameters for each individual shape.



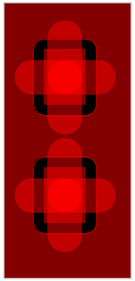
Tip

Hatch pattern shapes typically used for flex boards can be defined with **Xhatch** style.

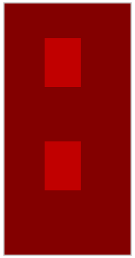
Dynamic fill:



Smooth corresponds gerber output.



Fast calculates shapes faster. The result will look similar to Smooth.



Disabled: Shapes don’t get recalculated.
Via **Update to Smooth** all shapes get recalculated.

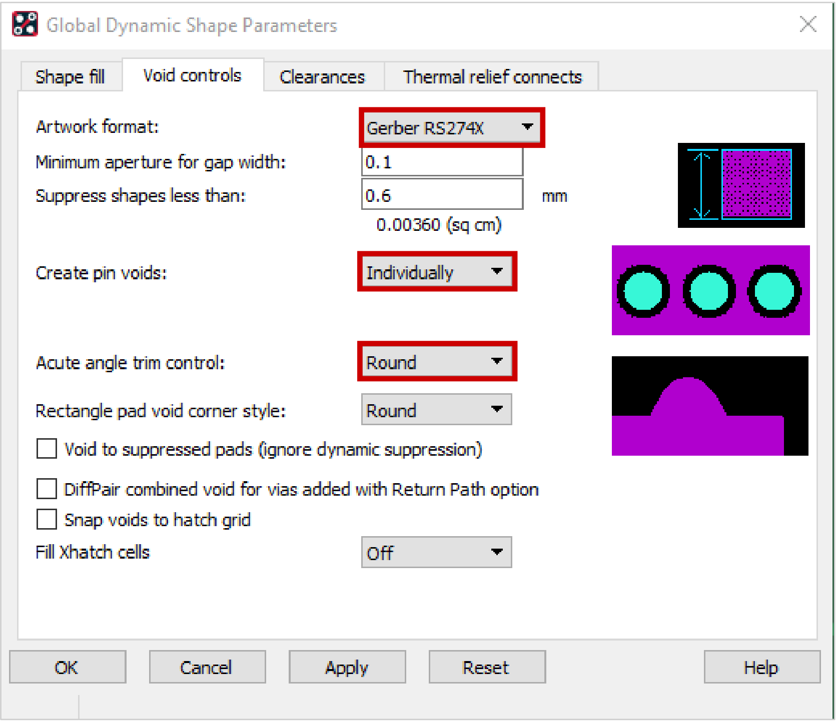
Global Dynamic Parameters: Void Controls

Settings in this section impact implementation of shapes.

Artwork format should be set to **RS274X**, this is industry standard. We will talk about artwork format related to manufacturing outputs in this chapter later.

Create pin voids:
Individual: Pins get individual cutouts.
In-line: cutout will be merged for more pins.

Acute angle trim control:
Does impact handling of corners depending on angle.

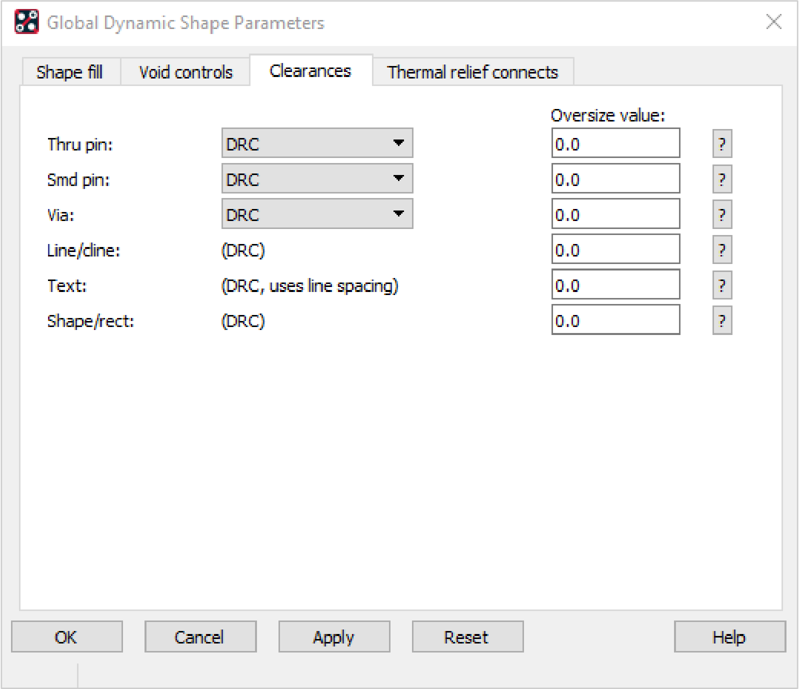


Tip

Generally, all shapes of a board have same format assigned. Therefore this bullet is excluded from individual parameters of shapes.

Global Dynamic Parameters: Clearances

Clearances define clearance (cut out) for each pad type. Default is DRC, meaning values from Constraint Manager are used.

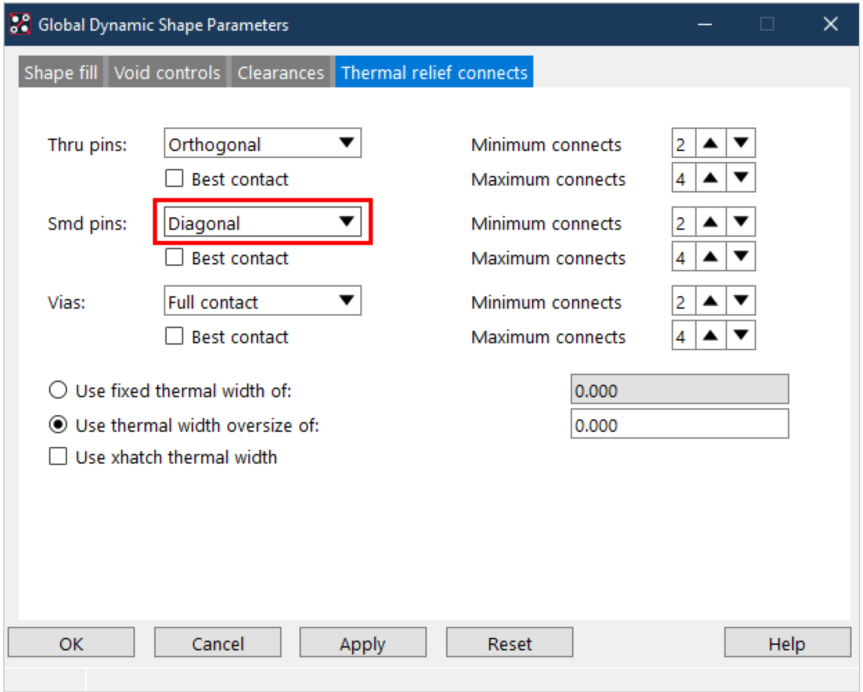


Tip

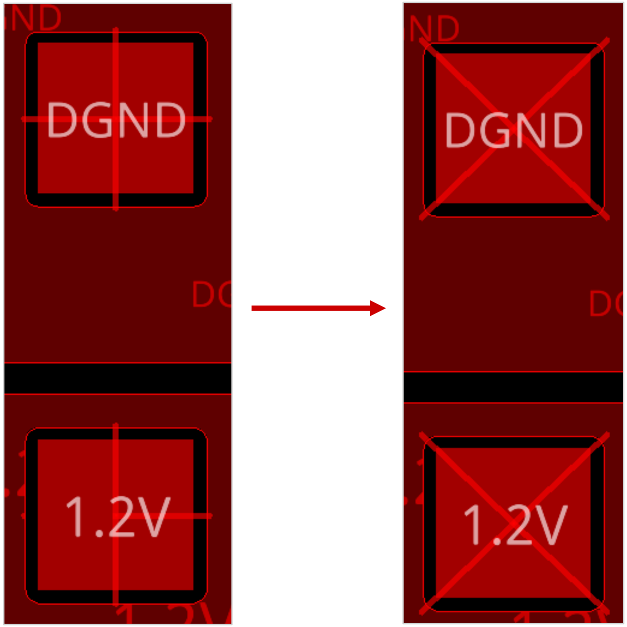
Please avoid oversized values.
Correct clearance values should already be defined in Constraint Manager.

Global Dyn. Param.: Thermal Relief Connects

Here you define thermal reliefs. There are different definitions for **Thru Pins, SMD Pins and Vias.**



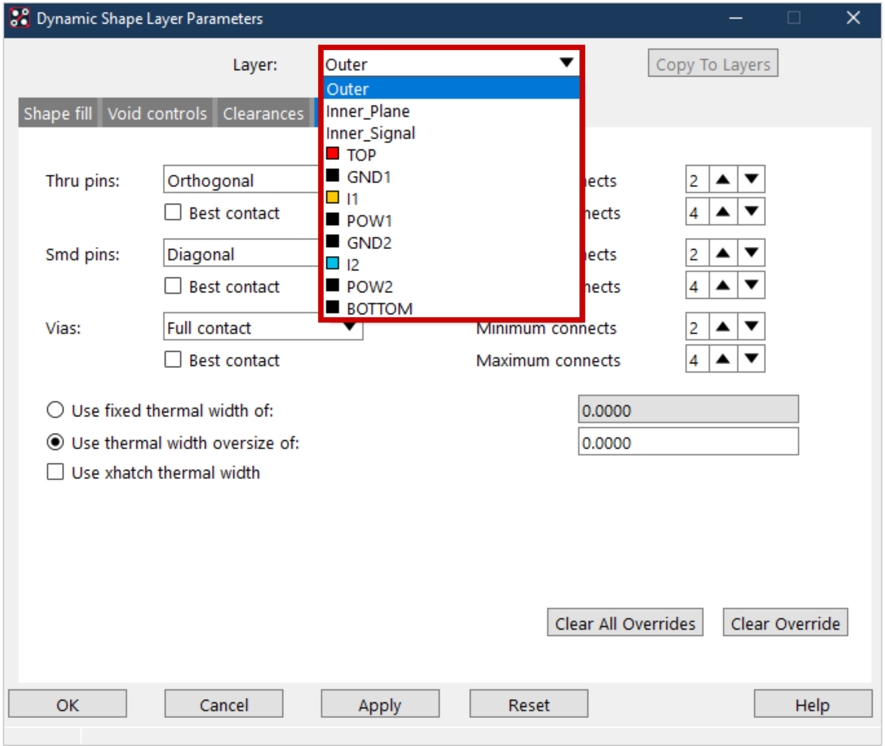
This value allows expansion of thermal reliefs compared to original design rules.



Shapes filled as Xhatch can use Xhatch line width also for thermal relief width.

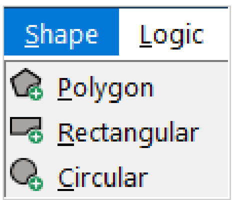
Layer Dynamic Parameters

Shape parameters can also be set individually for each layer via **Shape > Layer Dynamic Params**.



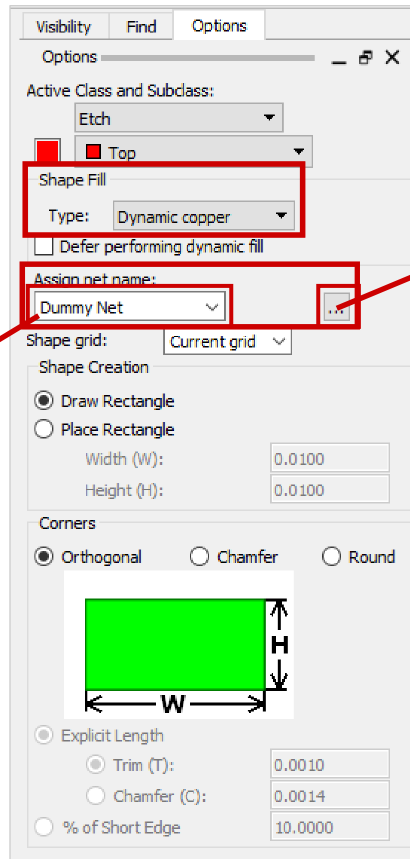
Adding Shapes

You can add shapes via the **Shape** menu.

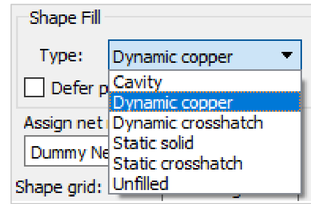


Shape Buttons:

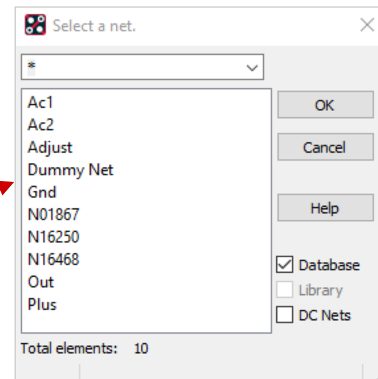
Shape Options:



Voltage supply nets that have the Voltage Property



You can choose between **Dynamic** and **Static** Shapes.



After outline definition **Dynamic Shapes** calculates shape automatically and keep clearances to all elements according to parameters. This will also be performed for every change.

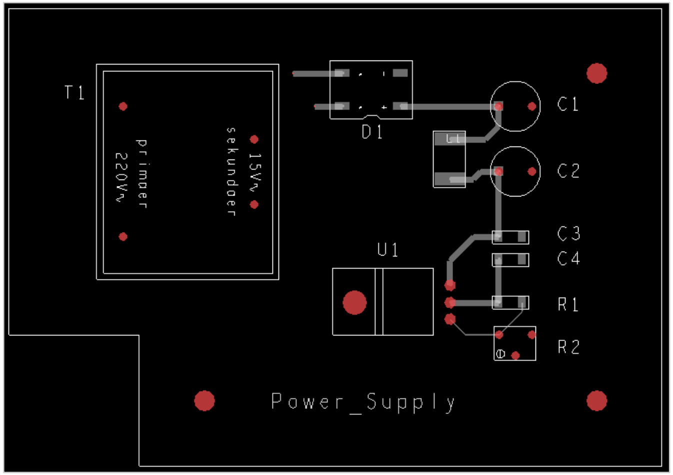
Tip

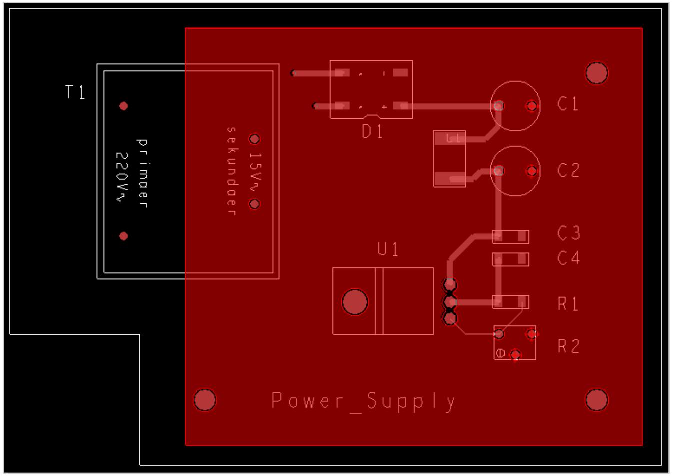
Please check points below before you generate shapes:

- **Global Dynamic Parameter**
- **Active Layer**
- **Chosen Net Name**

Lab: Shape Generation

1. Load board **routed.brd.**
2. Set gerber format under **Shape > Global Dynamics Parameters… > Void controls auf RS274X.**
3. Choose **Shape > Rectangle.**
4. Make ground layer visible **(Visibility).**
5. Set **Class** and **Subclass** to **Etch / GND.**
6. Set **Fill Type** to **Dynamic.**
7. Assign net name **GND** to the shape. Please use browser ... in option panel for this task.
8. Click **RMB** to define local parameters for the shape.
9. Drag a rectangle (2 x click with LMB) over right section of the board like illustrated.
10. Finish with **RMB** and Done.
11. Please note that shape outline is constraint by **Route Keep in** (yellow line). This results in a modified new shape outline.
12. Please repeat same procedure for Top layer.
13. Choose **Edit > Move** with filter on shape and move the shape. Please note that original shape contour is always in background preserved.



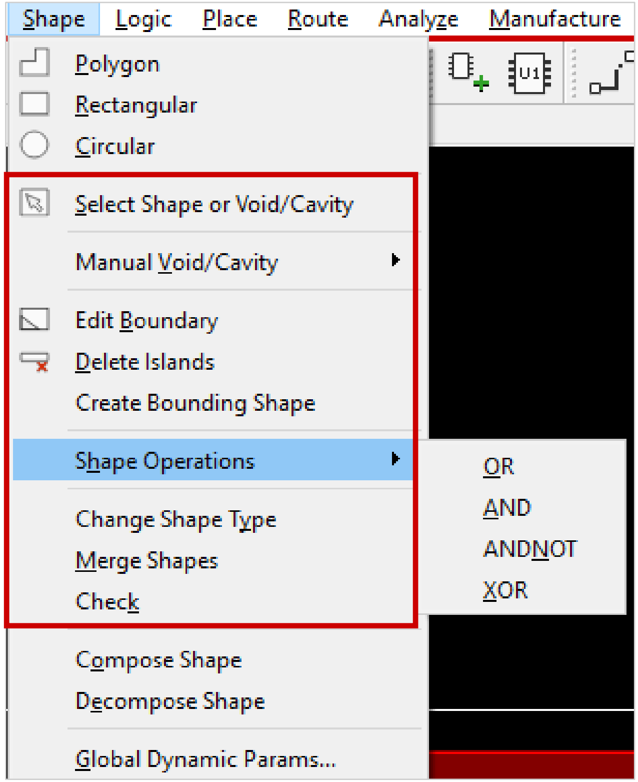


Shape Editing

In **Shape** menu many options for shape editing are available.

Tip

Please pay attention that you have set the correct layer in the options window for shape editing.
If necessary, you can assign a different net to a shape at any time.



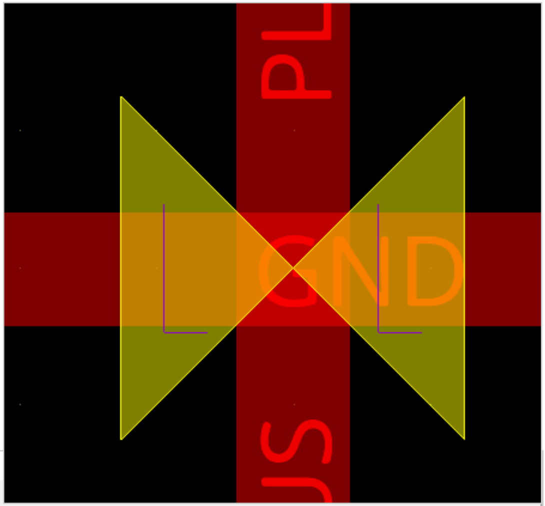
Design Rule Check and Reports

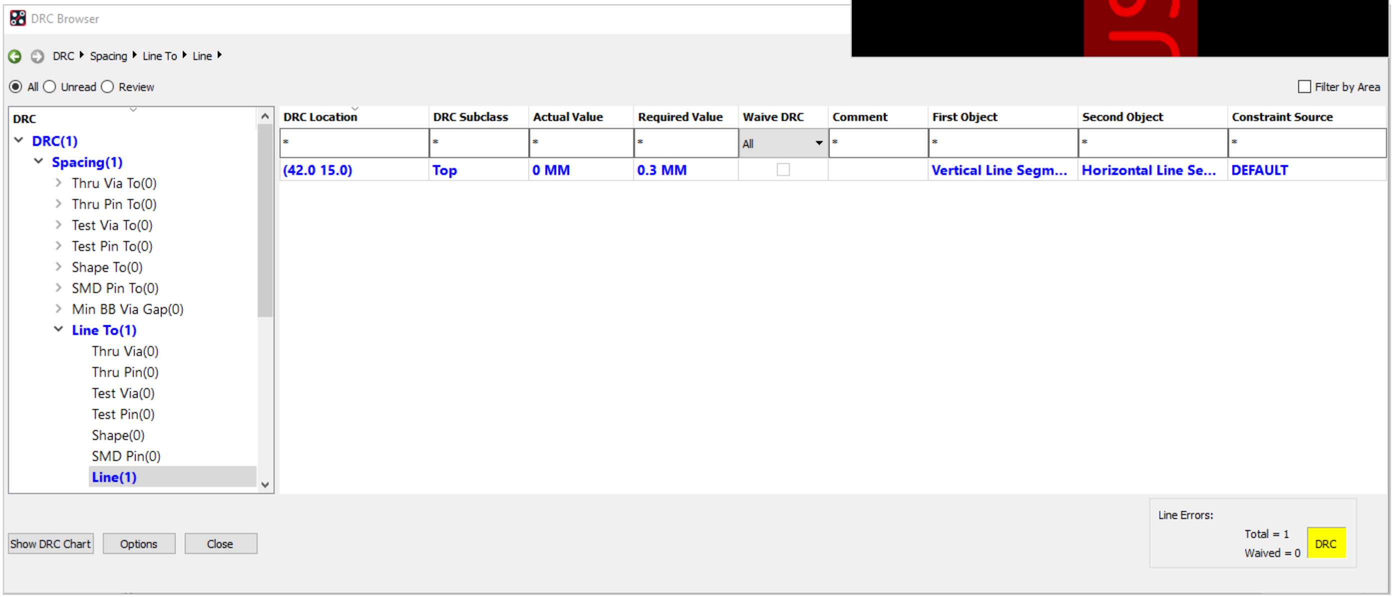
Design Rule Check

Violations of design rules get checked and marked online. Violations are marked with yellow DRC symbols (Butterfly symbol) like illustrated in the right picture. More detailed DRC information is available via **Display > Element** (set find filter to **DRC errors**).

All the DRC violations are listed in the DRC browser.
To open it use **Tools > DRC Browser**.

By double clicking on coordinates the location of DRC will be shown in work window.





Display Status

Pop-up menu Display **Status** gives you an overview of the design status.

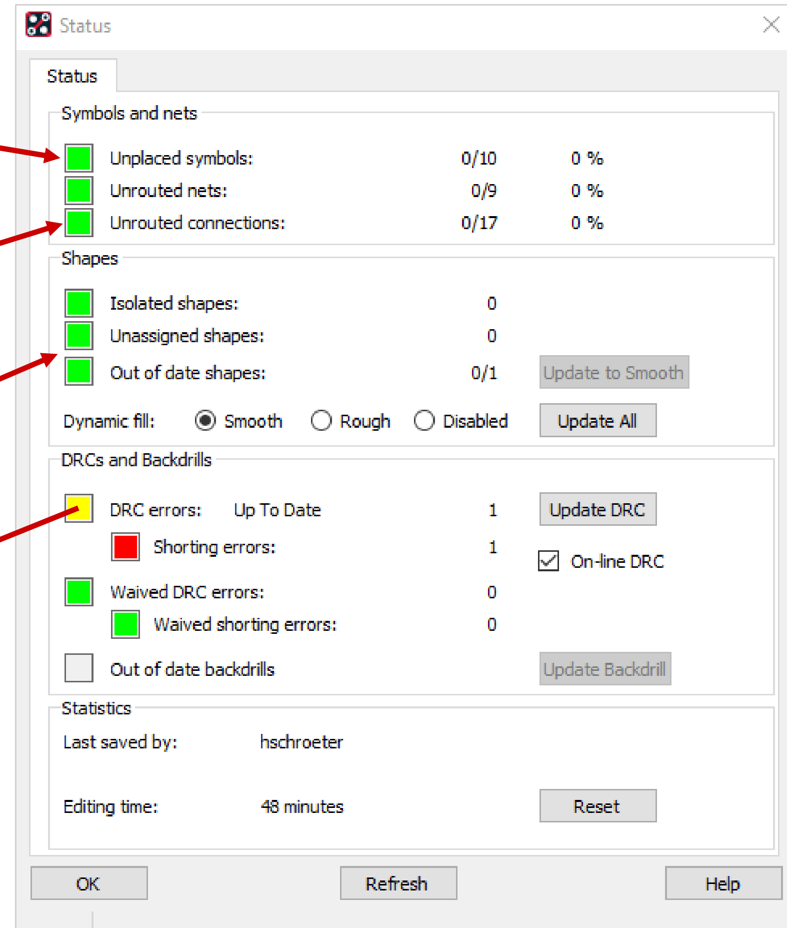
A click on the colored buttons gives you more details. Some options allow a cross selection or high light by clicking on the link in the report window.

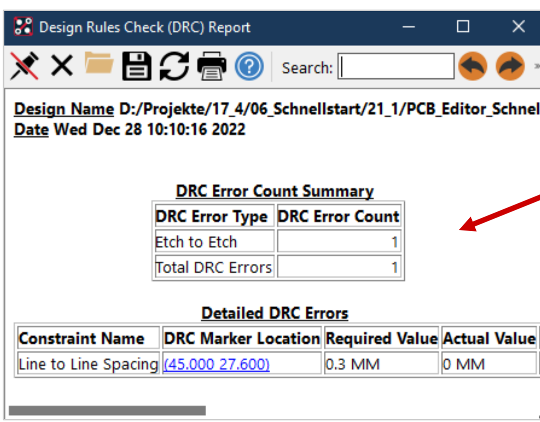
Are all components placed?

Are all nets routed?

Are all shapes error free?

Is DRC up to date and how many errors do exist?





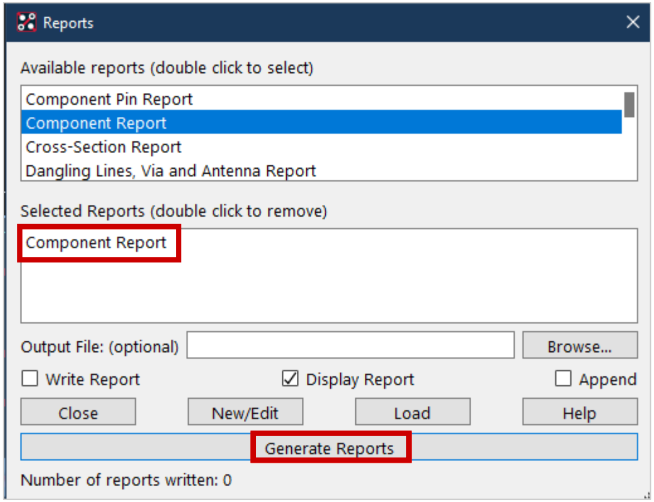
Reports

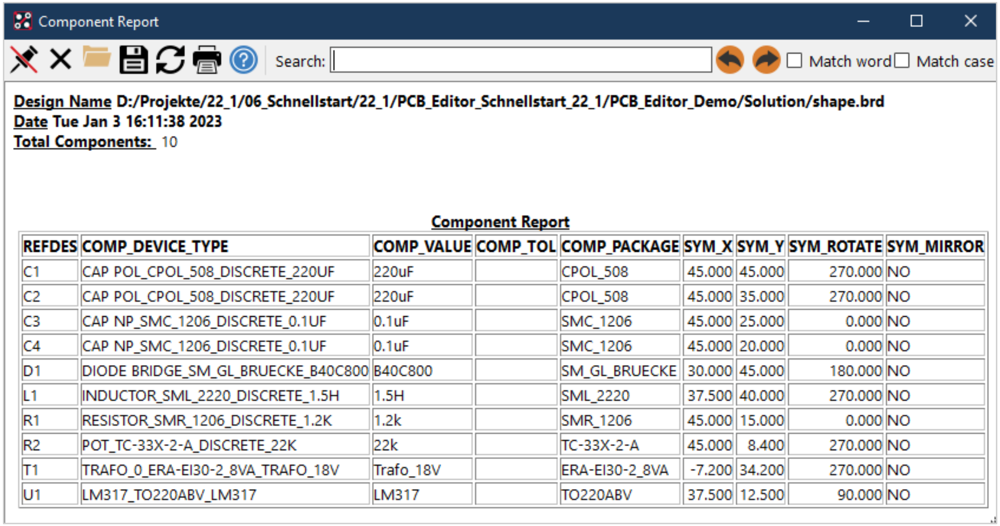
Another possibility to extract all possible information from the design are the reports. These can be created via **Tools > Reports**.

A very useful report is the **Component Report**. To select it, double-click on the desired report in the **Available reports** list at the top.

With **Generate Reports** the report is written.

You can also configure your own reports via **New / Edit**.





Design Name D:/Projekte/22_1/06_Schnellstart/22_1/PCB_Editor_Schnellstart_22_1/PCB_Editor_Demo/Solution/shape.brd
Date Tue Jan 3 16:11:38 2023
Total Components: 10

Component Report

REFDES	COMP_DEVICE_TYPE	COMP_VALUE	COMP_TOL	COMP_PACKAGE	SYM_X	SYM_Y	SYM_ROTATE	SYM_MIRROR
C1	CAP POL_CPOL_508_DISCRETE_220UF	220uF		CPOL_508	45.000	45.000	270.000	NO
C2	CAP POL_CPOL_508_DISCRETE_220UF	220uF		CPOL_508	45.000	35.000	270.000	NO
C3	CAP NP_SMC_1206_DISCRETE_0.1UF	0.1uF		SMC_1206	45.000	25.000	0.000	NO
C4	CAP NP_SMC_1206_DISCRETE_0.1UF	0.1uF		SMC_1206	45.000	20.000	0.000	NO
D1	DIODE BRIDGE_SM_GL_BRUECKE_B40C800	B40C800		SM_GL_BRUECKE	30.000	45.000	180.000	NO
L1	INDUCTOR_SML_2220_DISCRETE_1.5H	1.5H		SML_2220	37.500	40.000	270.000	NO
R1	RESISTOR_SMR_1206_DISCRETE_1.2K	1.2k		SMR_1206	45.000	15.000	0.000	NO
R2	POT_TC-33X-2-A_DISCRETE_22K	22k		TC-33X-2-A	45.000	8.400	270.000	NO
T1	TRAFO_0_ERA-EI30-2_8VA_TRAFO_18V	Trafo_18V		ERA-EI30-2_8VA	-7.200	34.200	270.000	NO
U1	LM317_TO220ABV_LM317	LM317		TO220ABV	37.500	12.500	90.000	NO

Manufacturing Outputs

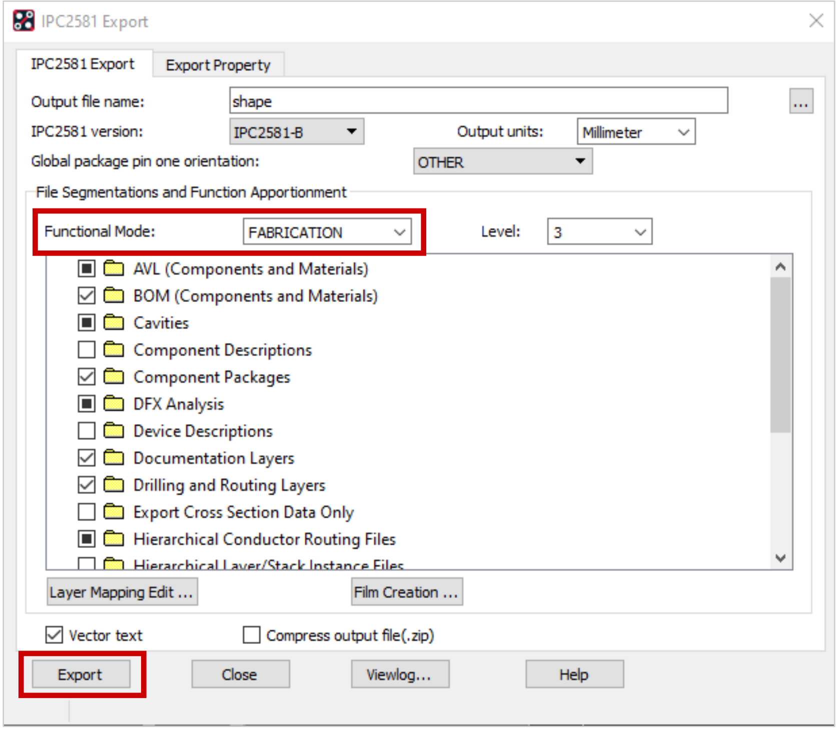
PCB Manufacturing Data – IPC-2581

In addition to classic output data like Gerber and drill data, PCB Editor is able to export IPC-2581 and ODB++.

IPC-2581 as well as ODB++ container can includes all necessary data for PCB bare board manufacturing and assembly.

Generate IPC-2581 via **File > Export > IPC 2581.**

Functional Mode allows to choose whether data should be written for PCB bare board, assembly or other manufacturing steps.



Manufacturing Output – Gerber Data

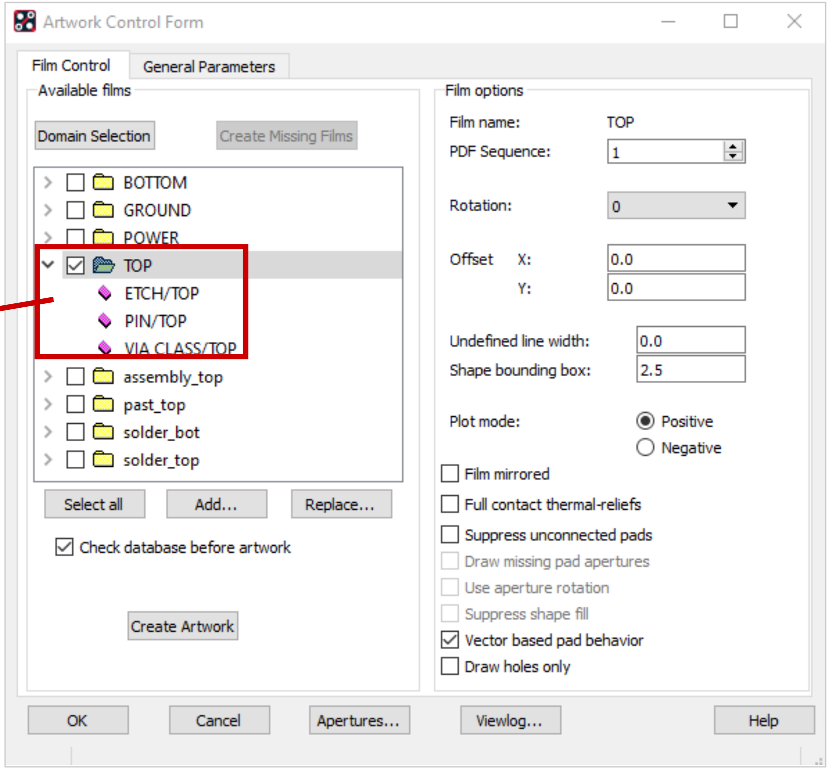
Classic output for manufacturing data consisting of Gerber (artwork) and drill data (NC drill) is divided into two parts.

For Gerber output of different Gerber layers the necessary data will be assembled from PCB design database (xyz.brd).

For example Gerber data for layer Top is assembled from design data Etch / Top, Pin / Top und Via Class / Top.

Film definitions described here are also used in IPC-2581 and ODB++.

Top.art



Lab: Gerber Data (I)

Manufacture > Artwork opens user interface for Gerber data output. In tab **General Parameter** base settings for output are defined.

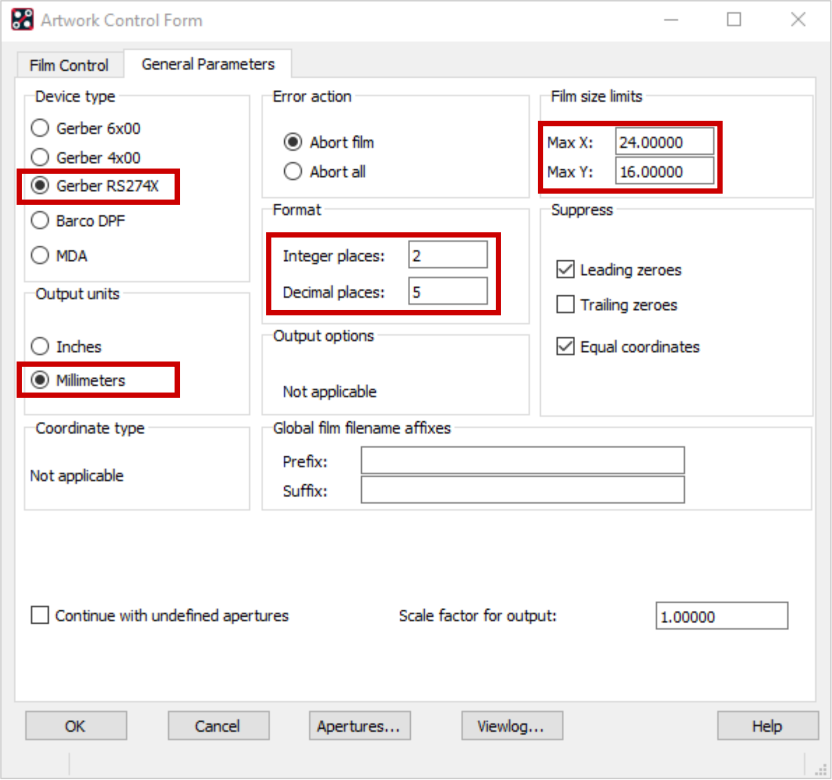
Please use following settings:

Devicetype (photo plot model):
Gerber RS274X – extended Gerber

Film size limits (available plot size):
Film size: 24 x 16 mm

Format (Integer / Decimal places):
Digits before / after the decimal point: 2.5

Output Units (units for the output):
Millimeters



Tip

Please use Extended Gerber (RS274X), this format contains apertures.

Use the same units in board and outputs.

Do not use too low resolution (decimal places).

Artwork Film Options

Chosen options will be stored for each film record.

Filename: Name of film

PDF Sequence: Number of film in the pdf output

Rotation: Film rotation, typically 0 degree

Offset: x / y offset

Undefined line width: Photo plot width for lines without dimensions. Always choose a value to avoid that structures will not be part of output data.

Shape bounding box: For negative planes, copper area will be generated with a negative offset related to entered value.

Plot mode: Negative, only for negative planes used

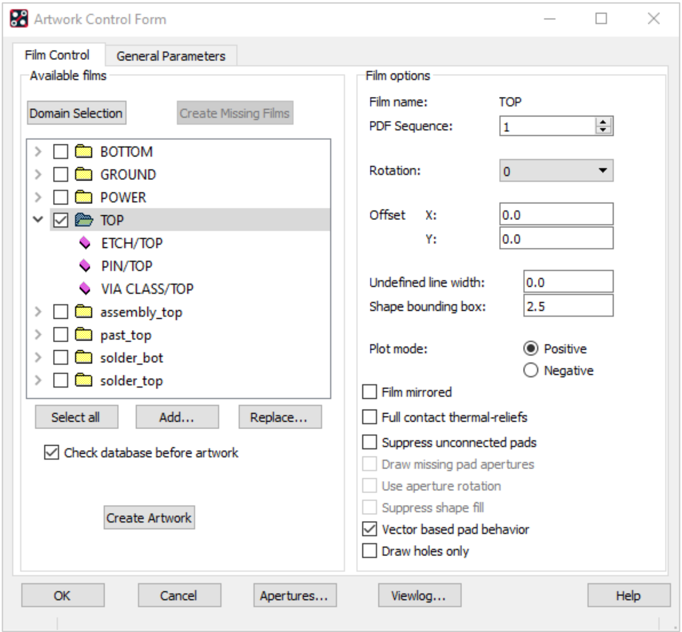
Film mirrored: Not standard (depends on bare board manufacturer)

Full contact...: Suppress thermal reliefs on copper planes

Suppress …: Suppress unconnected pads

Vector based …: Laser plot behavior like vector plotter flashing for pads

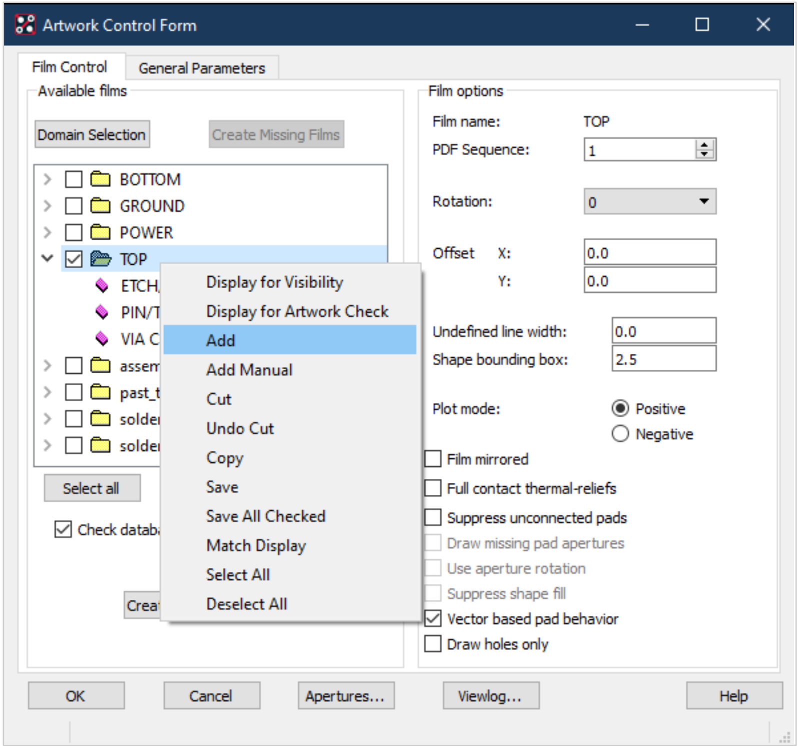
Draw holes only: Generation of shapes for drill holes. Applies only if only pins and / or vias on film are assigned.



Lab: Gerber Data (II)

In **Film Control Panel** all film records required for the output must be defined. By default, all film records defined under **Setup > Subclasses… > Etch** appear here. Additional film records like soldermask_top, assembly top etc. must be defined additionally.

- Set desired layers visible and all other layers hidden under **Display > Color Visibility** to define a new film.
- When you choose **RMB > Add** in Artwork Control Form, all visible layers will be combined to one film.



Lab: Drill Data

Menu to generate drill files: **Manufacture > NC > NC Drill**

Auto tool select: Requires an extra file named **nc_tools.txt** for automated tool change of drilling machine.

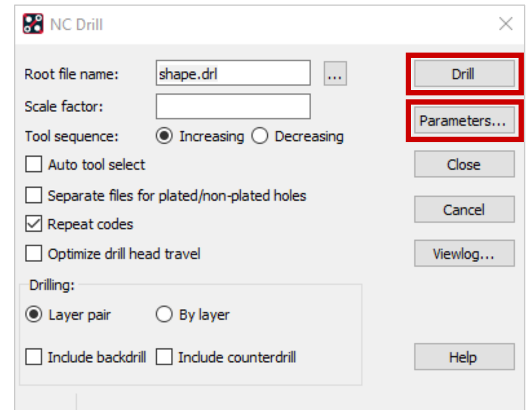
Separate files for ...: Separated files for plated and non plated drill holes.

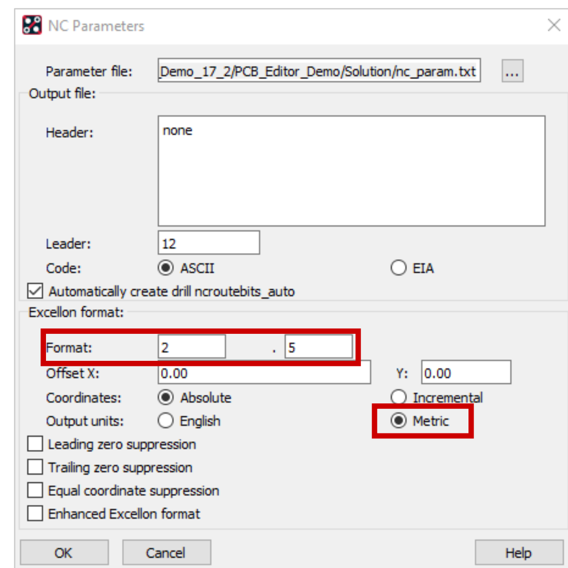
Repeat Codes: Should stay switched on.

Optimize drill …: Optimization of tool travel path. Format and output units should be similar like settings for Gerber files.

You can find more settings under **Parameters**.

Drill will start generation of drill data.



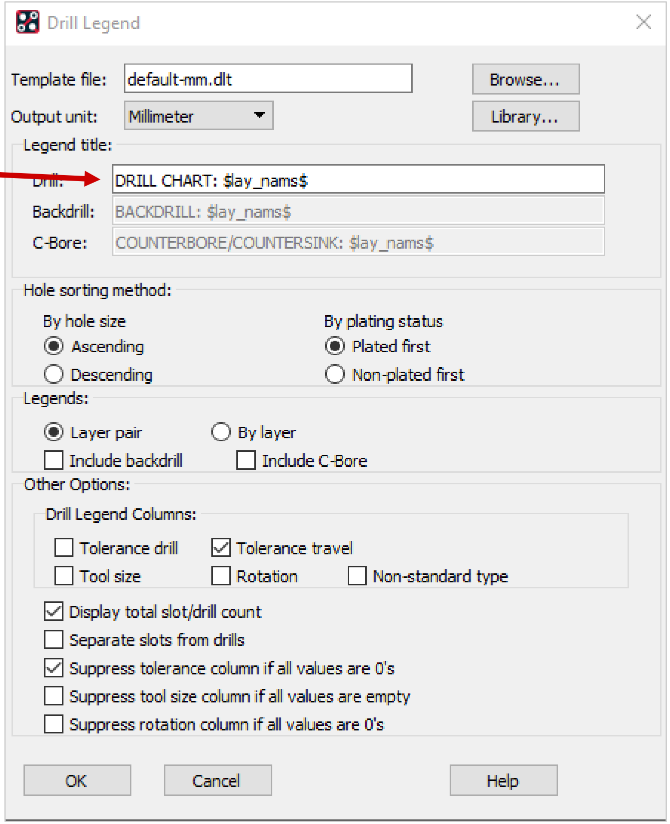


Documentation: NC Drill – Table

- A a drill table can be added to the layout by **Manufacture > NC > Drill Legend**.
- By **Library** you can choose different templates files for different units.
- For blind and buried vias the system automatically generates multiple drill charts.

Title of table and layer combination

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
•	13.0	PLATED	506
◇	31.0	PLATED	12
+	38.0	PLATED	122
△	75.0	PLATED	8
□	110.0	NON-PLATED	5



Tip

If find filter is set to group, the drill legend can be moved as one object.

Board Templates

Board Templates

This chapter gives a rough overview of how to create a mechanical board symbol or a board template. Board templates are useful if same board geometries and setup are used in several design (outline, technology, or preplaced components).

A **mechanical board symbol** typically contains following elements:

- Boardoutline, keepin / keepout (route and package) via keepout, dimensioning
- Mounting holes

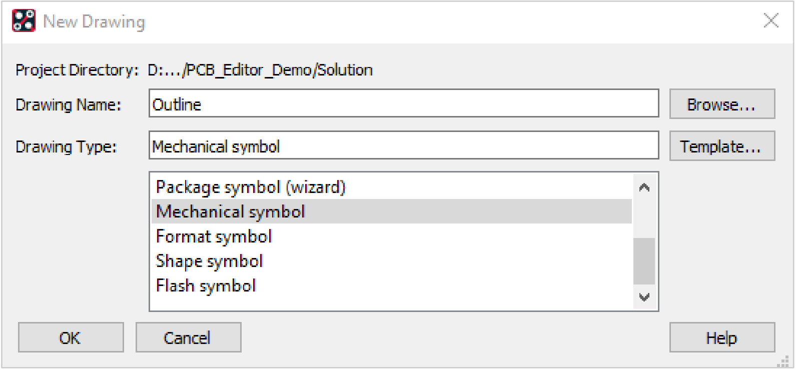
A **Masterboard** can contain the following elements:

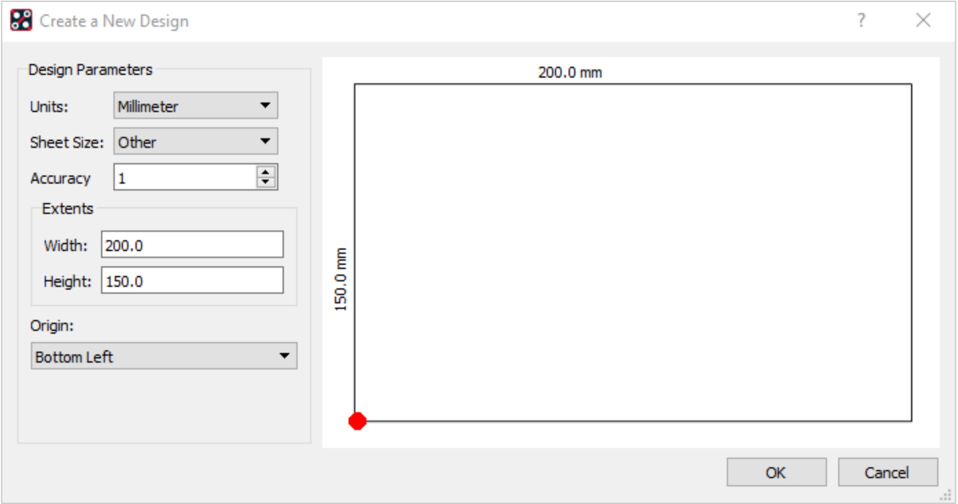
- Board symbol (.bsm)
- Drawing frame (.osm)
- Preplaced components, i.e. connectors (.psm)
- Technology constraints (clearance rules, trace with, etc.)
- Layer stack

Lab: Board Symbol

Follow the steps below to generate a board symbol:

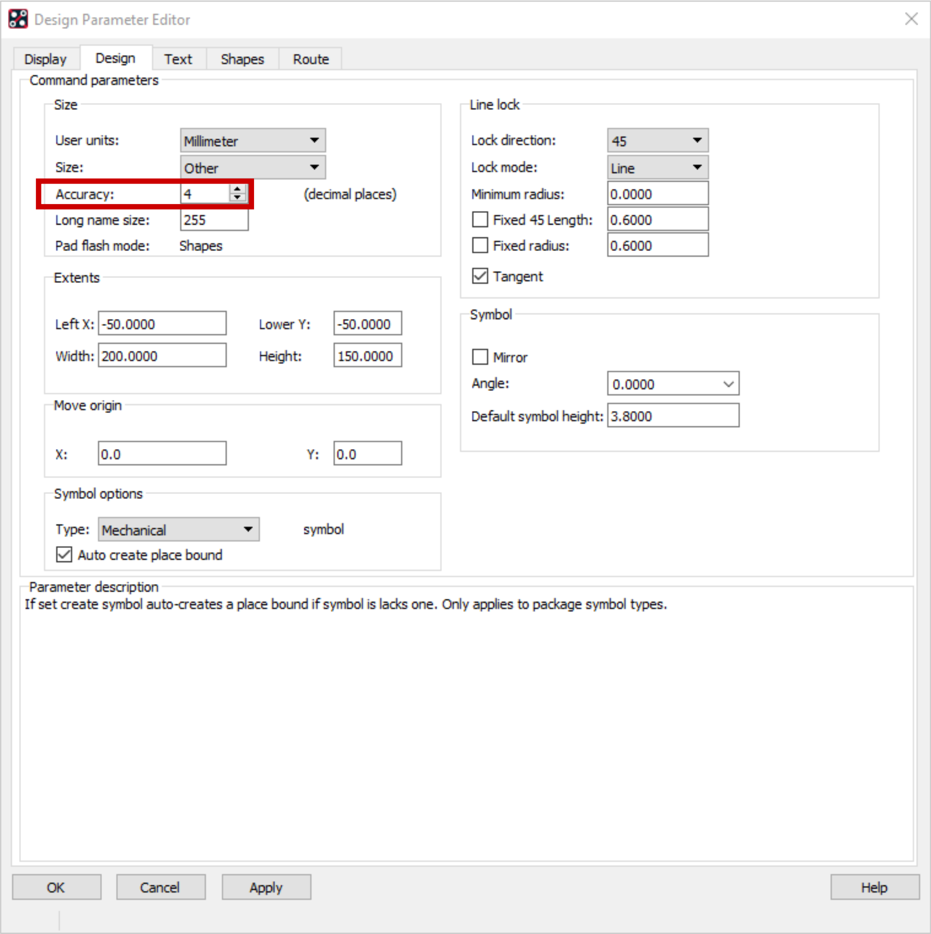
- **File > New > Mechanical Symbol**
- Enter **Outline** in Drawing Name field.
- **OK**
- Define units and dimensions of drawing page in dialog **Create a New Design**, which will appear automatically.
- **OK**





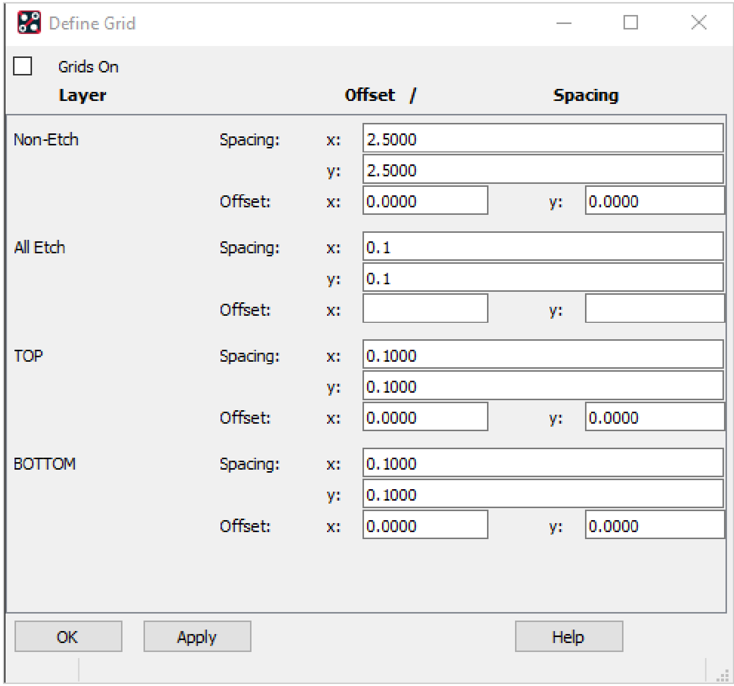
Lab: Board Symbol

- All other settings can be defined under **Setup > Design Parameters… > Design.**
- Precision of database should be high enough.



Lab: Board Symbol

- **Setup > Grids**
- In **Non Etch** section enter 2.5 for x and y.
- **OK** to close form.



Lab: Board Outline Generation

For our lab we assume that origin (0.0) of outline is the mounting hole on bottom left.

1. **Add > Line** from main menu.
2. Set active class and sub class to **Board Geometry / Outline.**
3. Please enter lines below in command line of editor and finish every line with **Enter**.

   x -30 10

   x -10 10

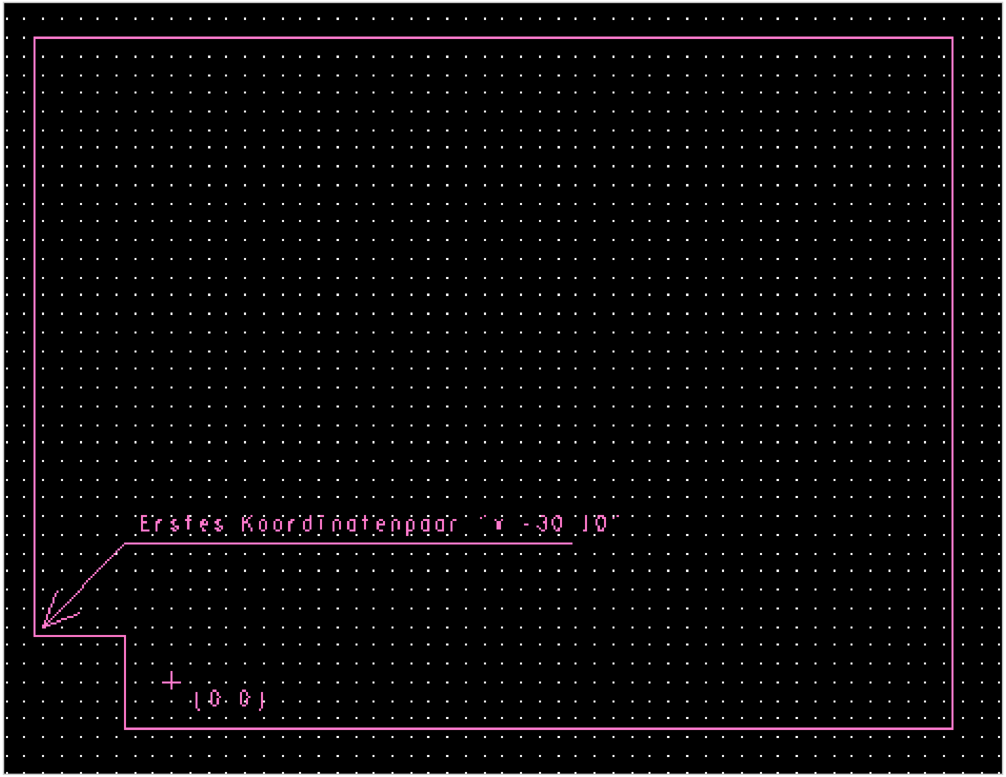
   x -10 -10

   ix 80

   iy 70

   ix -100

   iy -50
4. **RMB > Done.**
   Outline should look like illustrated in picture.



Tip

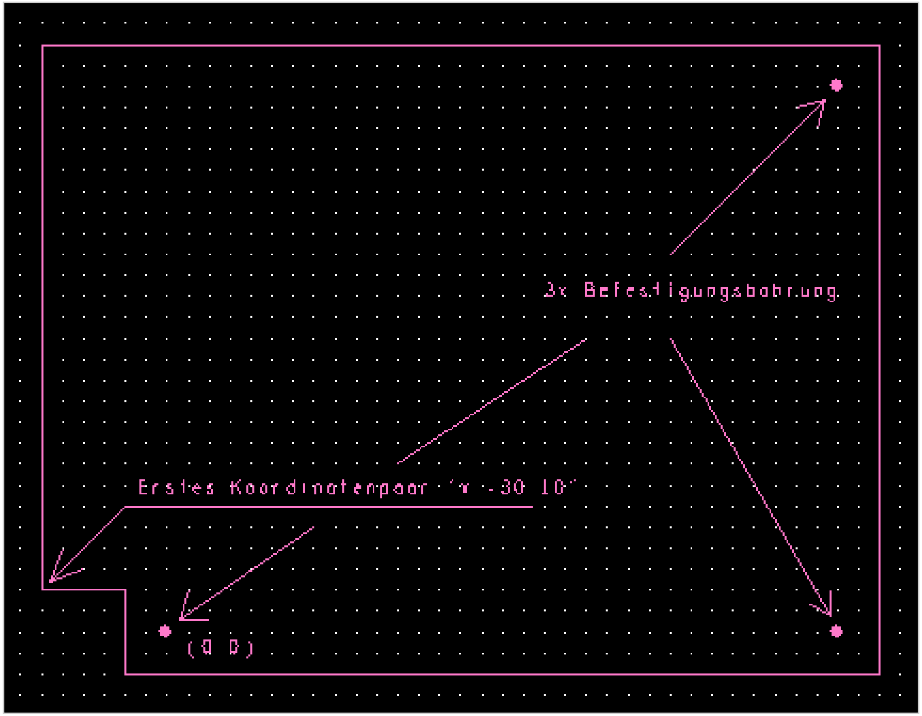
Absolut coordinates: x value value
Relative coordinates: ix or iy value

Lab: Mounting Holes

Second step is adding mounting holes.

1. **Layout > Pin** from main menu or via **Add Pin** icon
   Click Browse button ... in option window **Padstack** field.
2. Select **Hole120**
   Editor shows the message using **Hole120.pad**, meaning it was possible to find the pad in the library.
3. Please enter the data below, one after another in the command line, and confirm each line with **Enter**.

   x 0 0
   x 60 0
   x 60 50
4. **RMB > Done.**

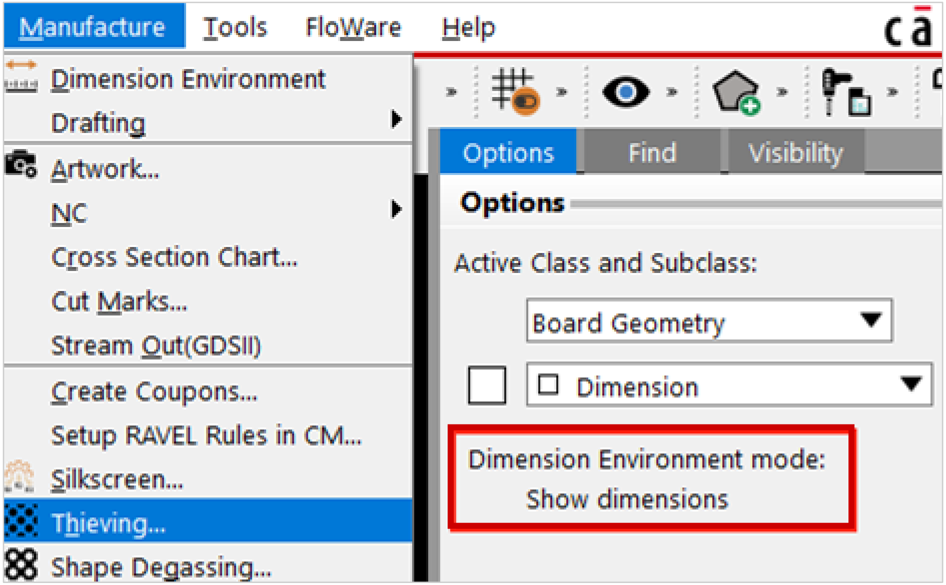


Lab: Dimensioning (I)

Third step is dimensioning. PCB Editor provides dynamic dimensioning. A change of contour triggers an automated update of dimensioning. Dimensioning can be entered in **PCB** or in **Symbol**. Usage is identical.

When working in a brd file in PCB Editor use: **Manufacturing > Dimension Environment**

When working in a mechanical symbol in Symbol Editor use: **Dimension > Dimension Environment**.

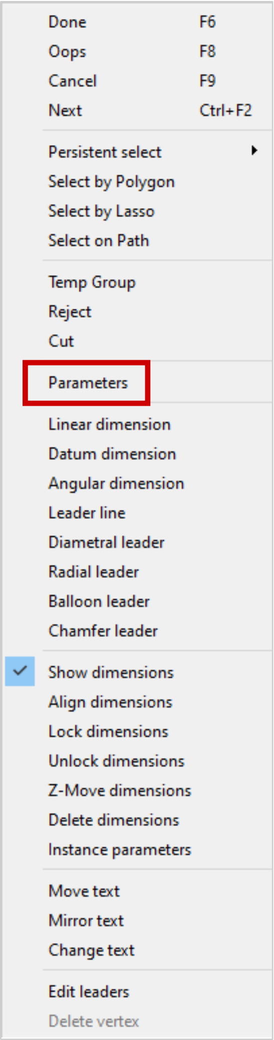


Lab: Dimensioning (II)

All commands for dimensioning are accessible by **right mouse button (RMB)**.

Next, we will use dimensioning on the outline example (mech. symbol).

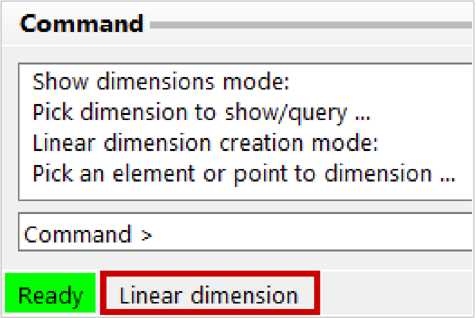
The Dimensioning can be adjusted by the parameters settings in the right mouse button menu.



Tip

When working with dimensions, please make sure that you always remain in the Dimension Environment. Otherwise the dimensions cannot be edited.

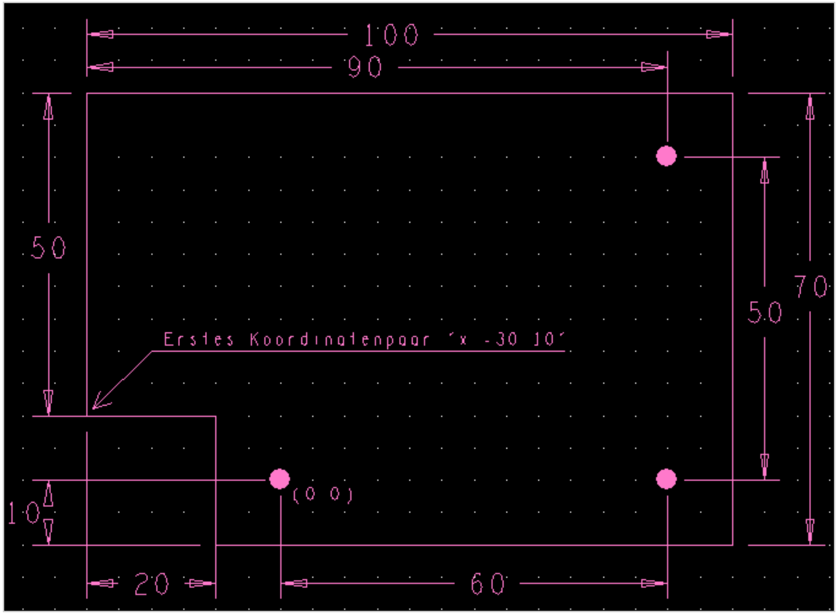
You can recognize this best by the status line.

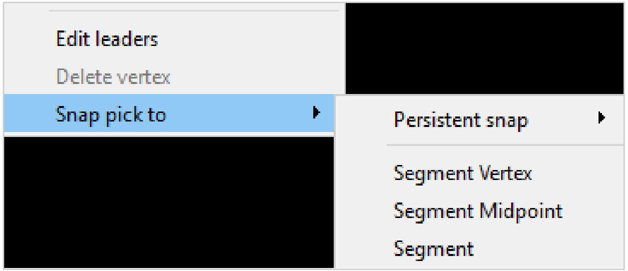


Lab: Dimensioning (III)

After parameter setup you can start with:

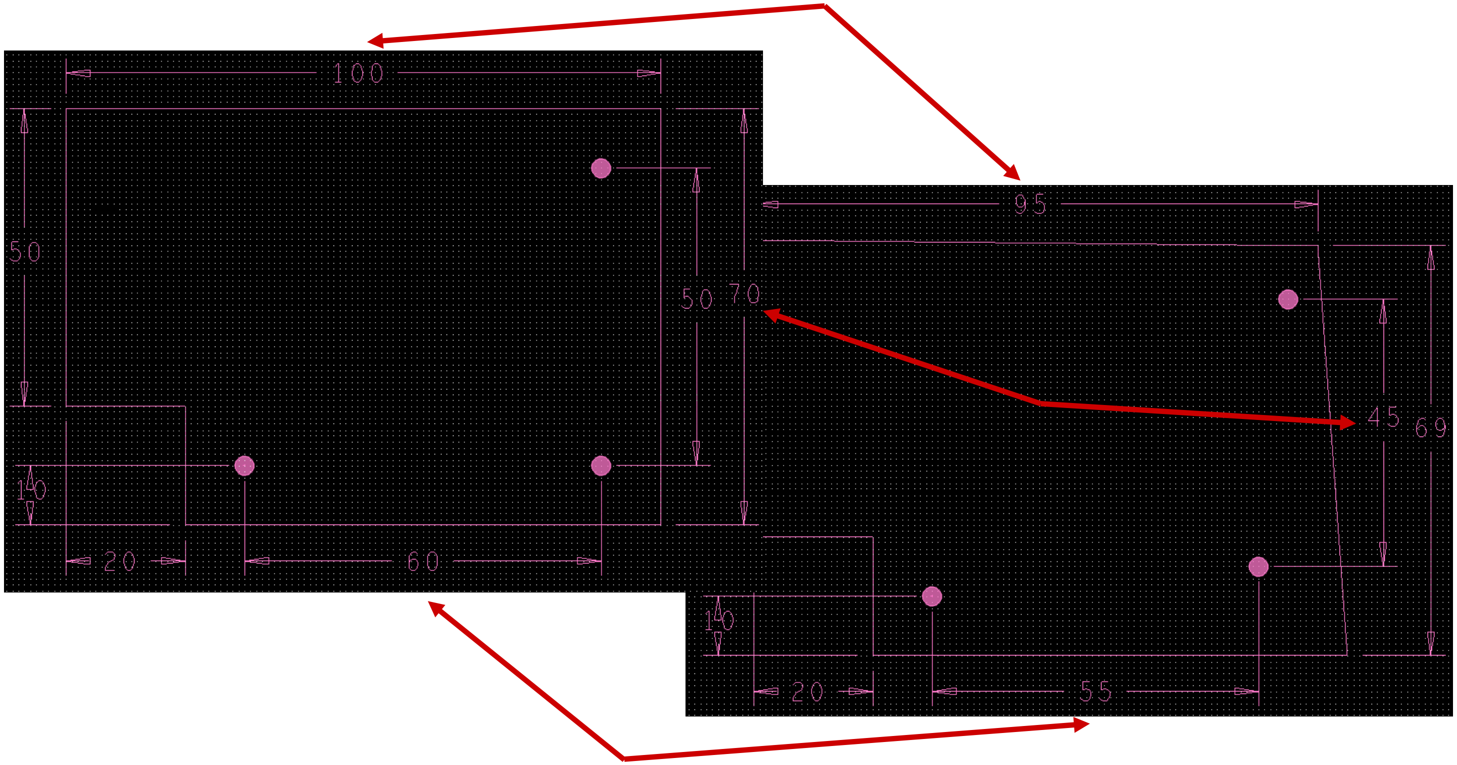
1. **RMB > Linear Dimension**
2. System is requesting to choose a location or an element for dimensioning.
3. Select top board edge (100) and place text.
4. Select right board edge (70) and place text.
5. Complete dimensioning like shown in the picture.
6. For a point to point dimensioning (drill hole bottom right -60) coordinates must be selected exactly (please note filter).
   You can also use the snap function.
7. For non orthogonal dimensions an additional click is required to define direction of dimensioning (horizontal or vertical).
   Bottom left corner with dimensions 10 and 20.





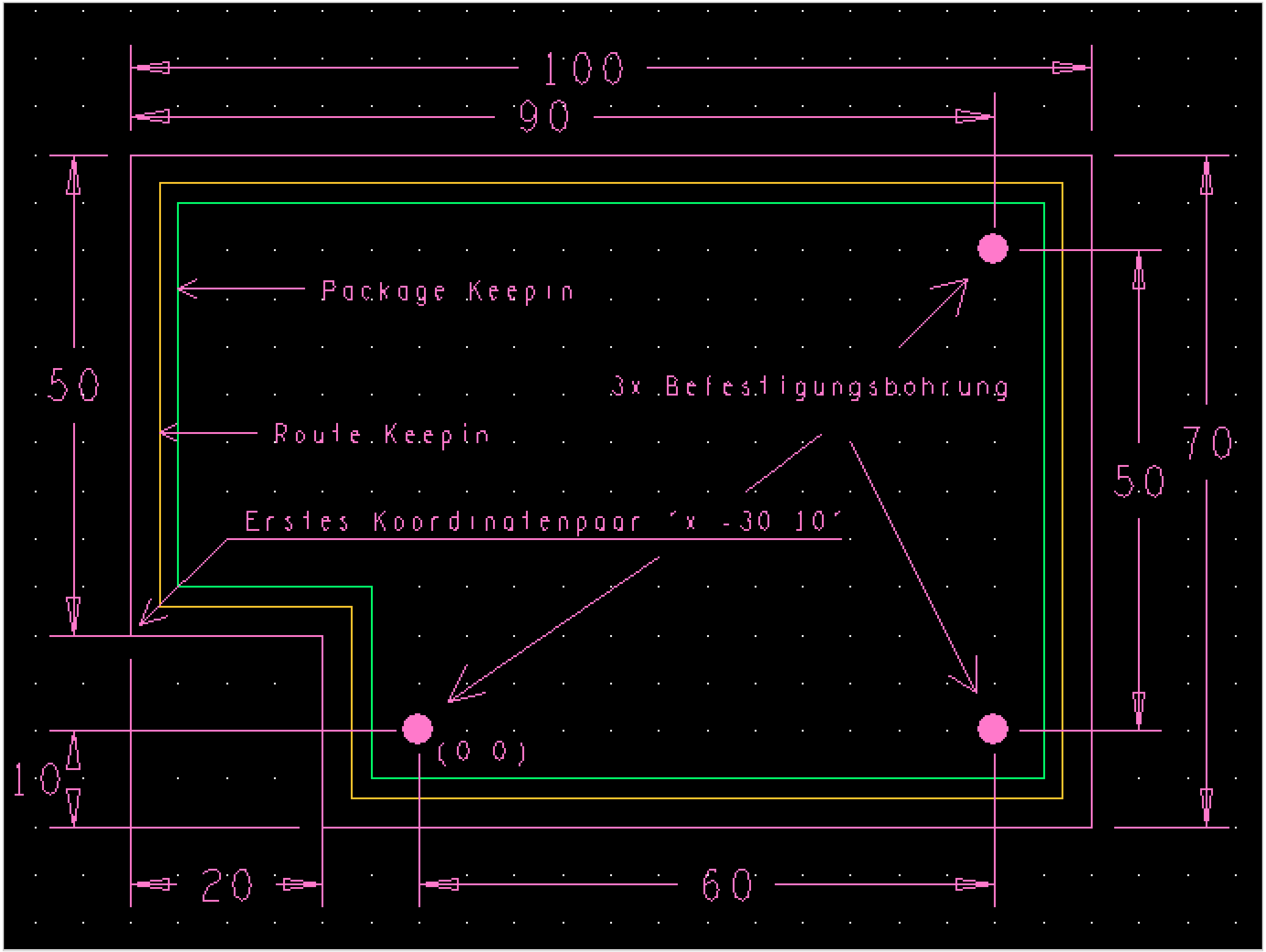
Lab: Dimensioning (IV)

8. To test dynamic behavior of dimensions please change position of bottom right mounting hole or top right corner of board outline.
9. Choose **Edit > Move** or icon  and move mounting hole.



FlowCAD

Completed Board Symbol

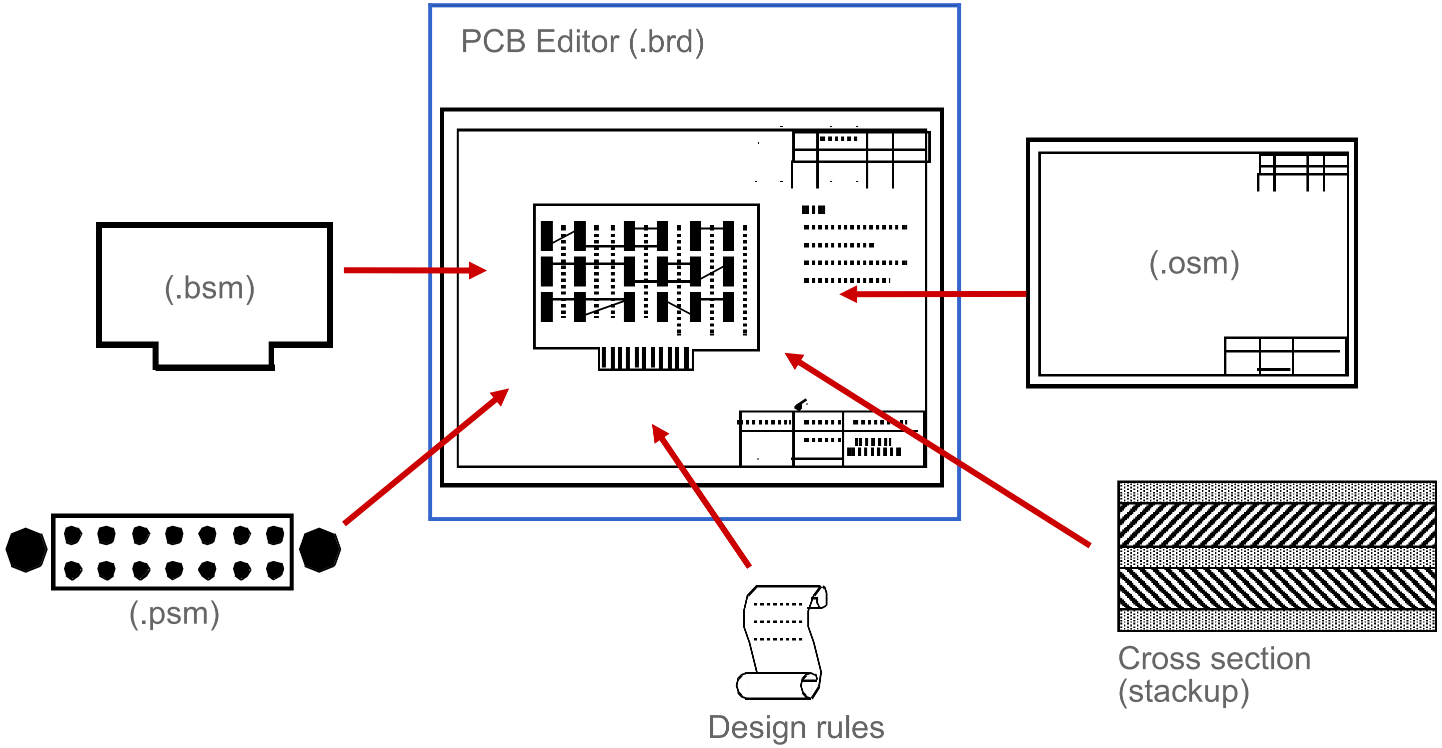


Master Board

A master board is a board template which contains settings which are mandatory for PCB design in addition to the board outline. These are:

Layer stack, design rules, preplaced components, etc.

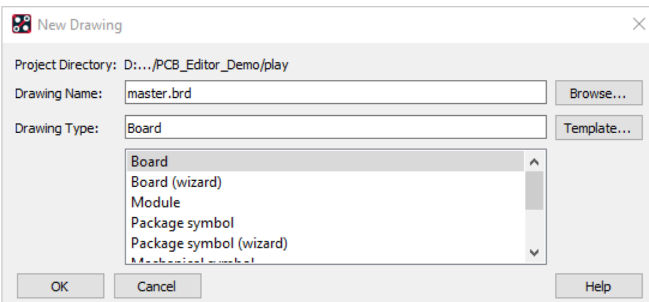
This method saves time and avoids errors, because parameters are already known good and will be reused.



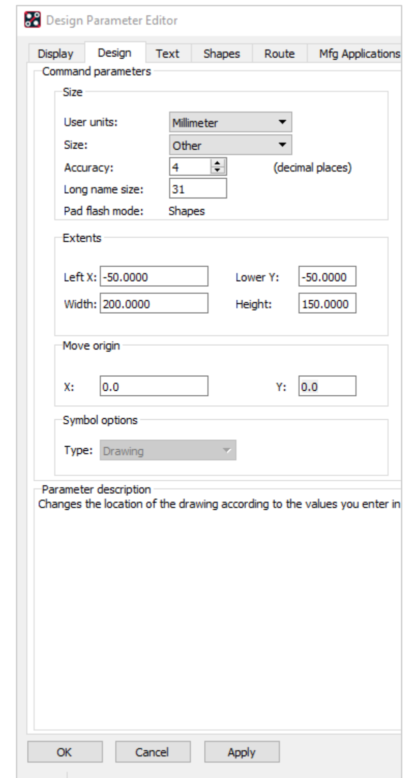
Lab: Master Board Setup

On the next pages we will describe most important steps on how to create a master board. These steps apply to any other board too.

1. **File > New** from main menu.
2. Enter **master** in Drawing Name field.
3. Select Drawing Type **Board.**
4. **OK.**



5. **Setup > Design Parameters… > Design**
6. Please change values like in drawing parameter box on right side.
7. **OK.**



Tip

Ensure that Drawing Extents are large enough to cover additional elements like drawing frames. Accuracy should be chosen high enough to ensure that shapes and fine traces have right resolution.

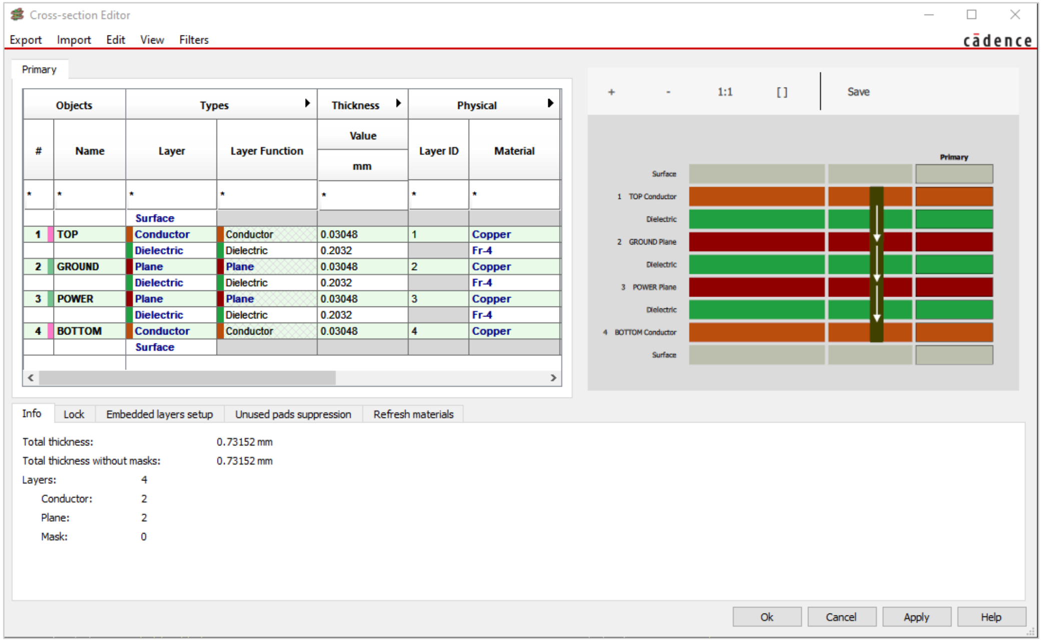
Lab: Master Board Layer Stack

The settings for the layer stack can be reached by **Setup > Subclasses > Etch** or 

This menu allows to add or remove electrical layers (routing layers).
RMB > **Add Layer / Remove Layer**.

Subclass Name of TOP and BOTTOM is default and cannot be changed. All additional layers can have any individual (unique) name. Chosen name appears also in Option Visibility window.

With **Type** it is possible to chose between Conductor (routing layer), Dielectric and Plane (power layer).



Tip

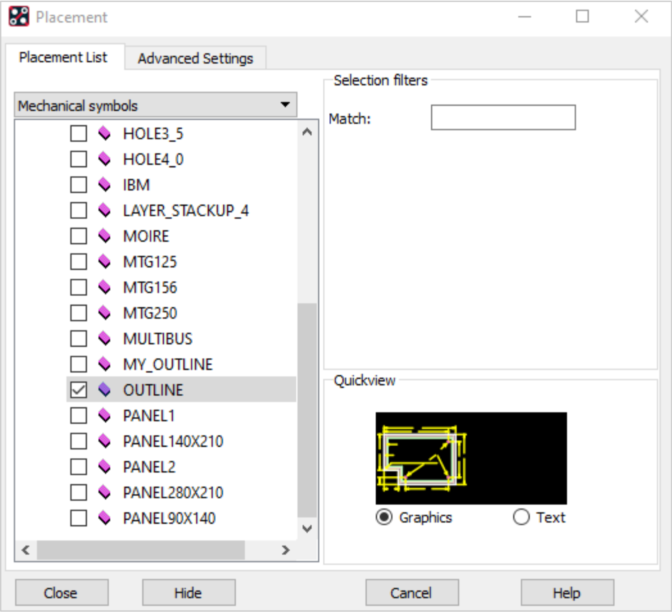
It is only possible to delete layers if they do not contain any data.

Lab: Master Board, Board Symbol

Like mentioned before, it makes sense to add a predefined board symbol (mechanical symbol) into a Master board for repeating designs. This makes design process efficient and reliable.

With the next steps, we load a board symbol into the open master board **master.brd**.

1. **Place > Manually** from main menu,
   a placement box (right side) appears.
2. Select **Database** and **Library in** the **Advanced Setting** tab**.**
3. Expand mechanical symbols in placement list and select **outline** (self defined symbol).
4. Enter **x 0 0** in command line and **Enter**.
5. **RMB > Done.** Mechanical symbol is placed.
6. **File > Save As.** A **master.brd** file will be saved.
7. Do **not** close PCB Editor!



Tip

At this point you can also preplace components (package symbols), format symbols and define other pre settings for grid, colors and design rules.
Design rules are dealt with from page 78 onwards.

Final Statements

As mentioned in the beginning, this tutorial is a quick start guide and not a training and should not replace one.

Quick start should give you an overview of functionality in the OrCAD flow and should enable you to make first independent steps. Main reason is to empower you to judge, if the OrCAD flow meets your needs.

Independent of this quick start we recommend a training to enable you to use full performance and highest efficiency for your daily tasks.

Trainings are scheduled and delivered by Cadence and FlowCAD on a regular base.
For details please visit Cadence and FlowCAD websites:

www.cadence.com

www.FlowCAD.com/en/training

Appendix

System Requirements (Full Version 22.1)

Operating Systems	Windows 11 Professional and Enterprise Windows 10 (64-bit) Professional and Enterprise, including Dark Theme mode; Windows Server 2016 (All Service Packs) Windows Server 2019
Hardware	Intel® Core™ i7 4.30 GHz or AMD Ryzen™ 7 4.30 GHz with at least 4 cores Note: Faster processors are preferred. 16 GB RAM 50 GB free disk space (SSD drive is recommended) 1920 x 1200 display resolution with true color (at least 32 bit color) A dedicated graphics card supporting OpenGL, minimum 2 GB (with additional support for DX11 for 3D Canvas) Dual monitors (for physical design) Broadband Internet connection for some service Ethernet port / card (for network communications and security HostID) Three-button Microsoft-compatible mouse

Contact us / Kontakt zu FlowCAD

Please do not hesitate to contact us.
Für weitere Fragen und Informationen stehen wir gerne zur Verfügung.

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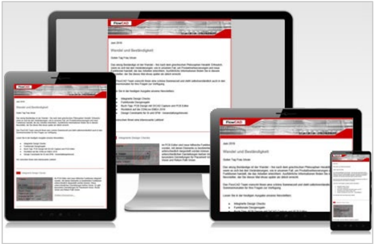

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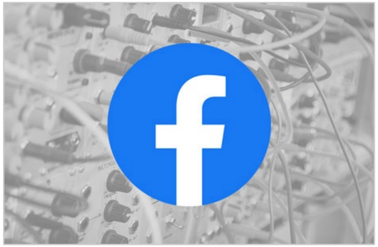

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