



Migration Guide

Migrating from CadSoft Eagle to OrCAD

Table of Contents

| | |
|--|----|
| Overview | 3 |
| Import Your Eagle Schematic Data to OrCAD Capture. | 4 |
| STEP 1 – Preparation | 4 |
| STEP 2 – Import the Eagle Schematic into OrCAD Capture. | 4 |
| Import Your Eagle PCB Data to OrCAD PCB Editor | 5 |
| STEP 1 – Preparation | 5 |
| STEP 2 – Import the Eagle PCB Design into OrCAD PCB Editor | 5 |
| STEP 3 – Backannotating Footprint Names from PCB Editor to OrCAD Capture | 8 |
| Synchronizing OrCAD Capture and PCB Editor Design. | 10 |
| STEP 1 – Creating a Netlist in OrCAD Capture | 10 |
| STEP 2 – Importing the Netlist in OrCAD PCB Editor. | 11 |
| STEP 3 – Check Design Status | 12 |
| STEP 4 – Check Physical and Spacing DRC Constraints | 12 |
| STEP 5 – Change to Preferred Colors | 12 |
| Importing Eagle PCB Libraries into OrCAD PCB Editor | 13 |
| STEP 1 – Preparation | 13 |
| STEP 2 – Import the Eagle PCB Footprint Library into OrCAD PCB Editor | 13 |

Overview

Choosing the right PCB design solution is never an easy task. No matter if you are a startup company looking for tools to develop your first or next innovative electronic-centric product or a large enterprise wanting a better solution to improve the productivity and efficiency of your design team and projects, selecting a PCB solution can be a daunting task. No one wants to get 75% of the way through a design to find out that the software you selected is not going to achieve what you need to accomplish.

There are many aspects you should consider when choosing your PCB Design solution, here are five that many users of Eagle discussed with Cadence:

- Does the capabilities of the offering and its technology meet your design requirements?
- What's the cost of the solution offering? Does it fit within your budget?
- What's the support service like? Will you be able to get quick responses to your questions and access online based tutorials, is there local help available?
- Can its technology and solution scale with your needs? As designs are getting more and more complex, will the capabilities of the tool adjust accordingly? Can it offer breadth and depth?
- How many other companies in your industry are using this tool and what is their feedback?

With OrCAD®, you can be confident that you will have the right solution and technologies at an affordable price to meet all of your design challenges today and tomorrow. Here are five of many reasons why:

- 30 years of innovation and leadership in the industry
- Affordable price and flexible purchase models
- Cutting-edge technologies
- Ecosystem empowered
- Industry's best customer support

Like many companies selecting OrCAD, you have existing or legacy designs you need to convert or translate into OrCAD. The good news is that OrCAD is supplied with an integrated and proven Eagle design translator built in. This guide will walk you through the steps and process involved in getting your design IP into the OrCAD format so you can start realizing the advantages of moving to OrCAD!

[Watch how Eagle Schematic and PCB data are migrated to OrCAD.](#)

[Watch how Eagle footprint libraries are migrated to OrCAD.](#)

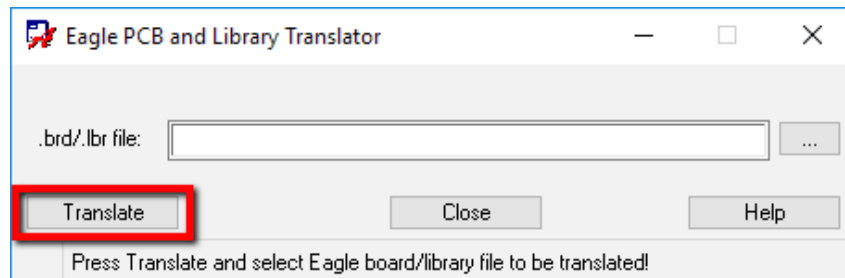
Import Your Eagle Schematic Data to OrCAD Capture

STEP 1 - Preparation

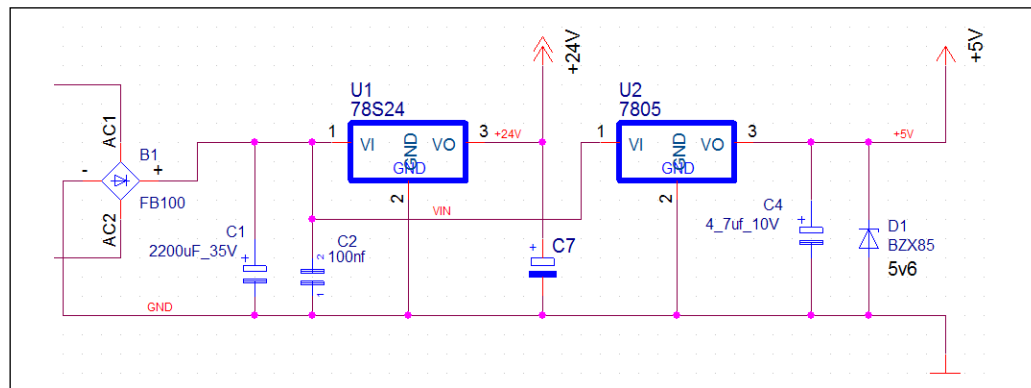
Before you start translating your Eagle schematic data into OrCAD Capture, the schematic must be in .xml format. If this is not the case, open the schematic in Eagle version 6.5 or later and save the schematic.

STEP 2 – Import the Eagle Schematic into OrCAD Capture

In OrCAD Capture, select “File » Import » Eagle Schematic Translator” to launch the Eagle to Capture translator. Browse to the schematic file to be translated (.sch). Then specify an output directory for the OrCAD project. Click on “Translate” button.



Leave the OrCAD output path blank if the output files should be located in the same directory as the source (.sch) file.



Once finished, open the project and check the schematic for any issues. Ideally, for catching problems, you should run the DRC tool (“Tools » Design Rules Check”) on the design.

Note: Make sure to check the log file shown after translation. It will show what happened during the Schematic translation.

```
(ELKO, Name=C5, Value=4.7uf_10V) (X=520, Y=520) X=530, Y=970
(CPOL, Name=C7, Value=N_A) (X=980, Y=980) X=990, Y=822 WARNING : Not on Grid

Replaced part name/Value
ELKO: Partvalue '4.7uf/10V' replaced by '4.7uf_10V'
R: Partvalue '0207/10' replaced by '0207_10'
R: Partvalue '0207/10' replaced by '0207_10'
R: Partvalue '0207/10' replaced by '0207_10'
R: Partvalue '0207/10' replaced by '0207_10'
ELKO: Partvalue '2200uF/35V' replaced by '2200uF_35V'
ELKO: Partvalue '4.7uf/35V' replaced by '4.7uf_35V'
ELKO: Partvalue '4.7uf/10V' replaced by '4.7uf_10V'
CPOL: Partvalue 'N/A' replaced by 'N_A'

Net alias replacements
'!OE5' replaced by '_OE5' - net alias position : Eagle coord : 1190, 810, Capture coord : 1210, 280
'!OE5' replaced by '_OE5' - net alias position : Eagle coord : 140, 810, Capture coord : 160, 280
```

The translation is done with connectivity in mind. This ensures a very high probability for design integrity and synchronization with the translated PCB design without any changes in connectivity, number of parts, etc.

Before creating a netlist for PCB synchronization, translate the Eagle PCB data to OrCAD PCB Editor. Do not close the project in OrCAD Capture!

Import Your Eagle PCB Data to OrCAD PCB Editor

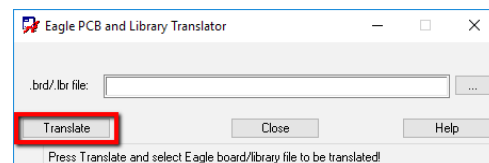
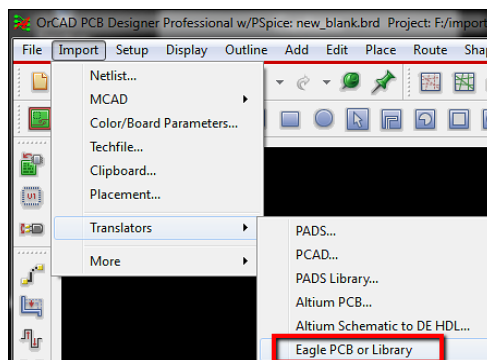
STEP 1 - Preparation

Before you start translating your Eagle PCB design data into OrCAD PCB Editor, the PCB design data must be in .xml format. If this is not the case, open the pcb in Eagle version 6.5 or later and save the board file (.brd).

STEP 2 – Import the Eagle PCB Design into OrCAD PCB Editor

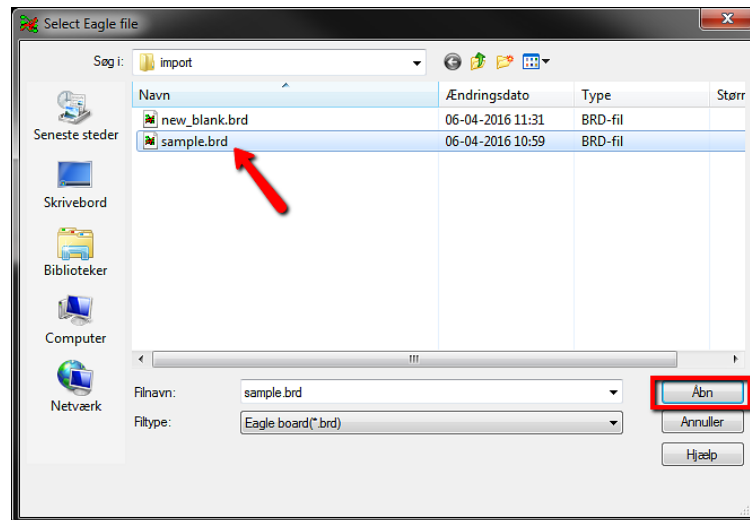
Start OrCAD PCB Editor.

Select “Import » Translators » Eagle PCB or Library”.



Click “Translate”.

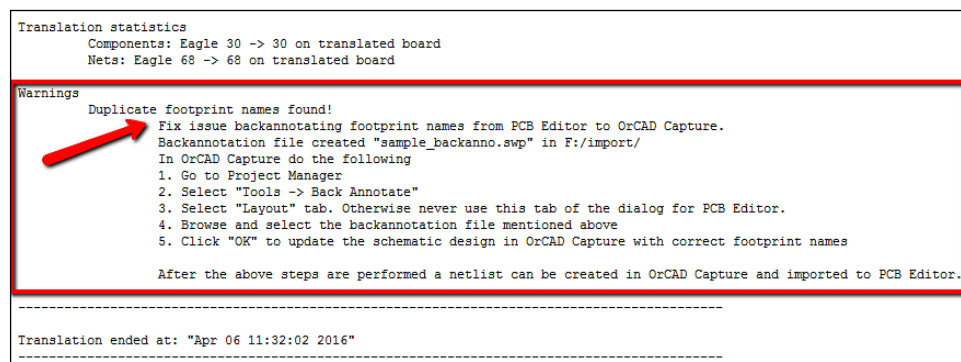
Browse to the Eagle PCB file and select “Open” and the translation starts.



The command window shows the translation progress.

Note: In some cases, especially for larger boards, it might seem like PCB Editor has stopped working. Do not close it as tests on large boards have shown translation times taking over five minutes, although this is unusual.

Note: Make sure to check the log file shown after translation. It will show what happened during the PCB translation. The most important part is at the bottom where statistics will compare the net and component count in the Eagle board with the data in the translated board.



The log can show two important warnings. Only one of them is present in this board.

"Nets with no pins found" (Not shown in this example.)

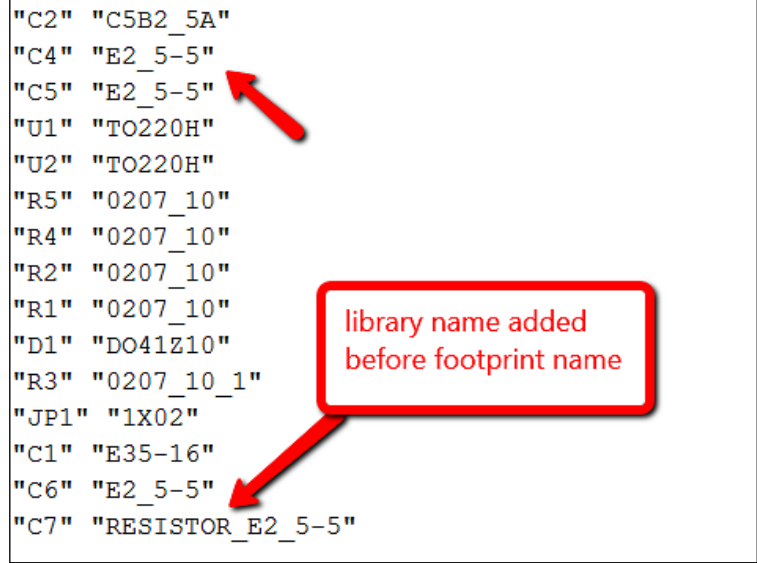
The statistics above this warning show the net count in both the original Eagle board and the translated PCB Editor board file.

If there is a mismatch, it is typically caused by "free" vias placed in Eagle. They are automatically assigned net names. This type of via will not have any net connection to the schematic and the net attachment is removed during netlist import. The same situation can occur if two or more free vias are placed and connected with a wire (cline) in Eagle but without being connected to a pin.

The translator will check if a net has any pin attachment and if not, warn that this is the case. The log file will show all the nets without any pin attachment and also report what the net count should be after netlist import.

"Duplicate footprint names found!"

This warning means that a backannotation process is needed to get the footprints' names aligned between the translated board and the translated schematic design. All steps involved are listed in the log and the necessary backannotation (.swp) file is generated for immediate use in OrCAD Capture. If duplicate footprint names are found, only the first instance will use the original footprint name, and the others will get the footprint library name added. In the example swap file for backannotation, C4 uses a "E2_5-5" footprint, as does C7 but from a library named RESISTOR, and the footprint is renamed to libraryname_footprintname.



```

"C2" "C5B2_5A"
"C4" "E2_5-5"
"C5" "E2_5-5"
"U1" "TO220H"
"U2" "TO220H"
"R5" "0207_10"
"R4" "0207_10"
"R2" "0207_10"
"R1" "0207_10"
"D1" "DO41Z10"
"R3" "0207_10_1"
"JP1" "1X02"
"C1" "E35-16"
"C6" "E2_5-5"
"C7" "RESISTOR_E2_5-5"

```

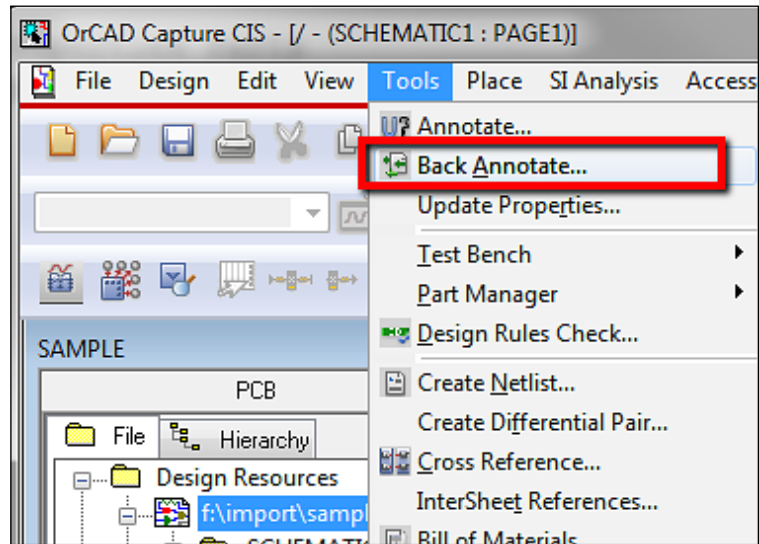
If there is no duplicate footprint warning in the log file, the back annotation process can be skipped. In that case, move ahead to "Synchronizing OrCAD Capture and PCB Editor Design".

STEP 3 – Backannotating Footprint Names from PCB Editor to OrCAD Capture

This step is only necessary if the bottom part of the log file after Eagle PCB to OrCAD PCB Editor states that there are "Duplicate footprint names found". If not, move ahead to "Synchronizing OrCAD Capture and PCB Editor Design"

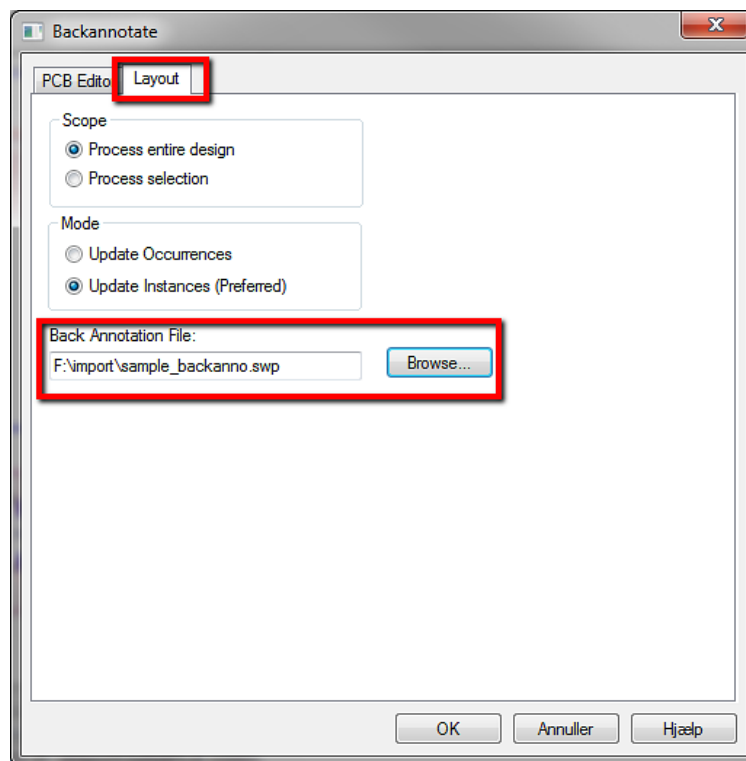
Go back to OrCAD Capture without closing OrCAD PCB Editor.

Select **"Tools » Back Annotate"** in OrCAD Capture.



Select the "Layout" tab. Select "Browse" and select the .swp file created by the Eagle PCB translator.

Note: This file is only created if necessary, so if there are no .swp file in the same directory as the translated board file, you can skip this part.



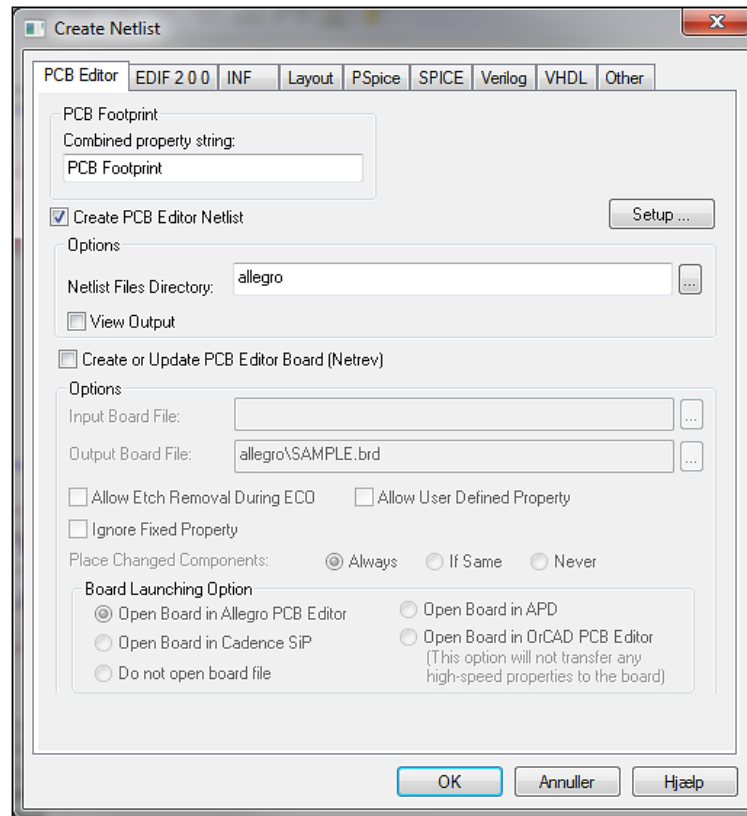
Click "Ok" to update the OrCAD Capture project with the footprint names in the board file. Check the Capture session log "Window » 1. Session Log" to see that all parts are updated.

Now the design is ready for synchronization.

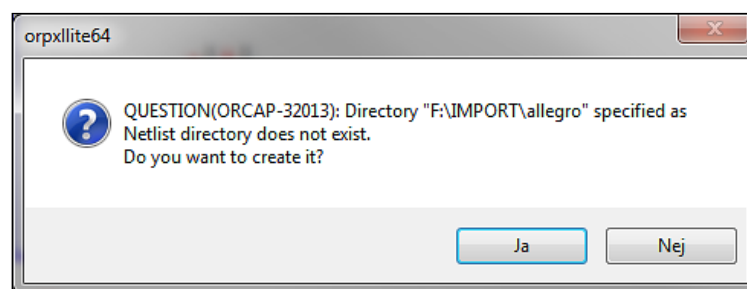
Synchronizing OrCAD Capture and PCB Editor Design

STEP 1 – Creating a Netlist in OrCAD Capture

Select “Tools » Create Netlist”.



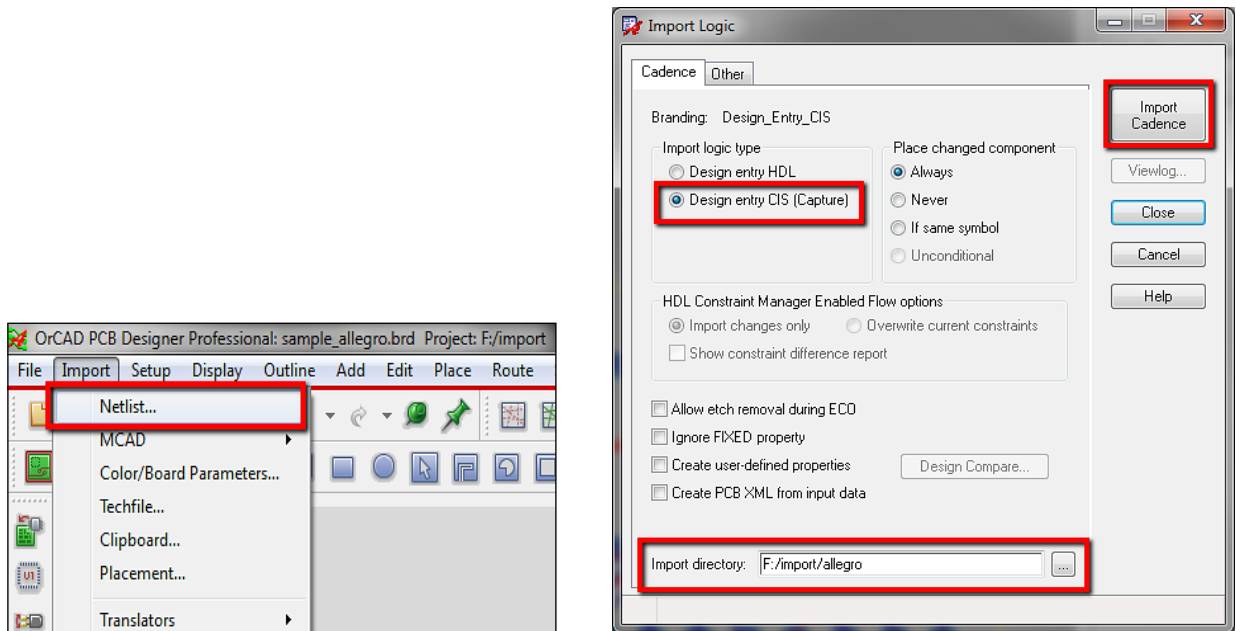
Click “Ok” to create the netlist and accept saving the project and creating an **allegro** subdirectory.



Note: The **allegro** subdirectory with the netlist is created in the directory where the OrCAD Capture design is located.

STEP 2 – Importing the Netlist in OrCAD PCB Editor

Select “Import » Netlist”.



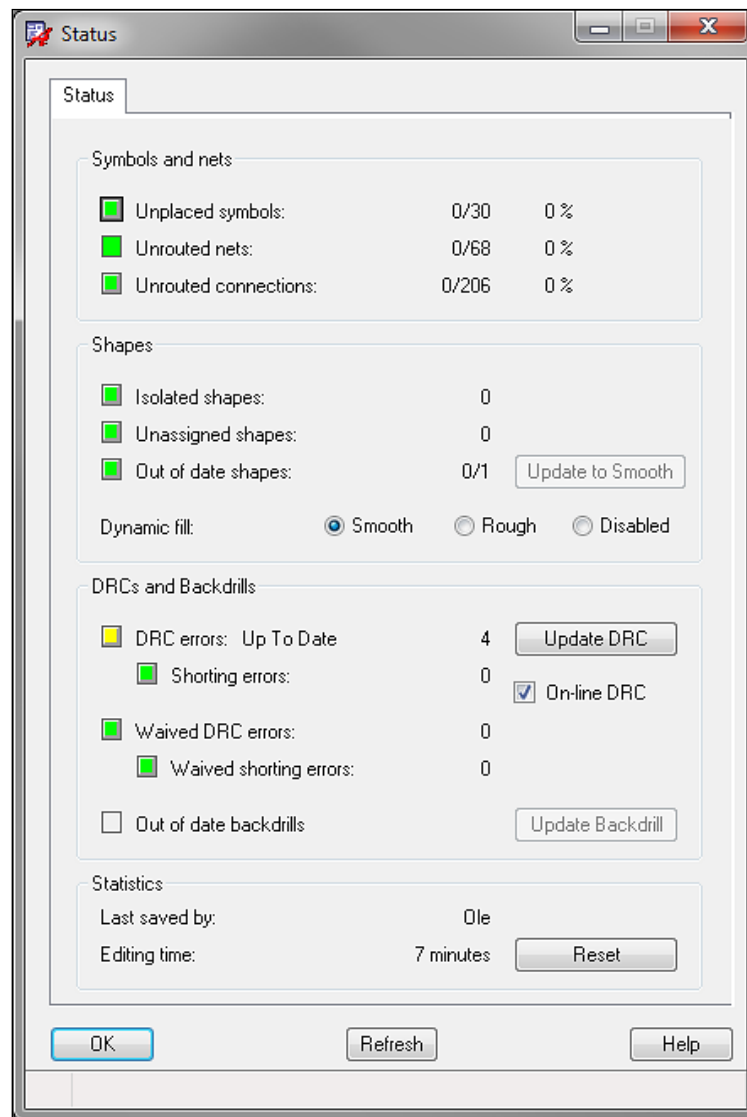
In the Import Logic window, make sure that the Import directory points to the **allegro** subdirectory with the netlist. This directory was created in the previous step.

Click “Import Cadence” to import the netlist.



This process should complete successfully.

STEP 3 – Check Design Status


Select “Check » Design Status” and, if necessary, click “Update to Smooth” to update the dynamic copper shapes.



STEP 4 – Check Physical and Spacing DRC Constraints

Start the Constraint Manager . Check and verify the physical and spacing DRC rules. Update the online DRC using the toolbar icon .

STEP 5 – Change to Preferred Colors

Changing the colors to suit your preferences is easy. Select the color and visibility toolbar icon  and change your color preferences accordingly.

Importing Eagle PCB Libraries into OrCAD PCB Editor

STEP 1 - Preparation

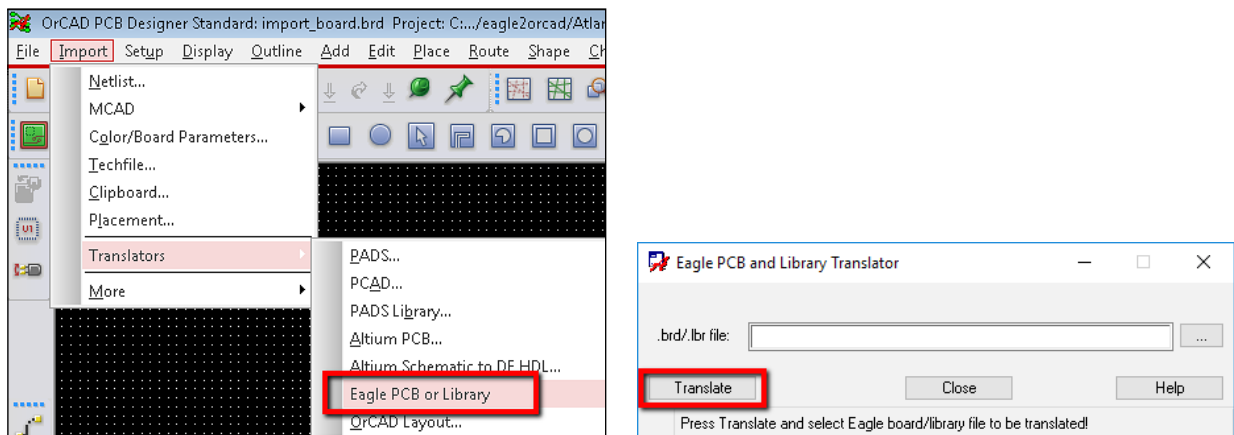
Before you start translating your Eagle PCB footprint library into OrCAD PCB Editor, the library data must be in .xml format. If this is not the case, open the library in Eagle version 6.5 or later and save it again (.lbr).

STEP 2 – Import the Eagle PCB Footprint Library into OrCAD PCB Editor

All the footprints in the library are imported to a board file. After the translation, they can be exported as individual footprints and padstacks.

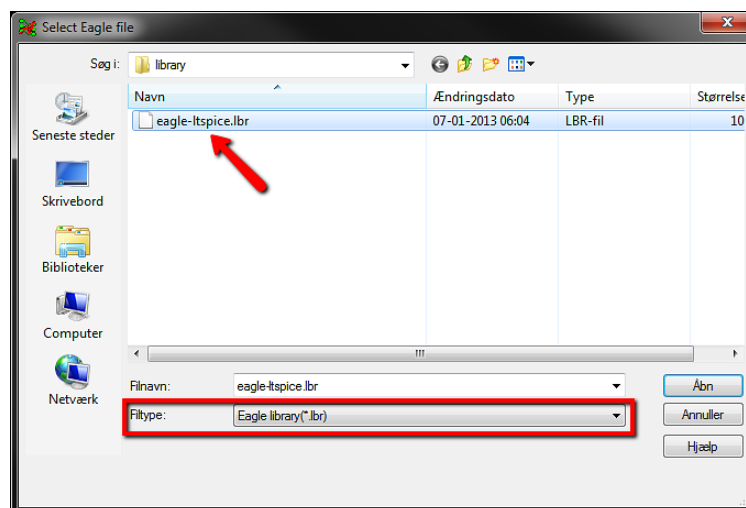
Start OrCAD PCB Editor.

Select “Import » Translators » Eagle PCB or Library”.



Click “Translate” and make sure to change the filetype to “Eagle library (*.lbr)”.

Browse to the Eagle library file (.lbr) and select “Open” and the translation starts.



The command window shows the translation progress.

Note: In some cases, especially for larger libraries, it might seem like PCB Editor has stopped working. Do not close PCB Editor but leave it running for a while.

Note: After the translation is finished, a log file will show what was done during translation.

```

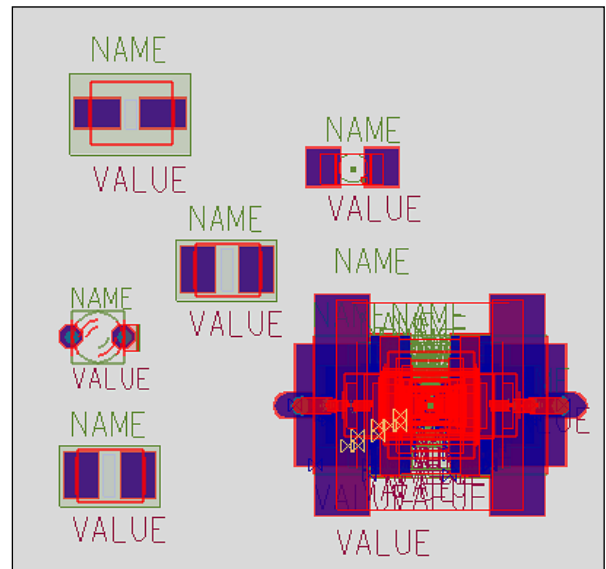
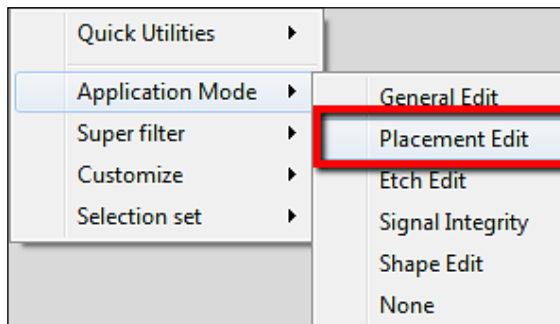
4 Creating footprint: R0805
4 Unknown object: "<b>RESISTOR</b><p>"
4 SMD: pin 1 at (-0.95 0.0) with pad r130_150m150p130
4 SMD: pin 2 at (0.95 0.0) with pad r130_150m150p130
4 Rectangle: Create ((0.4064 -0.6985) (1.0564 0.7015)) on PACKAGE GEOMETRY/ASSEMBLY_TOP
4 Rectangle: Create ((-1.0668 -0.6985) (-0.4168 0.7015)) on PACKAGE GEOMETRY/ASSEMBLY_TOP
4 Rectangle: Create ((-0.1999 -0.5001) (0.1999 0.5001)) on PACKAGE GEOMETRY/GLUE_TOP
4 Text: NAME created at (-0.635000 1.270000) on REF DES/SILKSCREEN_TOP
4 Text: VALUE created at (-0.635000 -2.540000) on COMPONENT VALUE/ASSEMBLY_TOP
4 Wire: created ((-0.41 0.635) -> (0.41 0.635)) with width 0.152400 on PACKAGE GEOMETRY/ASSEMBLY_TOP
4 Wire: created ((-0.41 -0.635) -> (0.41 -0.635)) with width 0.152400 on PACKAGE GEOMETRY/ASSEMBLY_TOP
4 Polygon shape: created on PACKAGE GEOMETRY/PLACE_BOUND_TOP
4 Create footprint as package symbol: R0805

```

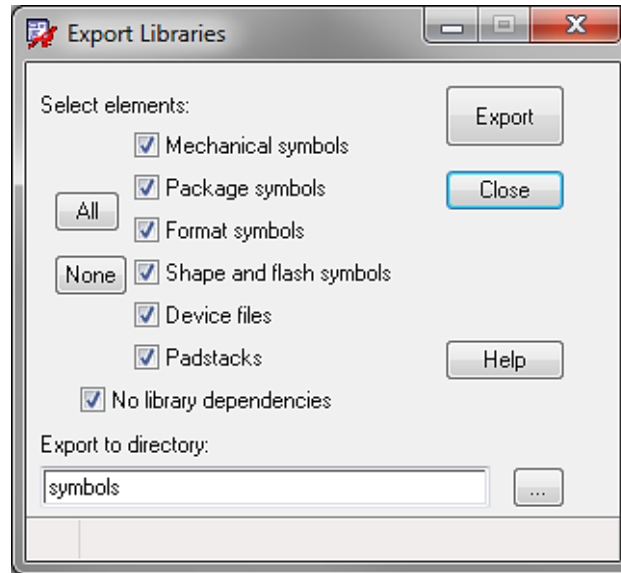
The "Unknown object" at the start of the file is a description text that is not translated for the footprint. The rest of the file lists the elements created for the footprint. The padstack names are translated so that they are ipc-like.

All the footprints are placed at the origin of the board and can be moved using standard PCB Editor place/move functions.

Right click and select "Placement Edit".

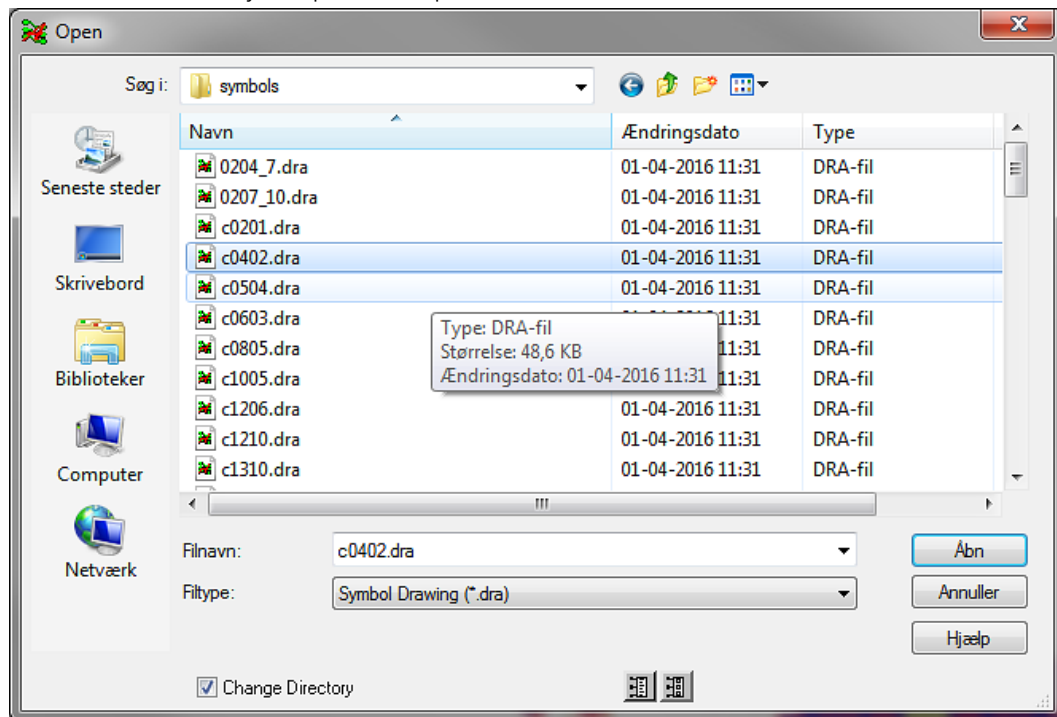


Use "Export » More » Libraries" to export to symbol and padstack files. It is a good idea to specify a subdirectory for the files created. The data are exported to a subdirectory named **symbols** in the same




directory as the translated library.

The OrCAD PCB Editor library footprints and padstacks are then created.



If you have any questions about the migration or in general about OrCAD, please do not hesitate to contact your local Cadence Channel Partner at <http://orcad.com/about/contact-us>.



© 2016 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc.. All other trademarks are the property of their respective owners.

The OrCAD product line is owned by Cadence Design Systems, Inc.