

Title: Start with electrical constraining

Product: Allegro PCB Editor with Performance Option or higher.

Summary: How to prepare a design for electrical constraining.

Author/Date: Beate Wilke / 03.12.2009

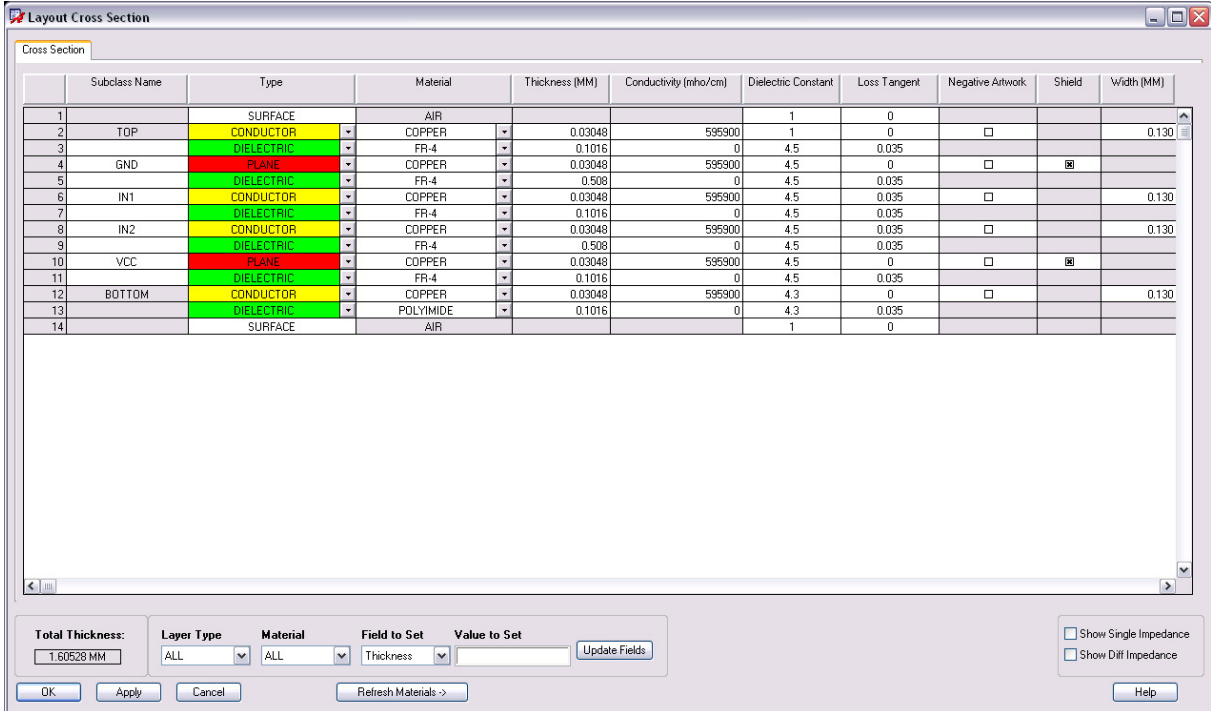
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1 Cross Section

The definition of Cross Section is the first step if you want to work with electrical rules. It includes very important basic information.

1.1 Basic Cross Section without impedance calculation:

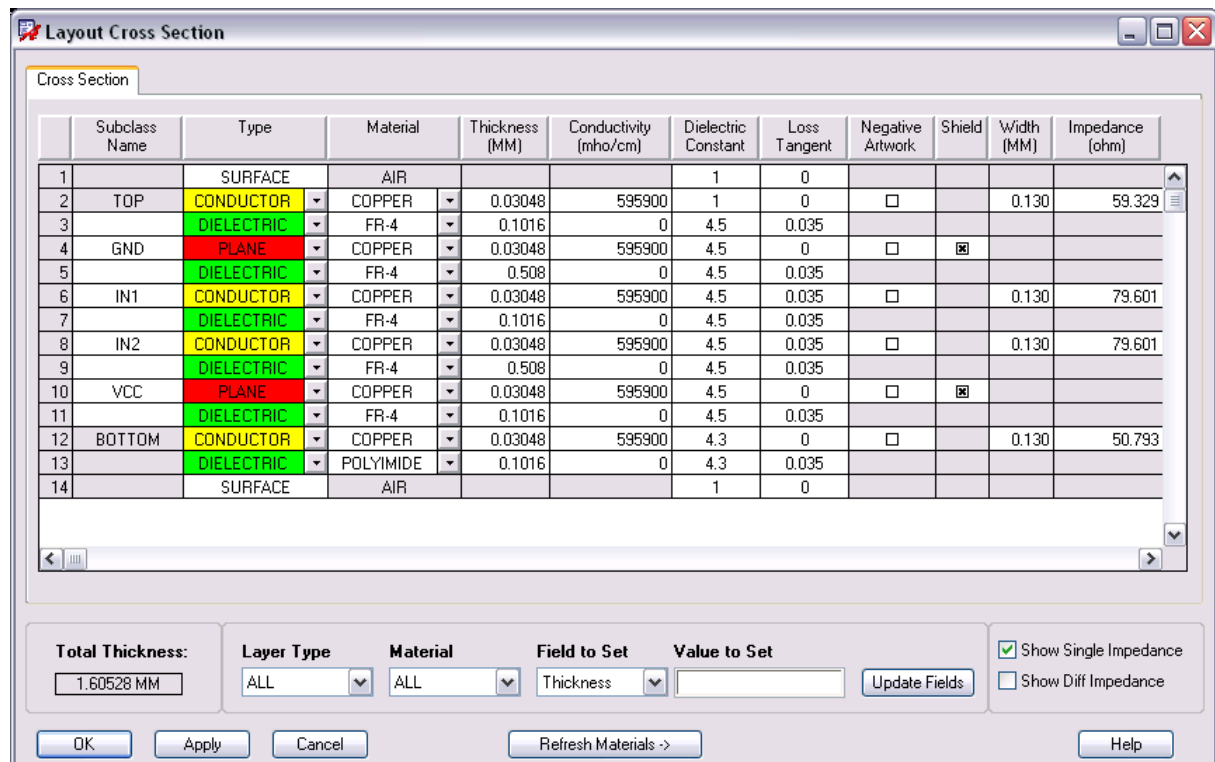


- Subclass Name - Name of the electrical layers.
- Type - The Type can be CONDUCTOR for signal layers, PLANE for plane layers or DIELECTRIC for non-electrical layers.
- Material - Material shows the different materials inside the board. All material information is stored in a file called material.dat. The default file is located in <cdsroot>share\pcb\text\materials. With Setup -> User Preferences -> Paths -> Config -> materialpath you can change this folder to user your own material.dat files.
- Thickness - Thickness of Material. Is also stored in material.dat but can be changed in the Cross Section.
- Conductivity (mho/cm) Conductivity is the specific value of the material.
 $E_CONDUCTIVITY > 100,000$ mhos/m = conductive (electrical)
 $E_CONDUCTIVITY < 100,000$ mhos/m = non-conductive (dielectric)
 Is also stored in material.dat but can be changed in the Cross Section.

Dielectric Constant -	Dielectric Constant in ϵ_r of the material. Is also stored in material.dat but can be changed in the Cross Section.
Loss Tangent -	Loss Tangent is the dielectric loss. The Impedance value changes when you modify the Loss Tangent value. Is also stored in material.dat but can be changed in the Cross Section.
Negative Artwork -	If you enable these boxes the plane layers are created as negative planes. We do not recommend using negative planes. It's easier to control positive planes than negative planes in case of plane islands and special plane spacing setting and thermal connections.
Shield -	Shield marks the reference layers as homogeneous planes for impedance calculation.
Width -	Width shows the min line width from the default rule set.

Note: We recommend modifying material.dat file and putting in your standard values. This increases the effort during work with Cross Section.

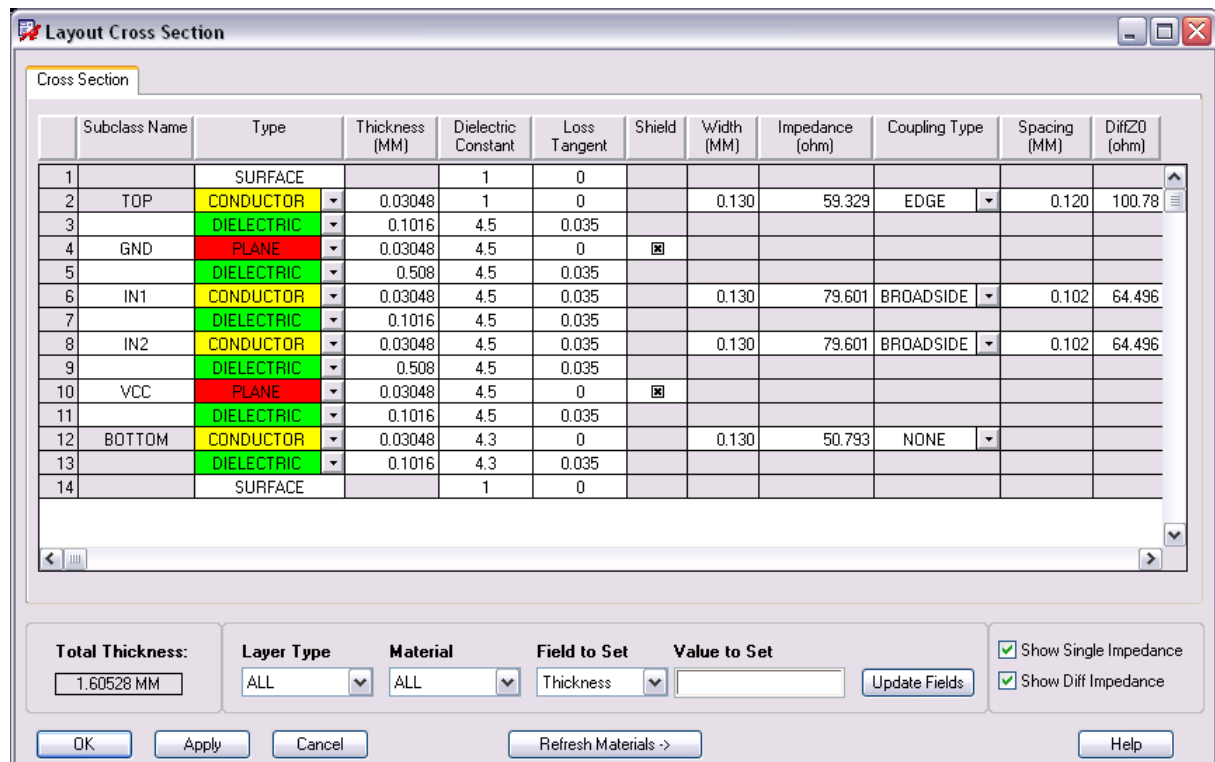
1.2 Cross Section with single impedance



When you enable “Show Single Impedance” on the right lower corner a new column appears on the right hand side. It shows the current single impedance. PCB Editor uses the values from the Cross Section to calculate the impedance. You can change the value for impedance to the needed value. The tool calculates the necessary width. You can change all values of the white boxes to calculate your impedance. Please recognize that the impedance on TOP and BOTTOM layer is different. We will talk about this later.

Note: This is only for calculation purpose. It creates no constraints.

1.3 Cross Section with differential impedance



When you enable “Show Diff Impedance” on the right lower corner 3 new columns appear on the right hand side.

Coupling Type - Possible options are NONE, EDGE and BROADSIDE.
 NONE – Default value.
 EDGE – Coupling between 2 clines on the same layer.
 BROADSIDE – Coupling between 2 clines on different layers separated by a dielectric layer.

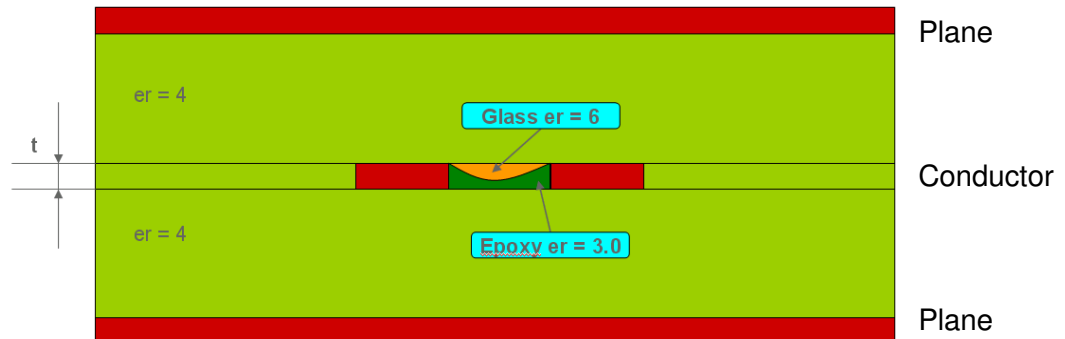
Spacing (MM) - Spacing between the 2 clines of a differential pair. The value can be used for EDGE and BROADSIDE coupling.

DiffZ0 (ohm) - Calculated differential impedance.

Like Single Impedance you can change the value for impedance to the needed value. The tool calculates the necessary width. You can change all values of the white boxes to calculate your impedance.

Note: If you want to change the material disable “Show Diff Impedance”.

1.4 Epsilon r on copper layers

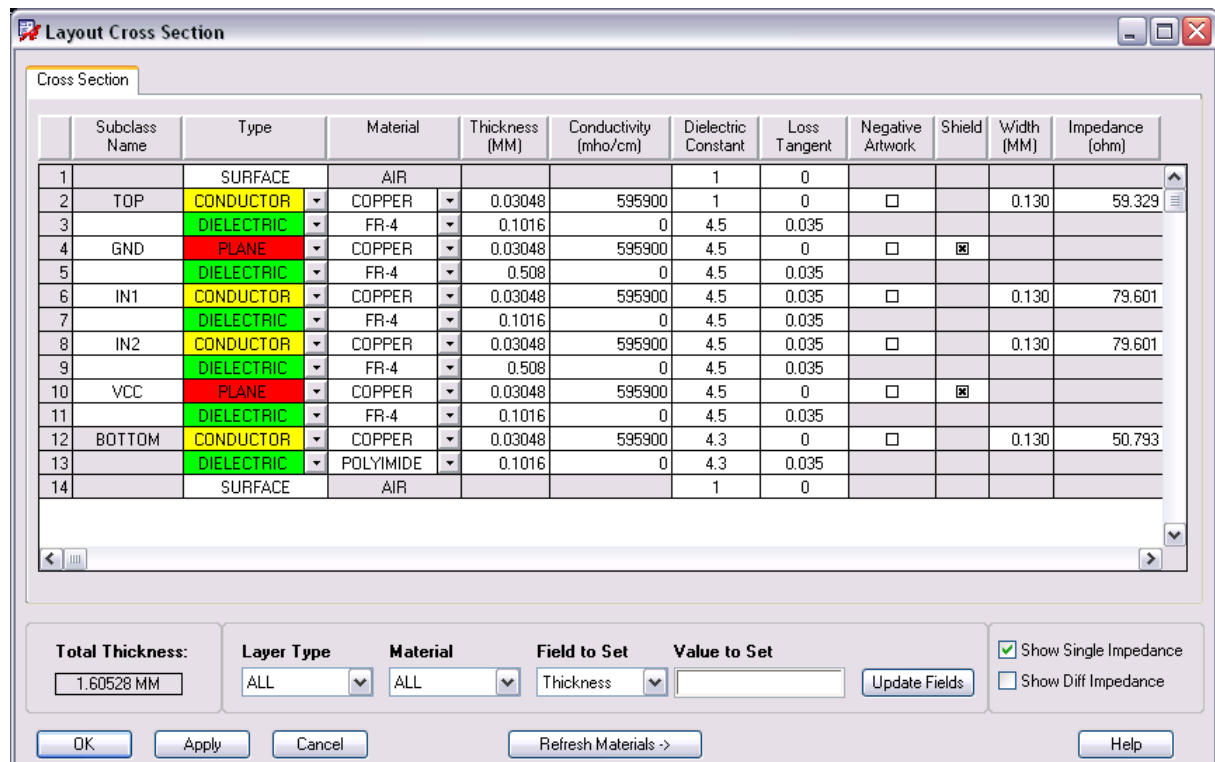


The value of Epsilon r on electrical layers is not for copper. It's for the dielectric between the clines.

Prepregs and cores are made out of glass and resin. Both materials have different Epsilon r. After laminating the board the distribution between the layers is homogeneous. The value for Epsilon r is 4 - 4.5. There are also glass and resin between the clines on the layers. If the spacing is large enough you also have a homogeneous distribution but when they are smaller you have more resin than glass in the spacings and the Epsilon r is different.

Normally you can use the same Epsilon r for electrical layers and dielectric. When the design is very critical, please talk to your PCB manufacturer to get the right values. They often have a good experience in creating the right values for impedance controlled designs.

1.5 The Solder Resist



On inner layer you can ignore the solder resist. It has no influence but on the outer layers. In our example the TOP layer has no solder resist, only the bottom layer has one. The results are different impedances on TOP (60ohm) and BOTTOM layer (51ohm).

You need to add the solder resist as extra layer. We recommend describing the solder resist in the material.dat file with all values. The tool automatically recalculates the impedance. The difference can be several ohms. Please remember (Chapter 1.4) to set the Dielectric Constant of the outer layer to the value of the solder resist.

The Propagation Velocity is different on outer and inner layer. The result is a different delay. If you route critical signals like clock on inner and outer layer you can get Jitter and Skew problems.

If your signals are very critical define the rules for Propagation Delay in time (ns) not in length (mm). The simulation tool considers the routing and calculates the final propagation delay.

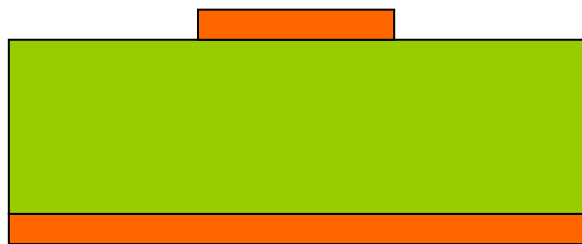
2 Topology

2.1 Microstrip Transmission Lines

Microstrip transmission lines are lines with one referencing plane layer. On outer layer you normally have microstrip lines.

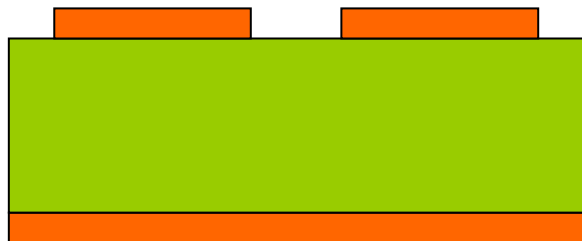
2.1.1 Surface

Surface lines are on an outer layer without resist.



2.1.2 Surface Differential

Surface differential lines are differential pairs on outer layer without resist.



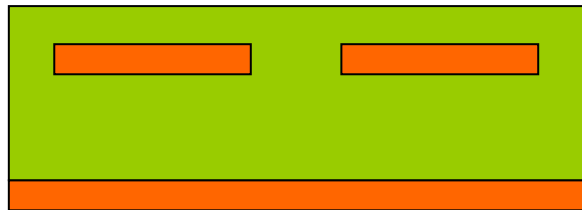
2.1.3 Embedded

Embedded lines can be on outer layers with resist or inner layers.



2.1.4 Embedded Differential

Embedded differential lines are differential pairs on outer layers with resist or inner layers.

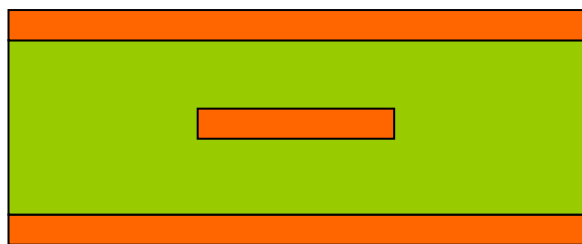


2.2 Stripline Transmission Lines

Stripline transmission lines are lines with two referencing plane layers. Stripline are possible only on inner layer.

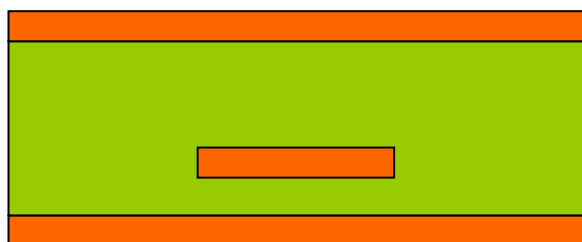
2.2.1 Balanced

Balanced striplines are in the middle of 2 plane layers



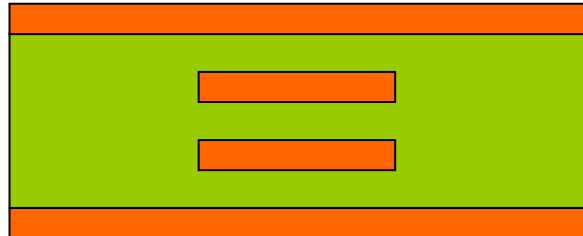
2.2.2 Unbalanced

Unbalanced striplines are out of the middle of 2 plane layers.



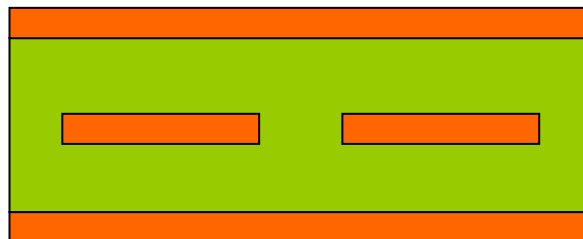
2.2.3 Broadside Coupled Differential Stripline

Broadside coupled differential striplines are differential pairs which are routed on 2 different layers.



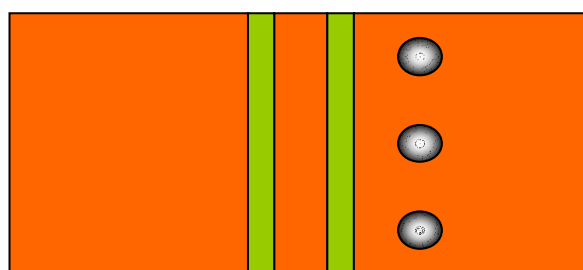
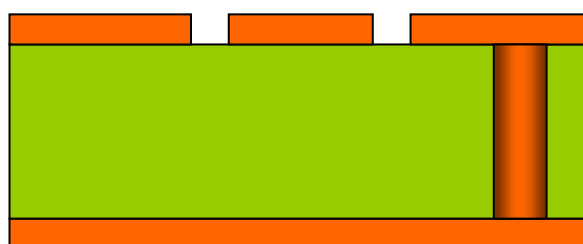
2.2.4 Edge Coupled Differential Stripline

Edge coupled differential striplines are differential pairs which are routed on 1 layers.



2.3 Coplanar transmission line

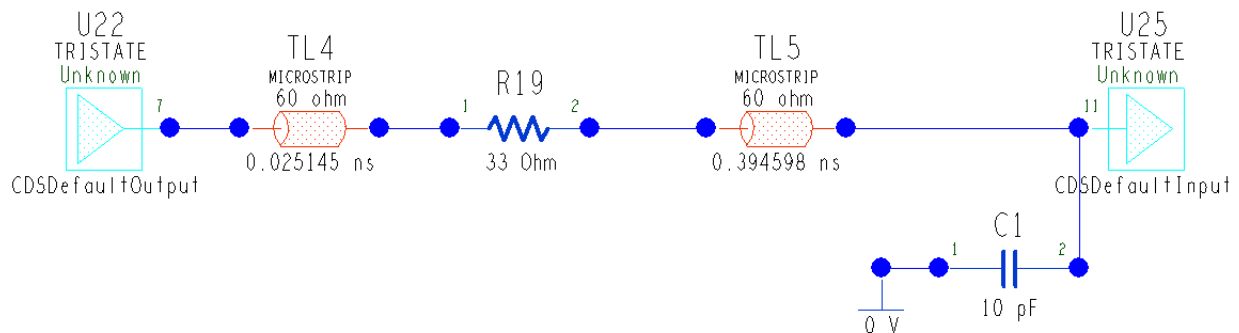
Coplanar lines are shielded by copper planes on the same layer. The edge of the planes is often stitched with via to a referencing plane layer.



Top view

3 Definition of DC-Nets

DC nets are necessary for correct simulator results. DC nets are also used as end points for Xnet definitions.



You will find signal names like GND, GND_A, P3V3 in your designs. We all know that these are DC nets but the simulator can't transfer a signal name into voltage information. The simulator needs an additional Voltage property which includes the real voltage value.

DC-Nets have a second, important function during extraction. All signals which are connected by a discrete, serial component (R, L and C) are put together to become an Xnet. Is there any DC net (pull up or pull down resistor) the tool identifies it as an end point for extraction.

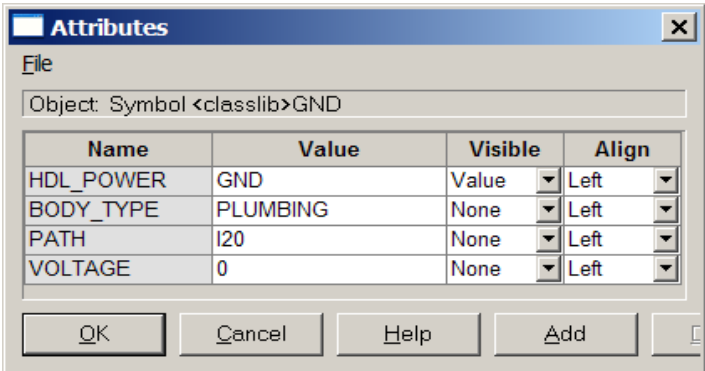
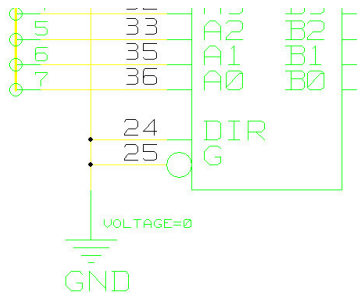
You don't need to identify all DC nets. Only the nets which are connected to pull up or pull down elements have to be defined. Power nets in analog areas can be ignored.

3.1 Defining a VOLTAGE-Property

Three ways to define it.

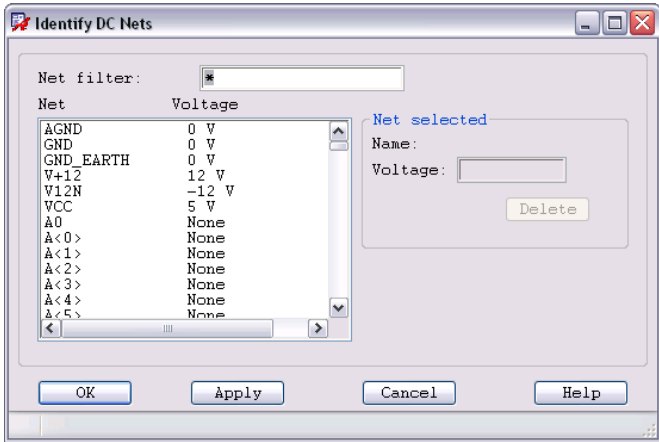
1. Design Entry HDL:

Define the Voltage property at the power and ground symbols.

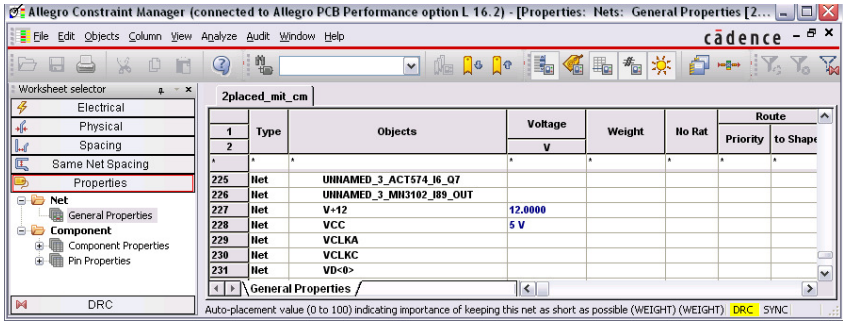


2. PCB Editor or PCB SI:

Logic->Identify DC Nets or Edit>Properties



3. Constraint Manager Property Workbook.



4 Component Classes

The component classes are very important.

Only components with the property CLASS = DISCRETE can be used to add physical nets to an Xnet.

Only components with the property CLASS = IC can act as driver and receiver.

CLASS and the pin property PINUSE have a central function during mapping of Templates

4.1 CLASS- und PINUSE-Property

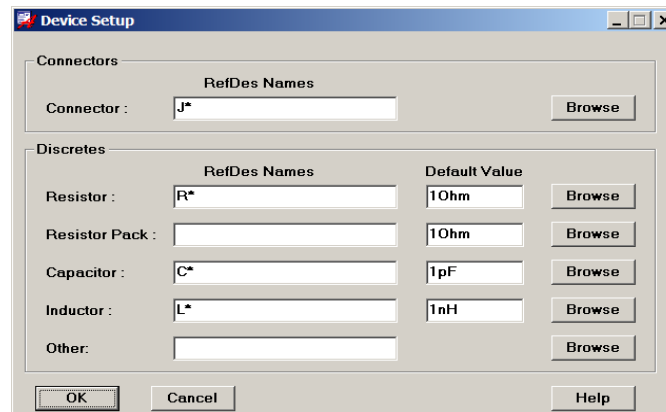
CLASS	Devices	Refdes	PINUSE
IC	Active digital components	IC*	IN, OUT, BIDIR, OCA, OCL,.....
DISCRETE	Passive	R*, L*, C*	UNSPEC
IO	Connectors	X*	UNSPEC

For R, L and C – Always CLASS = DISCRETE and PINUSE = UNSPEC

For IC – CLASS = IC. You can define the different PINUSE information in the library. If you connect an IBIS model to the component the pin descriptions from the model overwrites the pin descriptions from the library.

4.2 CLASS and PINUSE - Changes

The best method to change CLASS and PINUSE definitions in the board is Tools -> Setup Advisor -> Device Setup



This function changes CLASS and PINUSE to the right settings. In the box Connector fill in the RefDes prefix for your connectors. It changes CLASS to IO and PINUSE to UNSPEC. In the box Discretes fill in the RefDes prefixes for your discrete components. It changes CLASS to DISCRETE and PINUSE to UNSPEC.

Default Value is only for discrete components which have no Value property.

We recommend:

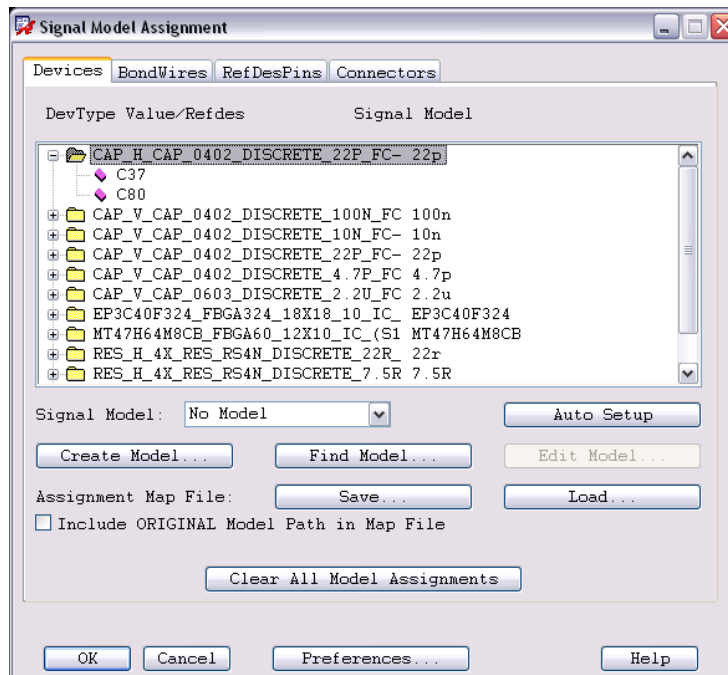
Always define the CLASS property in the library.

Always define the PINUSE for discrete components in the library.

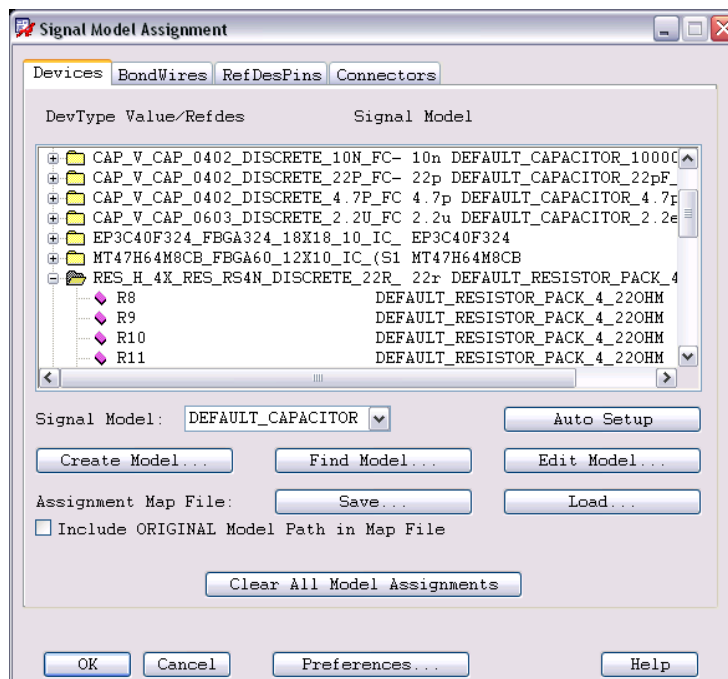
Otherwise it could be that during import of a new net list the library information overwrites the CLASS and PINUSE definition.

5 Signal Model Assignment

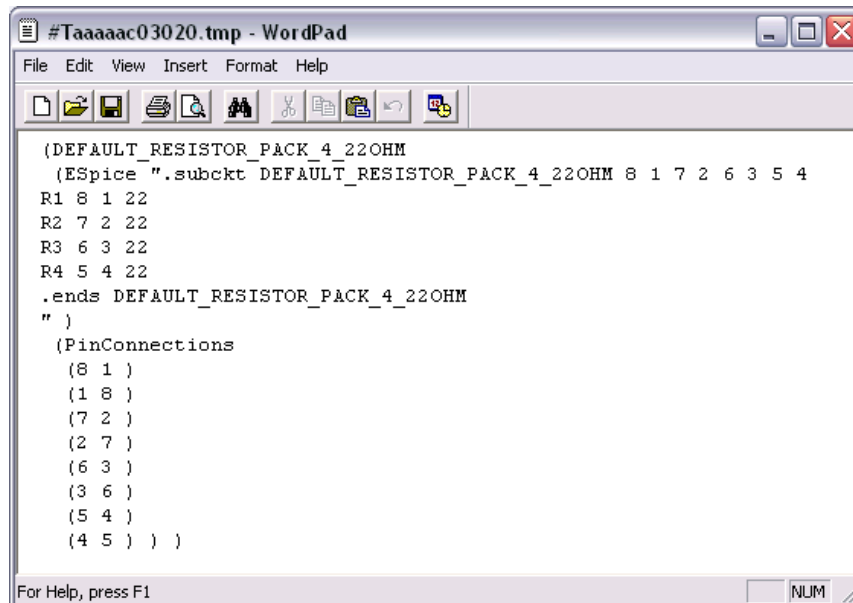
Allegro needs a Signal Model to create Xnet and differential Pair automatically. In PCB Editor go to Analyze -> SI/EMI Sim -> Model, the Signal Model Assignment window opens. You get a list of all components. Use Auto Setup to create the models.



Auto Setup creates an ESpice-Model for all components with Property CLASS=DISCRETE which don't have a Signal Model assigned. Only components with property Value=0 are ignored. It reads the value of property Value and put it into the ESpice Model.



It's important that you check the pin mapping of all array component models. Select the Signal Model of an array component and click on Edit Model. It opens the model description as ASCII file. If the mapping is wrong, correct and save it.



```
#Taaaaac03020.tmp - WordPad
File Edit View Insert Format Help
(DEFAULT_RESISTOR_PACK 4 22OHM
 (ESpice ".subckt DEFAULT_RESISTOR_PACK_4_22OHM 8 1 7 2 6 3 5 4
 R1 8 1 22
 R2 7 2 22
 R3 6 3 22
 R4 5 4 22
 .ends DEFAULT_RESISTOR_PACK_4_22OHM
 " )
 {PinConnections
 (8 1 )
 (1 8 )
 (7 2 )
 (2 7 )
 (6 3 )
 (3 6 )
 (5 4 )
 (4 5 ) ) )
For Help, press F1 NUM
```

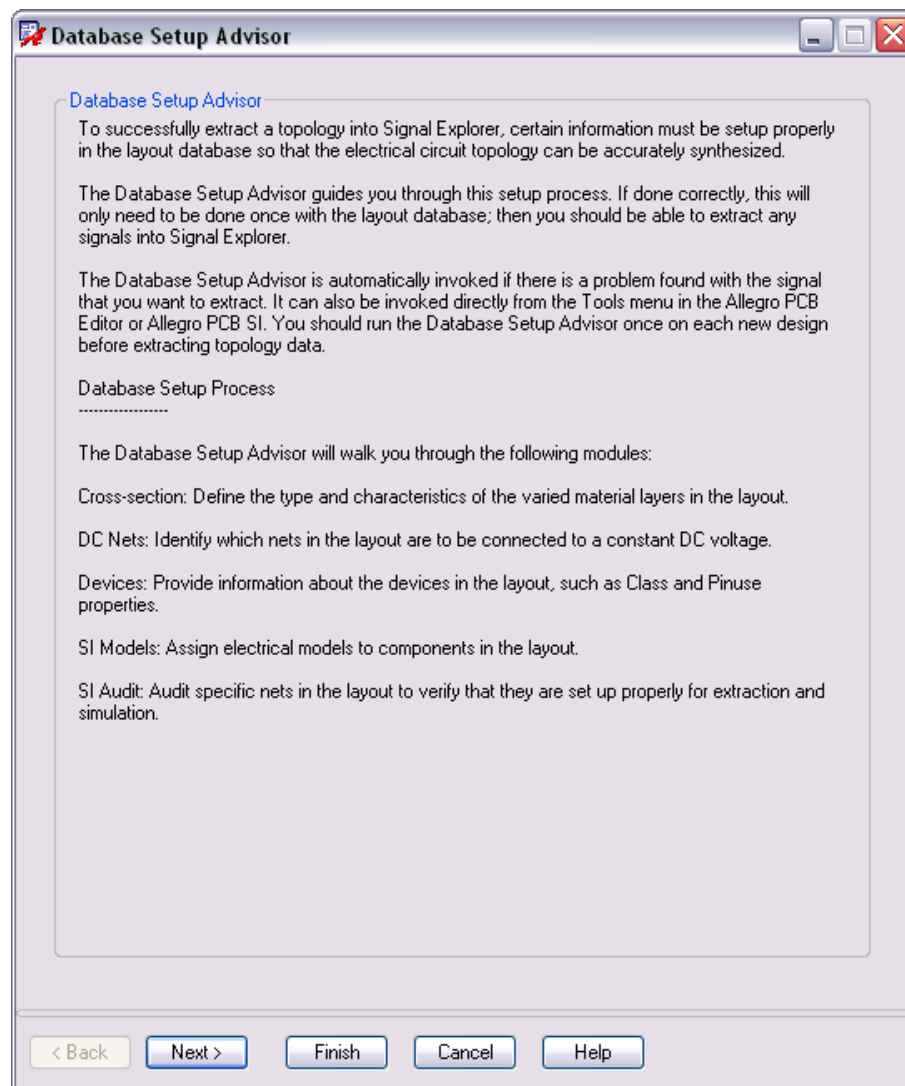
All models are stored in a library file called devices.dml. Go to Analyze -> SI/EMI Sim -> Library. This opens the Signal Analysis Library Browser.



The library interconnect.iml is a cache-library. Allegro use it to raise the performance during extraction or simulation. You can delete this library. The PCB Editor automatically creates a new one. Another cache Library is sigxp.dml. It contains all simulation models of the nets.

6 Setup Advisor

The menu Tools -> Setup Advisor gives you a good guideline through all necessary steps. All we talked about in chapter 1, 3 and 4 can be made during work through Setup Advisor.



7 Technology Files

You can import or export Technology Files from PCB Editor or Constraint manager.
User File → Import/ Export → Technology File

A Technology File includes:

- Drawing parameters (includes units and design extents)
- Layout cross section
- DRC modes
- Spacing, physical, electrical, and design constraints
- User property definitions

See [%CDSROOT%/doc/algrolibdev/algrolibdev.pdf](#) for more Information