Title: Routing with different line width

Product: Allegro PCB Editor

Summary: Using Net Schedule and Same Net Spacing make it possible to define different line width for the single parts of a net

Version 16.6

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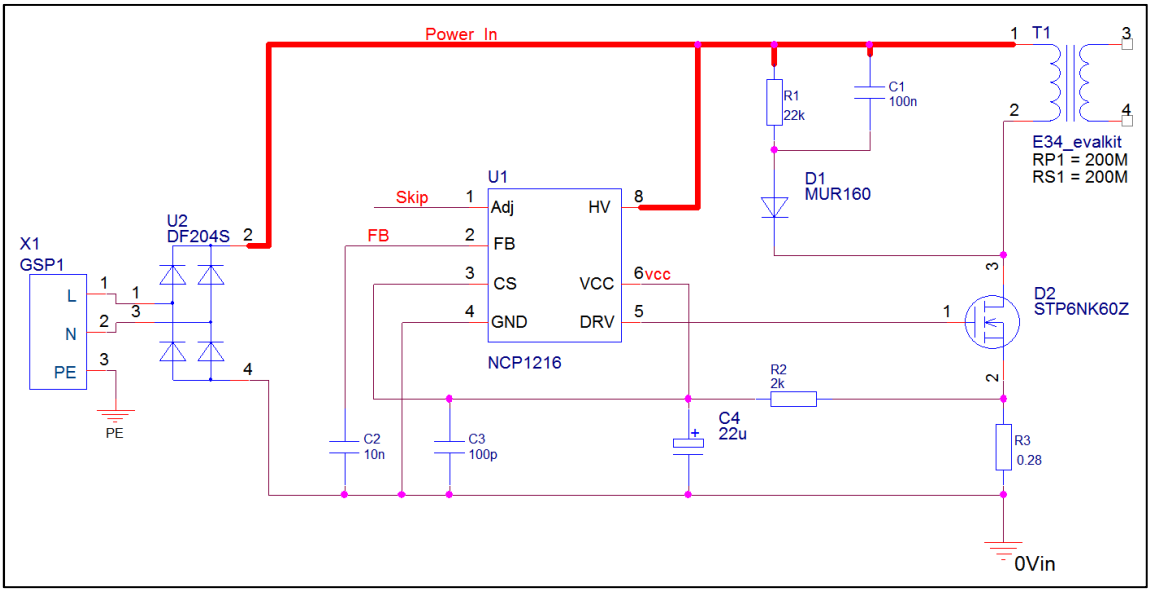
## Table of Contents

1 Example ..... 2
2 Necessary rules ..... 3
2.1 Physical rules ..... 3
2.2 Net Schedule ..... 4
2.3 Add physical rules ..... 5
2.4 Same Net Spacing ..... 6
3 Attached examples ..... 8
4 Solution for OrCAD ..... 9
4.1 Using Neck Mode ..... 9
4.2 Using funckey ..... 9

# 1 Example

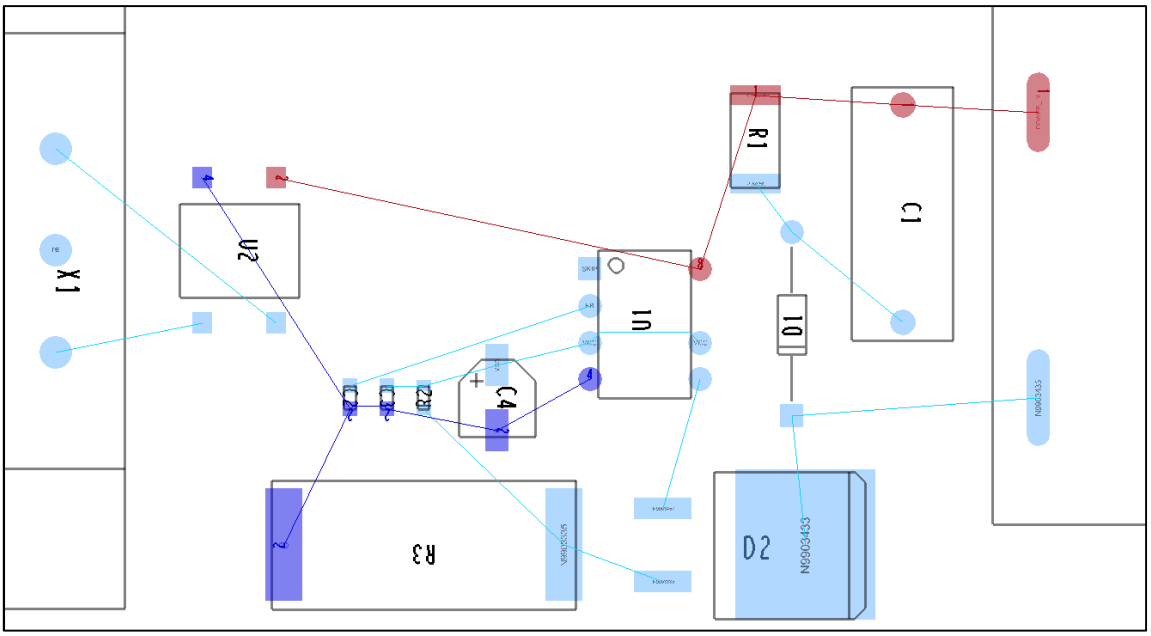
We use the primary side of a switching power supply as example. The design has some nets which should be routed with different line width. A good example for this Application Note is the net Power_IN. It's marked in red.



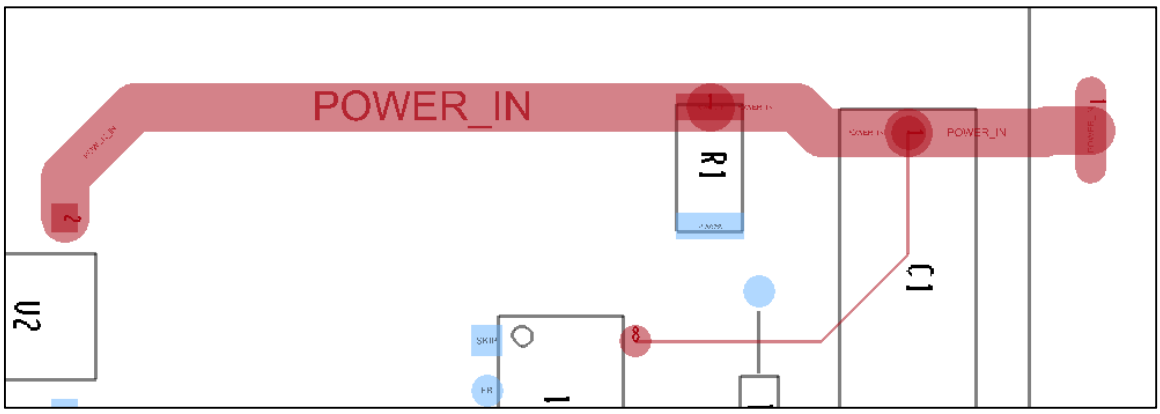

This net has a currency of 3A from U2 to T1 and need to be routed with 2.5mm width. The sense line to U1 needs 0.2mm only and should be connected at C1.

You can do this manually but PCB Editor gives you functionality to define these rules in Constraint Manager (short CM) to get perfect support during routing of this design.

This is the placement in PCB Editor. It's no real placement but it makes it easier to understand what to do.



The net Power_In is marked in red. You see that all unrouted connections are shown as short as possible. But that is not the way we want to route this net. We like to have this:




# 2 Necessary rules

We have to do these things:

- Define Physical rules for 2.5mm and 0.2mm
- Define Net Schedule to make sure that U1 is always connected to C1.
- Add physical rules to the different parts of net Power_IN
- Define Same Net Spacing rules to make sure that sense and main cline are really divided

## 2.1 Physical rules

Open CM and define these two rules.

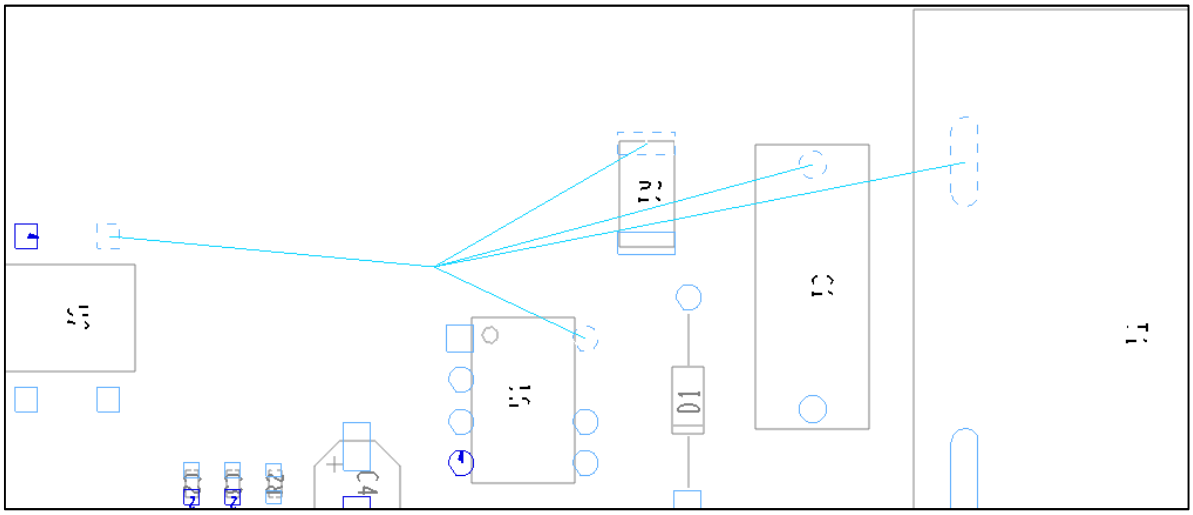
| Objects | | | Line Width | |
|---|---|---|---|---|
| | | | Min | Max |
| Type | S | Name | mm | mm |
| * | | * | * | * |
| Dsn | | ⊟ AN | 0.2000 | 0.0000 |
| PCS | | ⊞ DEFAULT | 0.2000 | 0.0000 |
| PCS | | ⊞ 2.5MM | 2.5000 | 0.0000 |

If 0.2mm is also your minimum rule for the whole design you can use Default rule. Otherwise define a separate rule with 0.2mm for Min Line Width.

## 2.2 Net Schedule

Select Display > Blank Rats > All to hide all rats and then select Display > Show Rats > Net and select a pin which is connected to Power_In. To help you, the pins are also marked in red.

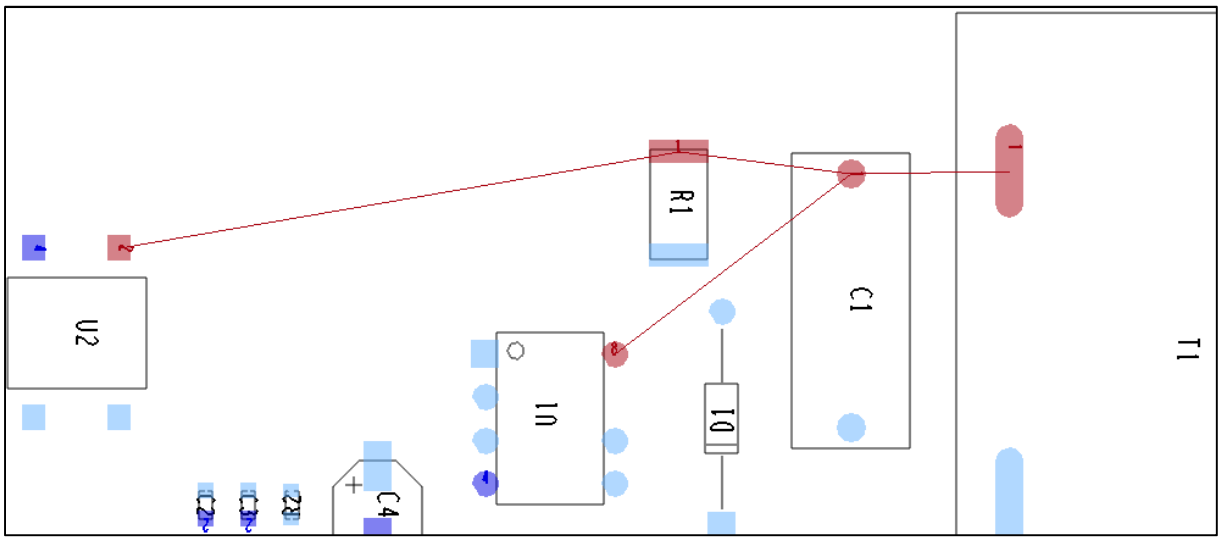
Select Logic > Net Schedule and select net Power_In. You will get this view.




Now select the red pins of:

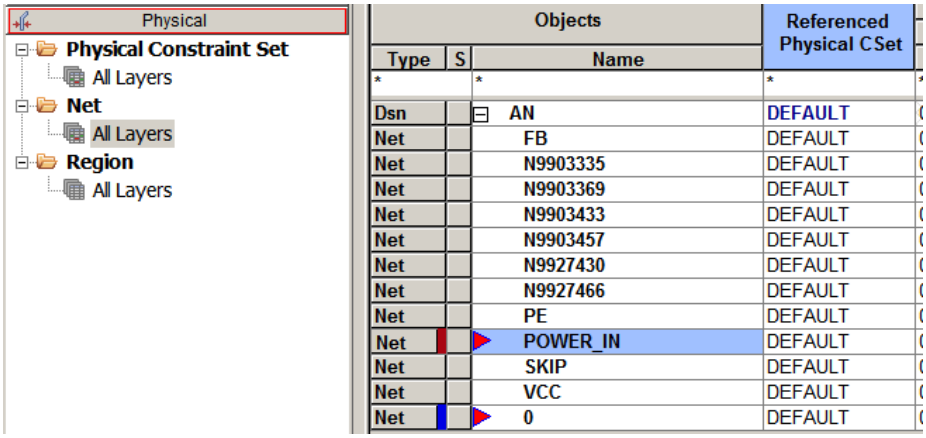
- U2 and R1
- R1 and C1
- C1 and T1
- C1 and U1

The result should look like this

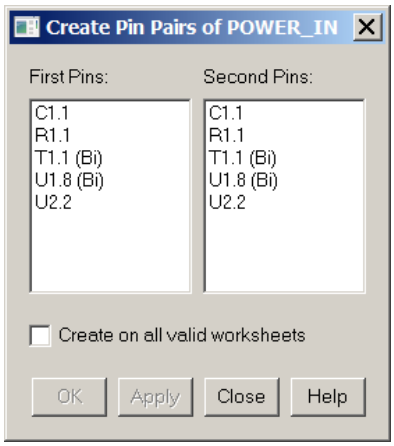


## 2.3 Add physical rules

Open CM and select Physical > Net > All Layers.




Right click on net Power_In > create > Pin Pair.

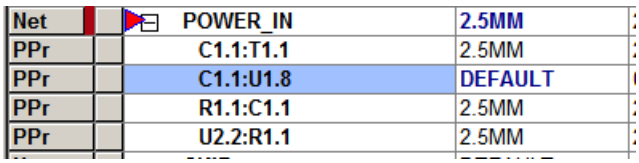



Create these Pin Pairs:

- U2 – R1
- R1 – C1
- C1 – T1
- C1 – U1

Close pin Pair menu. If you get CM Warning window close it using OK.

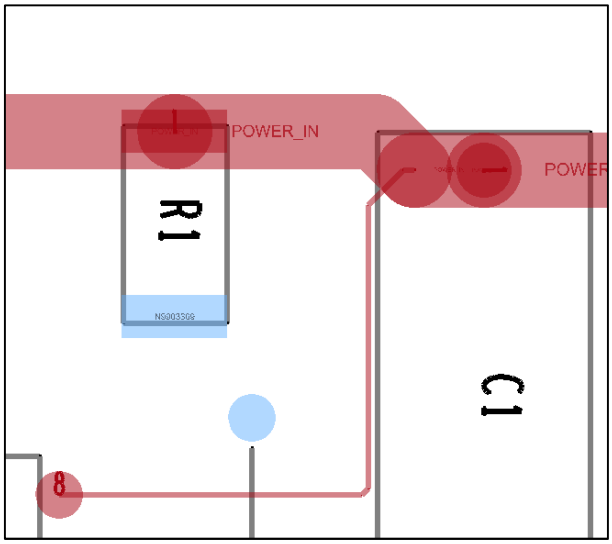
Now assign physical rule 2.5mm to the whole net Power_In and the Default rule to the Pin Pair C1.1:U1.8.




Now you can do your first routing test. Route the connection between U1 and C1 starting from U1 because the pin of C1 is connected to both rules. Only the pin of U1 has a unique setting.

## 2.4 Same Net Spacing

When you route and slide the net Power_In you will see that you can slide the sense connection into the thicker main connections without getting any DRC.



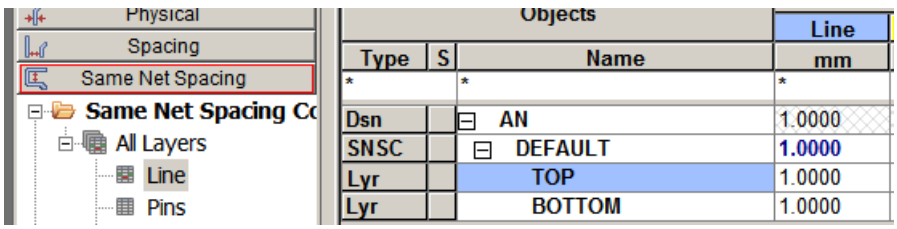

That is not what we like to have. So we need Same Net Spacing rules.

Open CM > Same Net Spacing > Same Net Spacing Constraint Set > Options

| Objects | | | Enable DRC By-Layer |
|---|---|---|---|
| Type | S | Name | |
| * | | * | * |
| Dsn | | AN | TRUE |
| SNSC | | DEFAULT | TRUE |
| Lyr | | TOP | TRUE |
| Lyr | | BOTTOM | TRUE |

The value of Enable DRC By-Layer must be set as TRUE.

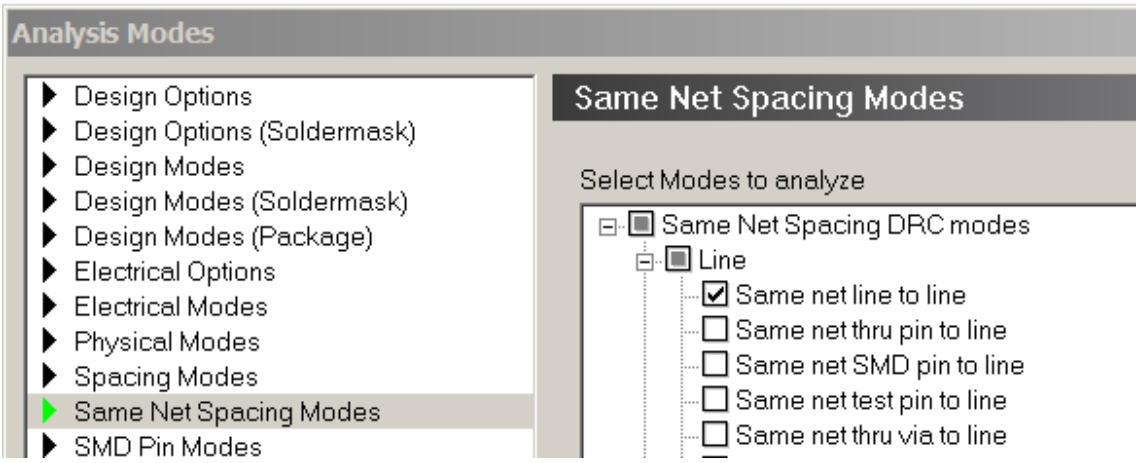
Change to Line in the same category. Set a value for Line to Line Spacing. We use 1mm in our example.




| Objects | | | Line |
|---|---|---|---|
| Type | S | Name | mm |
| * | | * | * |
| Dsn | | AN | 1.0000 |
| SNSC | | DEFAULT | 1.0000 |
| Lyr | | TOP | 1.0000 |
| Lyr | | BOTTOM | 1.0000 |

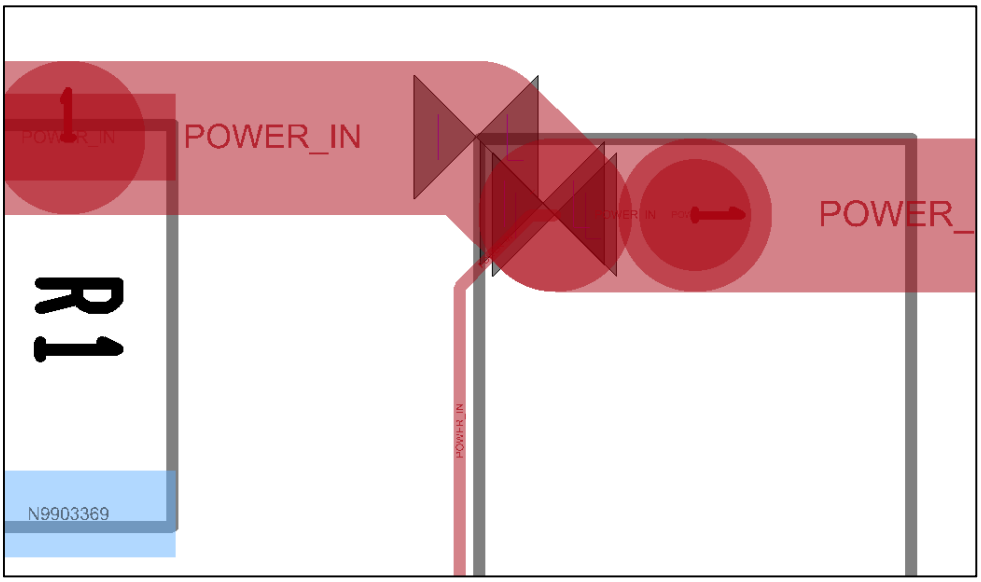
Now you need to activate the Line to Line Same Net Spacing check. In CM go to Analyze > Analyze Modes. In PCB Editor use Setup > Constraints > Modes.

Select Same Net Spacing Modes > expand Line options and activate Same net line to line.

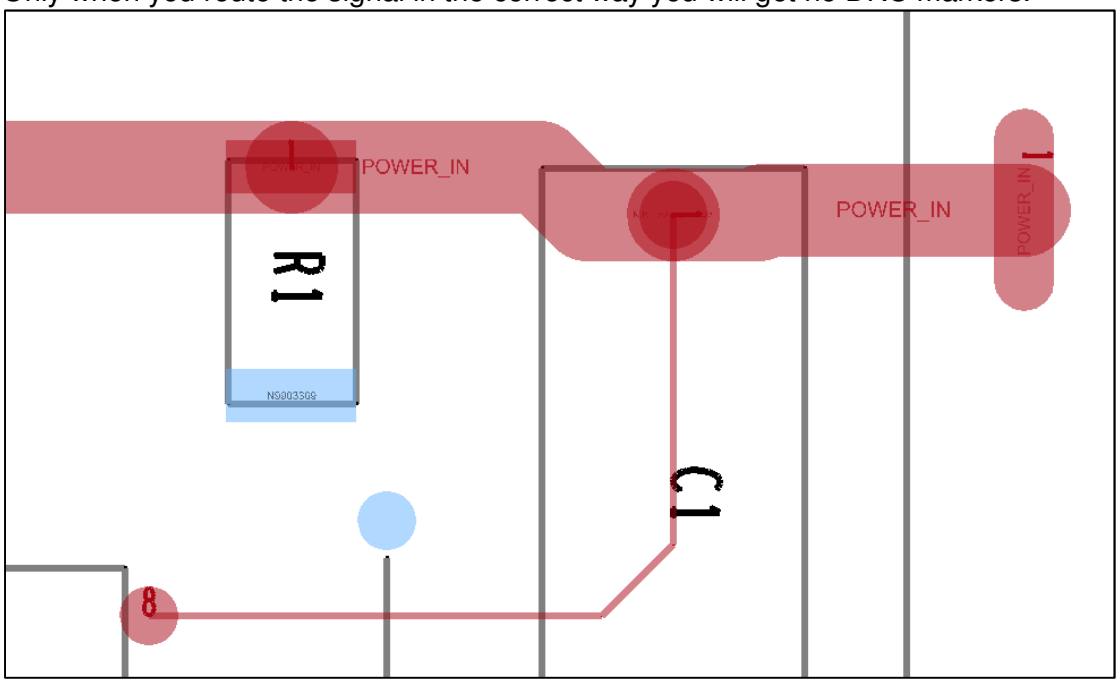



Check if On-line DRC is enabled and close the window using OK.


PCB Editor updates DRC Check and you will get DRC markers if you routed the signal like this.



Only when you route the signal in the correct way you will get no DRC markers.




# 3 Attached examples

Attached you find the Allegro_start.brd without any rules and the Allegro_solution.brd with the complete rule set and routing of net Power_In.

# 4 Solution for OrCAD

In OrCAD PCB Editor the function Net Schedule and Create > Pin Pair are not available. But there is a manual way to route such a net.

## 4.1 Using Neck Mode

Define a physical Cset with Min Line Width = 2.5mm for Main Routing and Min Neck Width = 0.2mm for sense connection. Set Neck Max Length to a value higher then sense connection length. You can change this value at any time.

| Objects | | | Line Width | | Neck | |
|---|---|---|---|---|---|---|
| | | | Min | Max | Min Width | Max Length |
| Type | S | Name | mm | mm | mm | mm |
| * | | * | * | * | * | * |
| Dsn | | ⊟ OrCAD_solution | 0.2000 | 0.0000 | 0.2000 | 0.0000 |
| PCS | | ⊞ DEFAULT | 0.2000 | 0.0000 | 0.2000 | 0.0000 |
| PCS | | ⊞ POWER_IN | 2.5000 | 0.0000 | 0.2000 | 50.0000 |

Assign this Cset to net Power_In.

Now you can route the main connections and then route sense connection using right mouse button > Neck Mode.

Fix this routing because routing other signal may have influence to this net and change it.

## 4.2 Using funckey

If you often want to route a signal with different line width you can define this funckey.

funckey w 'settoggle width 0.1 0.2 0.3 0.5 1 2; echo "Using width " $width;  options acon_line_width $width'

Pressing key w will toggle the routing line width between the listed values. Change the values to the line width you need and place this funckey definition in the beginning of your env file. You find it under $HOME/pcbenv.