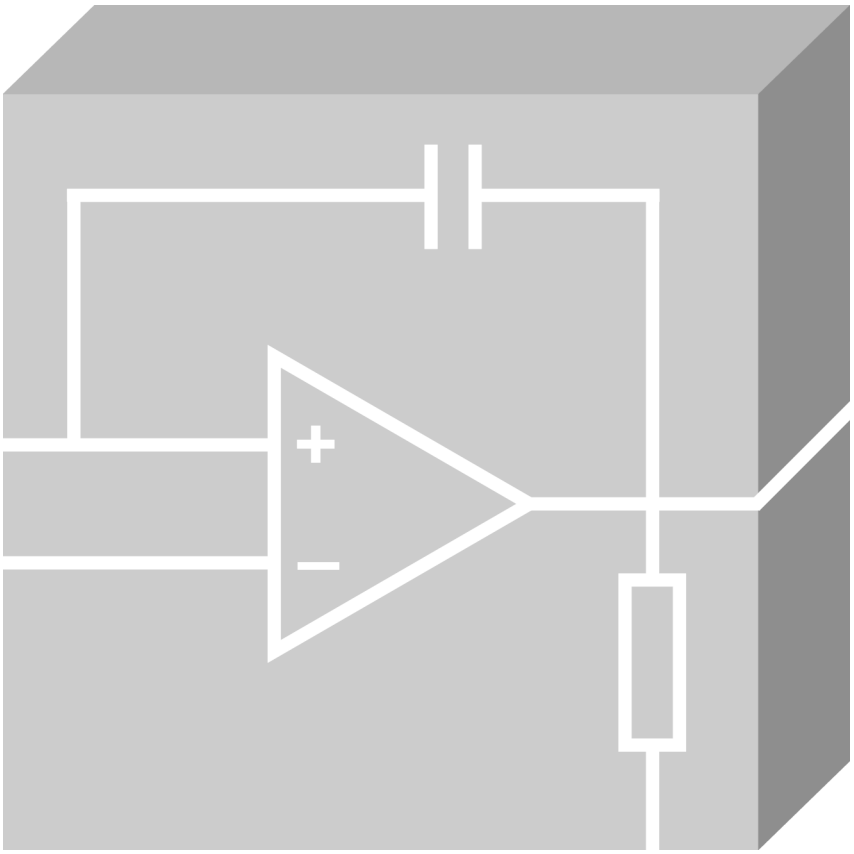
FlowCAD

Shorten Nets/Pins in a Capture Design



OrCAD Capture

Application Note | V1.1

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What are the Available Options to Short Nets / Signals in a Capture Design?

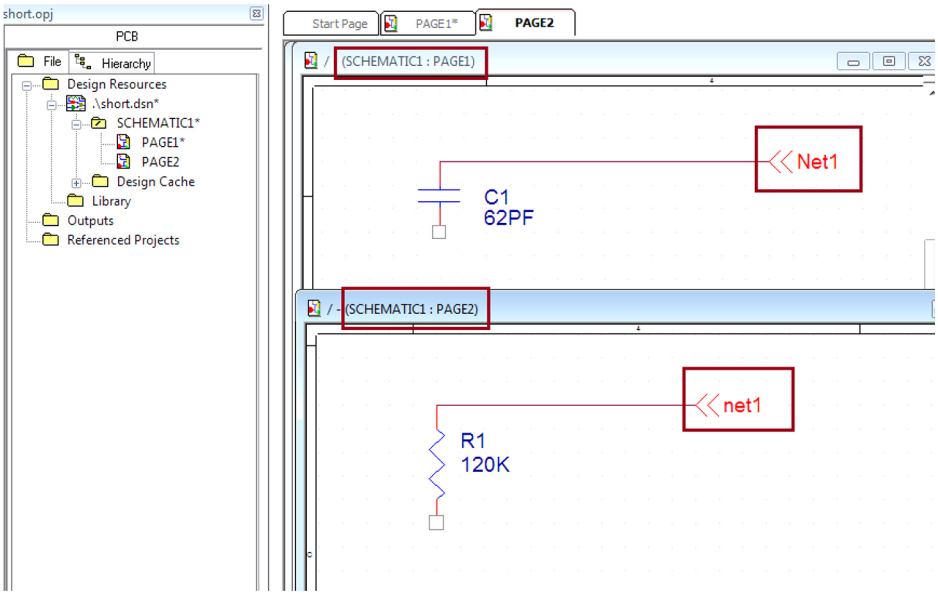
Capture allows you to short nets / signals in a design without actually physically shorting them. This keeps the design very clean. You can short two or more nets on a page, nets on different pages within a schematic folder, nets in different schematic folders, and two or more pins on a component.

Shorting Nets on the Same Page

This can be done by giving the same net alias to two or more nets that are to be shorted. Net alias can be assigned to a net by using the **Place > Net alias** menu or by pressing **N** on the keyboard. It opens the **Place net alias** dialog box. Specify a name for the net and click the net to which you want to assign this alias.

Shorting Nets on Different Pages Within the Same Schematic Folder

Nets connected to the off-page connector with the same name will get shorted. These nets can be on different pages, but they have to be within the same schematic folder. For example, in the following image, C1 and R1 are shorted to each other.



To place an off-page connector on the schematic, go to **Place > Off-Page Connector** or click the toolbar icon.

Shorting Nets in a Hierarchical Design

In a hierarchical design, connection is transferred from a bottom-level design to the hierarchical block through a Hierarchical port (H-port)-Hierarchical pin (H-Pin) pair. A hierarchical block has an H-pin corresponding to every H-port in the schematic to which it points.

In the following image, R1 is connected to C1 through the H-port-H-pin pair NetA.

Note

It is a good practice to assign a net alias to a net connected to the H-pin, like in the above image. The name of the net at the top level gets propagated to the bottom level. So, if a net alias is not assigned to the net coming out to the hierarchal block, it will get a system-generated net name, which might get confusing.

Shorting Pins on a Component

The `PACK_SHORT` property allows you to map one logical pin to two or more physical pins. You can define the `PACK_SHORT` property on a component to short two or more pins on that component.

For example, if you want to short the nets attached to logic pins A1, B1, and Y1 with each other and the nets attached to pins A2 and B2 with each other, you can define the `PACK_SHORT` property as follows:

```
PACK_SHORT = (A1, B1, Y1) (A2, B2)
```

Note

You should not short the pins physically on the schematic if they have already been shorted using the `PACK_SHORT` property.

Refer to the attached pack_short_test.zip file to see an example of how to use the `PACK_SHORT` property.

Shorting Nets with different Netnames Using Net_Short Property

1. Add the NET_SHORT property
   - Add the NET_SHORT property to the pin of the component instance.
   - Take care to be sure to select the pin of the component rather than the attached wire or the component itself. Make the value of the NET_SHORT property GND:AGND.
   - The first netname in the value string is the net that the pin is connected to (GND in this case).
   - The second netname in the value string is the net (AGND) that I wish to allow to short to GND at this point. The netnames are separated by a colon.
2. Set up the allegro.cfg file
   - Save the schematic and select **Tools > Create Netlist > Allegro**.
   - Before netlisting, select the **Setup** button on the Create Netlist form and choose the allegro.cfg file to be edited.

- The allegro.cfg file is loaded into a plain text editor.
- Locate the section called [pinprops] typically towards the bottom of the file.
- Add the line NET_SHORT = YES to this section.
- Save the allegro.cfg file and OK the Setup form.
- Then run the netlister by OK'ing the Create Netlist form.

3. View the results in PCB Editor
   - After netlisting is completed successfully, import the netlist into the board.
   - Place component SP1 and place other components including pins of the net AGND.
   - With Bubble Mode set to Off (instead of Hug Preferred or Shove Preferred) start a cline (add connect) at an AGND pin and draw the cline into the pin of component SP1.
   - No DRC marker is reported even though the cline is on net AGND and the pin of SP1 is on net GND.
   - PCB Editor ignores the violation because of the NET_SHORT property.