

ABM Model Table

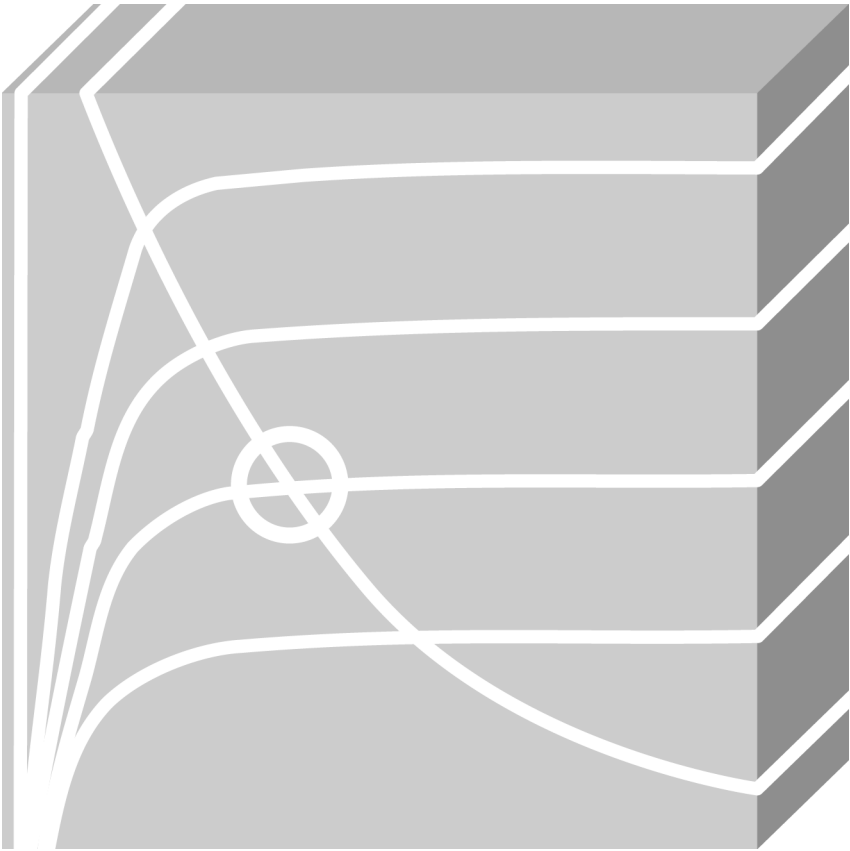


Table of Contents

- 1 Introduction 3**
- 2 TABLE 3**
 - 2.1 Simulation With the Default TABLE 3
 - 2.2 Modify the TABLE 4
- 3 ETABLE and SUBCKT 6**
 - 3.1 Limitation of the Line Length..... 7
 - 3.2 Using a Sub-Circuit..... 7
 - 3.2.1 Define a Sub-Circuit..... 7
 - 3.2.2 Create a Capture Symbol 8
 - 3.2.3 Configure the Capture and PSpice Library for Simulation 9
- 4 Bibliography 9**

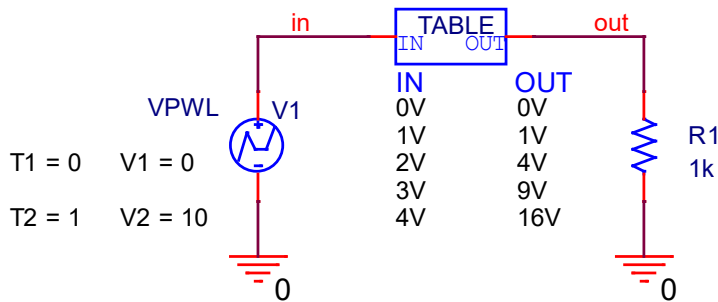
1 Introduction

The ABM (Analog Behavioral Modeling) part TABLE provides a lookup table that is used to correlate an input and an output based on a set of data points. Per default, you can use up to five value pairs to define the table. However, you can modify it to allow more value pairs available.

The part ETABLE is a voltage-controlled voltage source using a transfer function described by a table. But the length of the table is limited to 132 characters. You can define a sub-circuit to avoid this limitation. Once this is done, you can create a Capture symbol for this model using PSpice Model Editor.

2 TABLE

A simple demo circuit in the project etable_subckt.opj is created as follows and the voltage source used here is VPWL.



2.1 Simulation With the Default TABLE

Run the simulation for e.g. 1 second. The input and output voltage can be displayed in the Probe Window.

If you want to show the data points of curves, click **Tools > Options... > General** in Waveform Viewer and select the option **Mark Data Points**.

Or use the symbol .

The TABLE part has default 5 rows. Each row contains an input and a corresponding output value. Linear interpolation is used between data points. For example in Fig. 2,

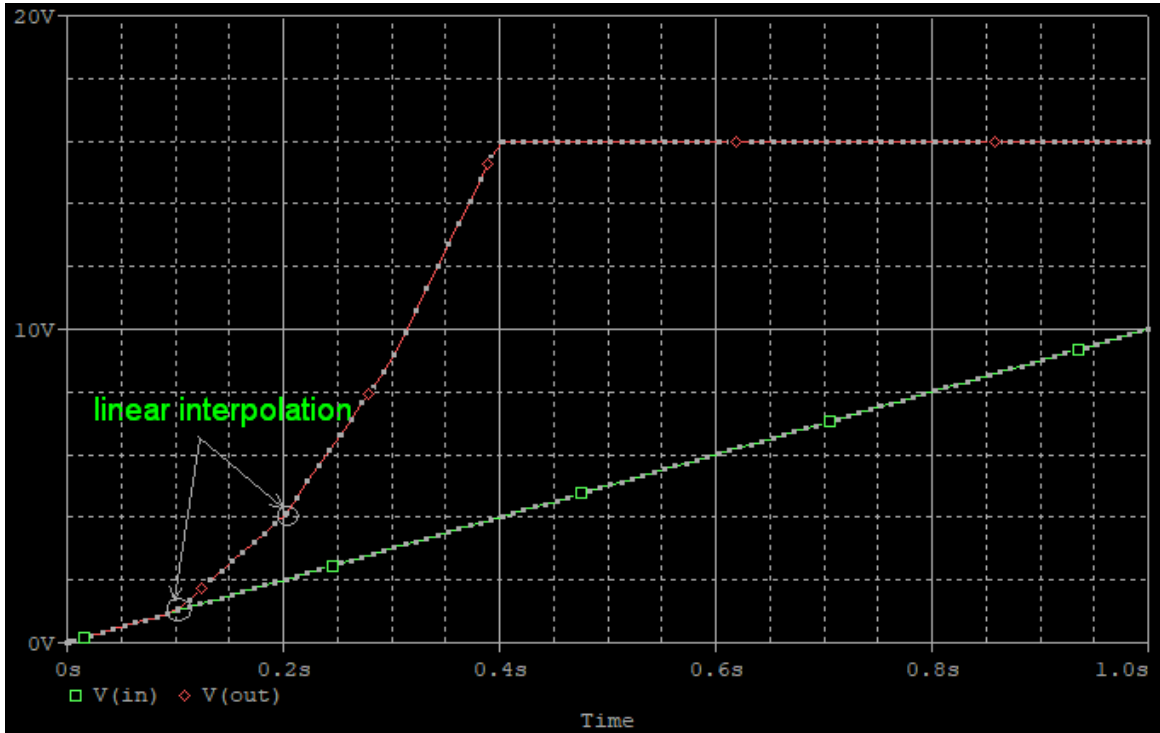
$$V(\text{in}) = 1\text{V} \rightarrow V(\text{out}) = 1\text{V}$$

$$V(\text{in}) = 2\text{V} \rightarrow V(\text{out}) = 4\text{V}.$$

The data points between 1V and 4V of V (out) are linear interpolated.

Note

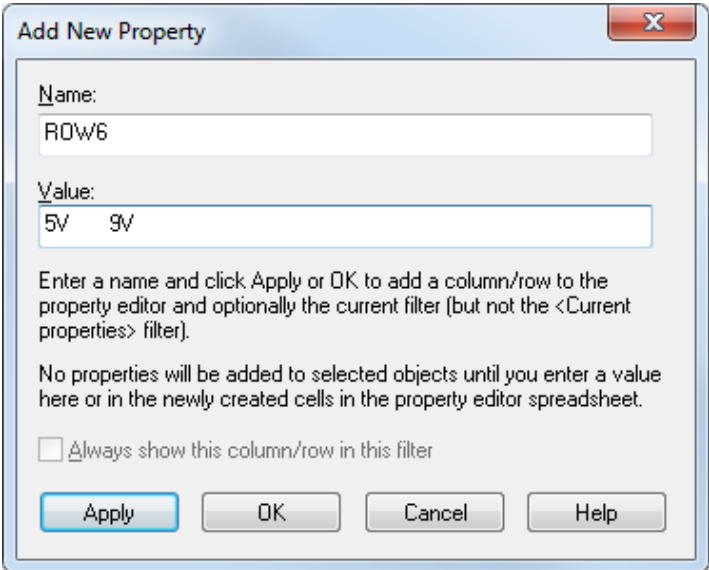
Values of input must monotonically increase.



If input values are outside the range of the table, the device’s output is a constant with a value corresponding to the entry with the smallest (or largest) input. In the above example, the corresponding output voltage is 16V because of $V(in)=4V$. The input voltage increases further, but the output voltage remains 16V.

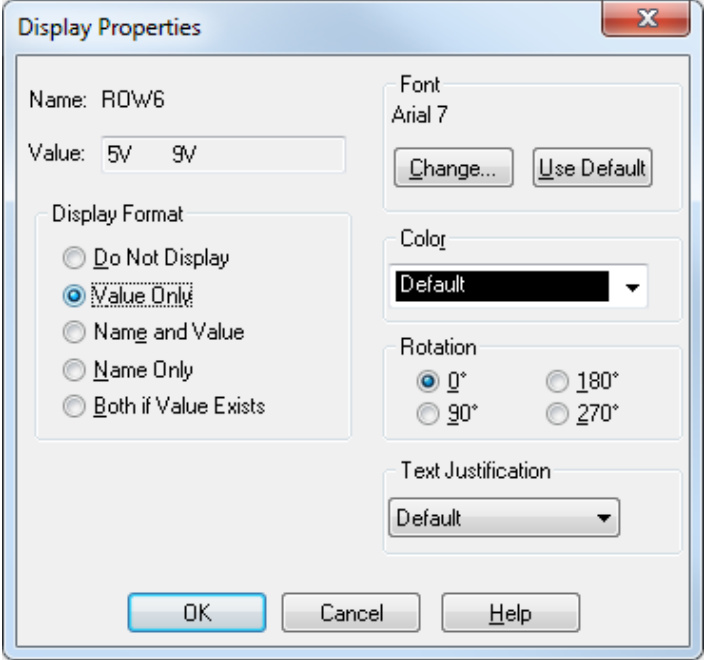
2.2 Modify the TABLE

If you want to add more value pairs, the TABLE part can be customized through the Property Editor. Select the part TABLE, double click it and the Property Editor comes up. Click the button **New Property...**

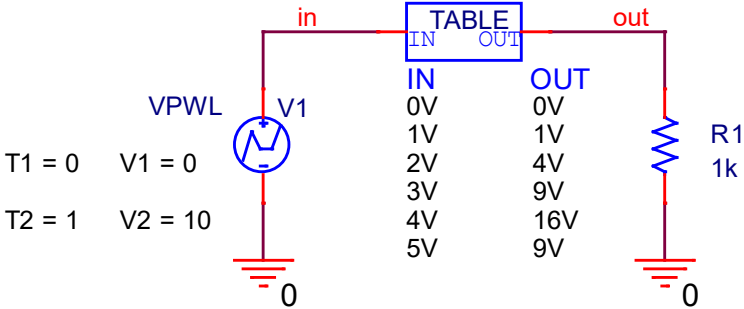


Enter the name and the value in this dialog window and click **OK**.

Move the mouse over the property ROW6 in the Property Editor, highlighting it. Then click the right mouse button and select **Display...** from the context menu, the **Display Properties** dialog window comes up.



Set the Display Format **Value Only** to show this property in the schematic. Now you will see the newly added row is displayed.



In order to make the extended table available for the PSpice simulation, you have to modify the property **PSpiceTemplate** in the Property Editor.

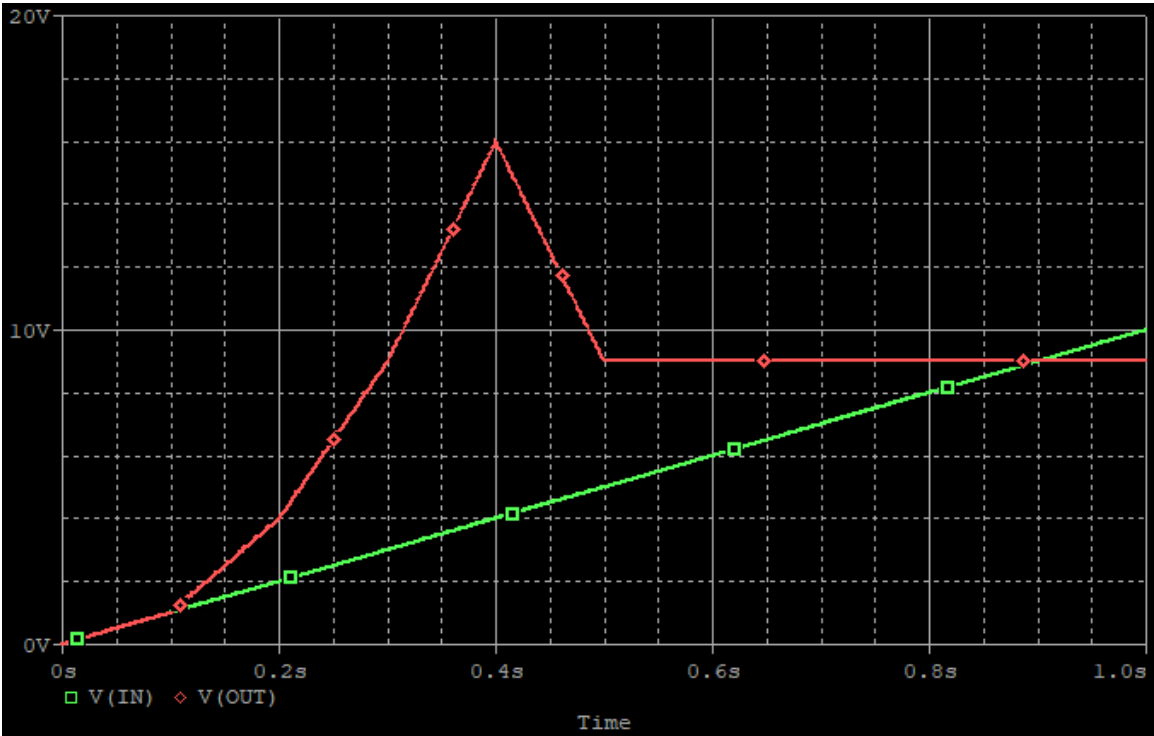
Change the original PSpiceTemplate from

- `E^@REFDES %OUT 0 TABLE {V(%IN)} @ROW1 ?ROW2| \n+ @ROW2| ?ROW3| \n+ @ROW3| ?ROW4| \n+ @ROW4| ?ROW5| \n+ @ROW5|`

to

- `E^@REFDES %OUT 0 TABLE {V(%IN)} @ROW1 ?ROW2| \n+ @ROW2| ?ROW3| \n+ @ROW3| ?ROW4| \n+ @ROW4| ?ROW5| \n+ @ROW5|?ROW6| \n+ @ROW6|`

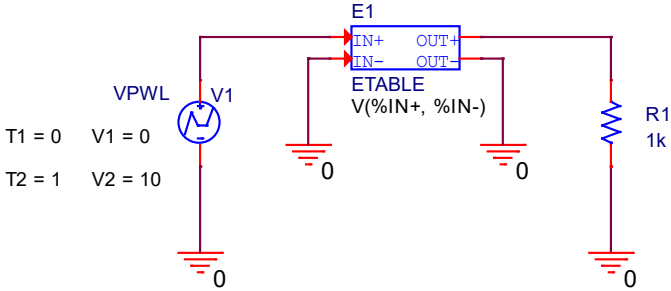
Run the simulation for 1 second. This time the input and output voltage can be displayed as follows:



Simulation result with extended table

3 ETABLE and SUBCKT

You can use the part **ETABLE** in **ABM.OLB** library to define a voltage-controlled voltage source. A simply example is as follows:



3.1 Limitation of the Line Length

If you open the Property Editor and you should see a property named **TABLE**.

A	
	root : PAGE1 : E1
Color	Default
Designator	
EXPR	V(%IN+, %IN-)
Graphic	ETABLE.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	660
Location Y-Coordinate	140
Name	INS29052
Part Reference	E1
PCB Footprint	
Power Pins Visible	<input type="checkbox"/>
Primitive	DEFAULT
PSpiceOnly	TRUE
PSpiceTemplate	E^@REFDES %OUT+ %OUT- TABL
Reference	E1
Source Library	C:\CADENCE\SPB_16.6\TOOL
Source Package	ETABLE
Source Part	ETABLE.Normal
TABLE	(-15,-15) (15,15)
Value	ETABLE

The input and output value pairs are given for the TABLE property. Unfortunately, PSpice can not accept more than 132 characters for a table. An error occurs in the output file and the simulation aborts.

ERROR - Line too long. Limit is 132 characters.

3.2 Using a Sub-Circuit

3.2.1 Define a Sub-Circuit

In order to solve this problem, a sub-circuit is used to define a voltage-controlled voltage source using a TABLE. You can use any texteditor to define a sub-circuit.

Save the File as .txt and rename it to .lib. Define a sub-circuit, e.g. my_ETABLE, as follows and save it as e.g. my_sub.lib.

```

1 .SUBCKT my_ETABLE IN+ IN- OUT+ OUT-
2 E_E1 OUT+ OUT- TABLE { V(IN+, IN-) }= (
3 +(0,0)
4 +(0.004,0.004)
5 +(0.128,0.128)
6 +(0.628,0.628)
7 +(1.128,1.384)
8 +(1.628,2.884)
9 +(2.128,4.639)
10 +(2.628,7.139)
11 +(3.128,9.896)
12 +(3.628,13.396)
13 +(4.128,15.104)
14 ***you can give more value pairs here***
15 +)
16 .ENDS my_ETABLE
17

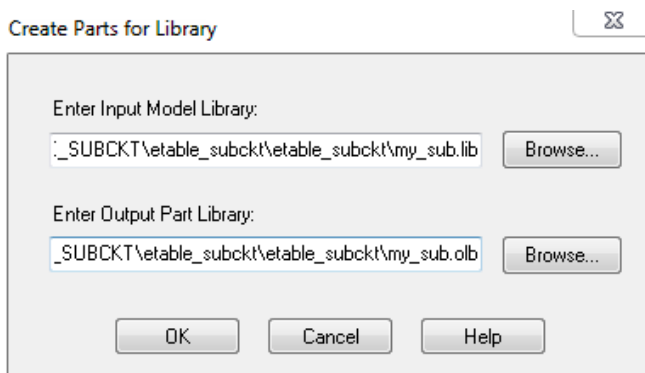
```

Note

If a definition is too long for a line, you can distribute it over multiple lines using the continuation sign +. It should be added at the beginning of a new line, here starting in the third line.

3.2.2 Create a Capture Symbol

- Open PSpice Model Editor through **Start > All Programs > Cadence > Release 17.2 > PSpice Accessories > Model Editor** and then select **Capture** if you are asked which design entry tool you are using.
- **File > Open** find the my_sub.lib and open it in the Model Editor.
- **File > Export to Capture Part Library...**



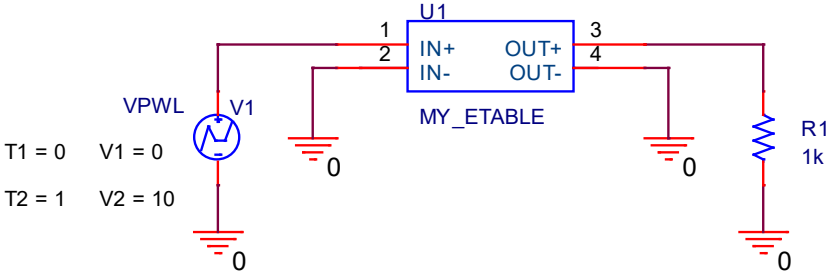
- Click **OK**, and if the **Enter Output Part Library** is left unchanged, a Capture symbol library will be created in the same directory in which the PSpice library is located.

Note

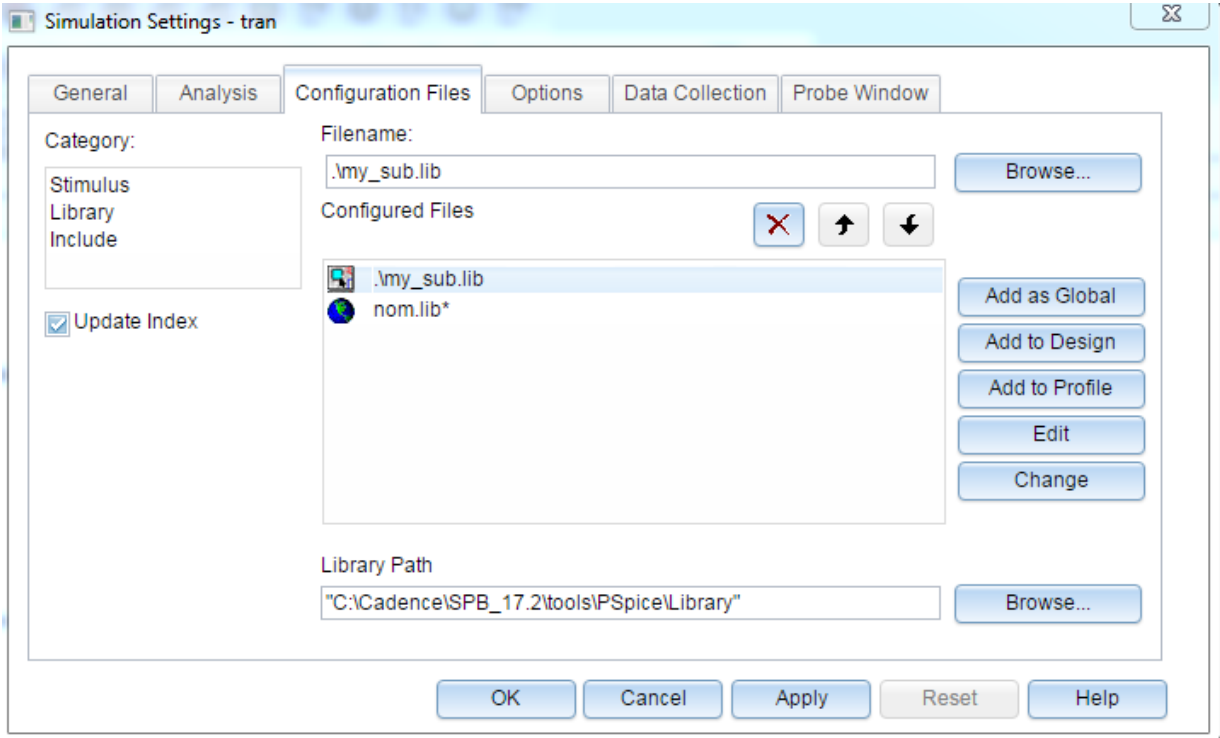
Per default, the Model Editor will create a rectangle graphic as a Capture part based on a PSpice sub-circuit definition.

3.2.3 Configure the Capture and PSpice Library for Simulation

Place the newly generated part in the schematic and build up a test circuit as follows:



The PSpice library must be configured, so that PSpice can find this sub-circuit for the simulation.



- In the **Simulation Settings** window, select the **Configuration Files** register, select **Library** from **Category**, and click the button **Browse** to find my_sub.lib and **Add to Design**. Click **OK** to finish the configuration.
- Run the simulation for 1 second.

Note

You can use a sub-circuit to avoid the limitation of the character length not only for the part ETABLE, but also for parts (e.g. GFREQ) which use look up table to define value groups.

4 Bibliography

[1] PSpice User’s Guide, Cadence
 [2] OrCAD Capture User’s Guide, Cadence