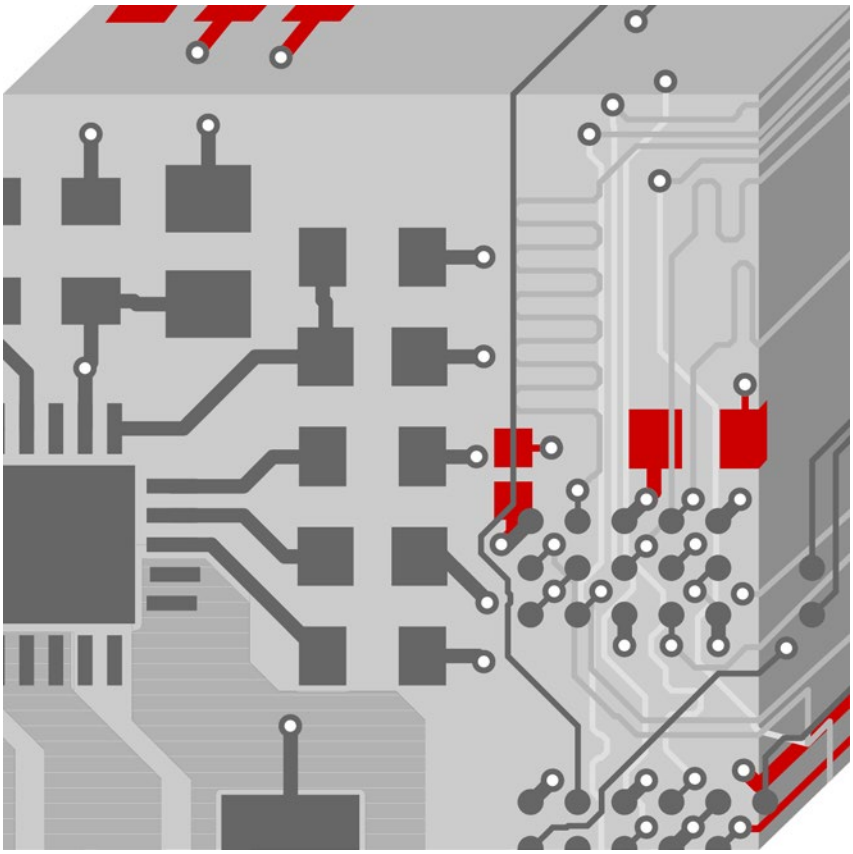
FlowCAD

Testpoint Generation



Allegro / OrCAD PCB Designer

Application Note | V2.0

FlowCAD

Table of Contents

1 Introduction

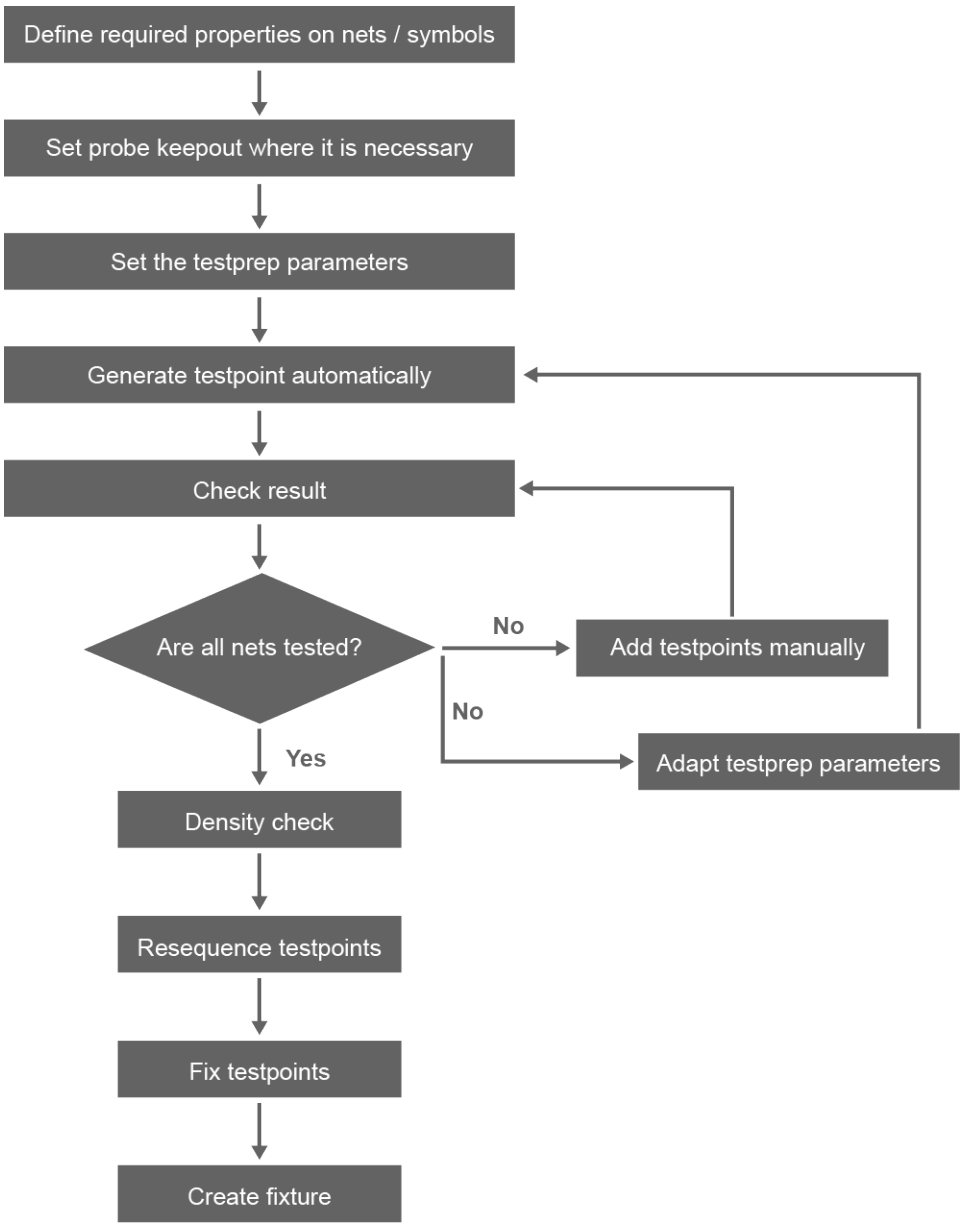
This application note describes how you can generate testpoints on your PCB. It explains the different parameters which you can set to obtain the best result.

Note

Generating testpoints is not a one click command. First set the properties / parameters, and then generate the testpoints. Check the result and modify the parameters afterwards. Change the settings and set the missing testpoints, until you get the desired result.

Depending on the test method, you have different requirements. Please contact your PCB or ICT Engineers to check for requirements e.g., regarding the minimum size of the testpads and the distance between the testpoints, etc.

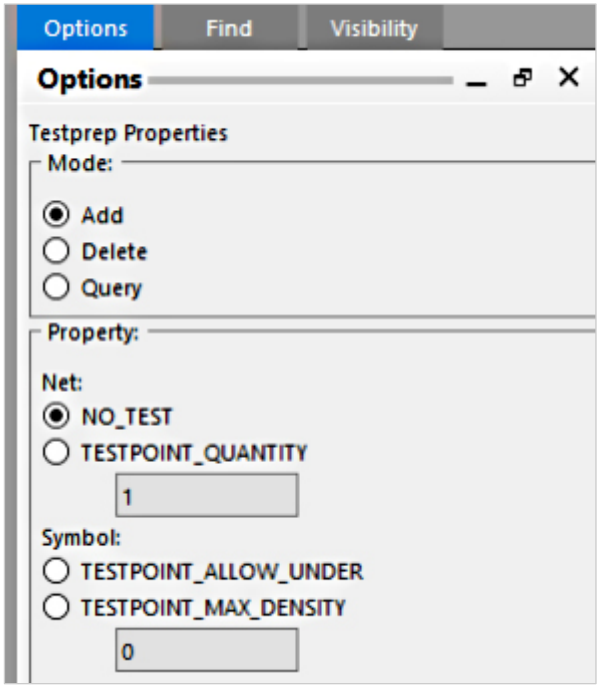
1.1 Process Flow



2 Setup and Preparations

2.1 Add Properties Manually

With **Manufacture > Testprep > Properties** you can define properties before automatically generating testpoints. For example, you can specify which nets won't be tested.



How to proceed:

1. Chose the mode for the property. E.g.: Add or Delete
2. Select the property.
3. Select the desired net or symbol in the PCB.

Explanation of the properties:

NO_TEST	Add this property on a net, when it doesn't require testpoints.
TESTPOINT_QUANTITY	Limit the number of testpoints on a net.
TESTPOINT_ALLOW_UNDER	Attach this property to a symbol to allow testpoints underneath a component instance of a symbol and override the **Allow under component** field on the Testprep Parameters dialog box if it is enabled. Typically used on mechanical parts or components inserted after test.
TESTPOINT_MAX_DENSITY	Attach this property to a symbol to specify the maximum number of testpoints desired under a symbol.

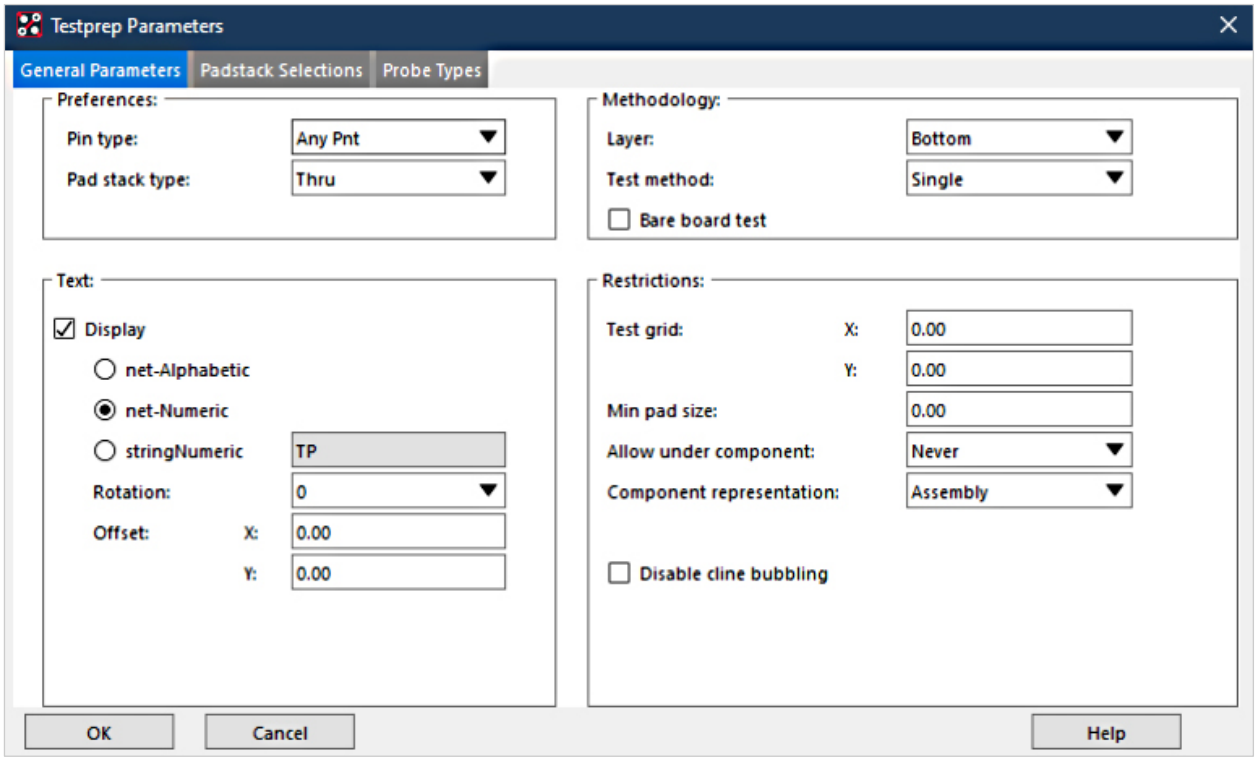
2.2 Probe Keepouts

For areas where no testpoints are allowed, you can add probe keepouts (**Setup > Areas > Probe Keepouts**). The keepout areas can be set for top and bottom of the PCB individually.

2.3 Testprep Parameters

With **Manufacture > Testprep > Parameters** you can determine the output of the automatic or manual testpoint generation process by setting the parameters.

2.3.1 General Parameters



In this chapter, the general parameter settings are described.

Preferences

- Pin Type: Specifies the type of pin that can be chosen for testing:
  - Input
  - Output
  - Any pin (input and Output)
  - Via
  - Any Pnt (all listed types can be used)
- Pad stack type: Specifies the type of pad needed as a contact point for the test probe (SMT Testpad, Thru Via, Either). You can restrict probing to either SMT pads or through-hole pads, or both by toggling this field. The default is through-hole pads.

Methodology

- Layer: Specifies the side of the design on which testpoints can be set.
  - Top: Allegro PCB Editor chooses probe points only on the top side of the design.
  - Bottom (default): Allegro PCB Editor chooses probe points only on the bottom side of the design.
  - Either: Allegro PCB Editor sets probes on both sides with a preference given to the Bottom subclass.
- Test method: Specifies the number of probe points per net.
  - Single: One testpoint per net (for in-circuit).
  - Node: indicates Allegro PCB Editor designates every endpoint on a net.
  - Flood: indicates that Allegro PCB Editor should designate one testpoint for every pin or via in the net (recommended for bare board testing).
- Bare board test: Specifies if the board is assembled during testing or not. If checked, any component pin is eligible for testing on either side of the design as long as it has a padstack defined on that side.

Text

- Display: When enabled, a text for the testpoint will be generated on the MANUFACTURING/PROBE_TOP or PROBE_BOTTOM layer.
- Net-Alphabetic: Testpoint name contains the net name and an alphabetic incremental extension, started by A.
- Net-Numeric: Testpoint name contains the net name and a numeric incremental extension, started by 1.
- stringNumeric: The testpoint name use the string and appends an incremental number.
- Rotation: Specifies the orientation of text labels. You can choose 0, 90, 180, or 270 degrees.
- Offset: Specifies the position of the text measured from the pad center in the X and Y directions.

Note

Allegro PCB Editor increments additional extensions to any new testpoints but does not replace any testpoints you delete from a sequence. For example, if a net has testpoints GND-1, GND-2, and GND-3, and you delete GND-2, the next testpoint is GND-4.

Restrictions

- Test Grid: Specifies grid dimensions for the test fixture. Allegro PCB Editor chooses or inserts testpoints from pads on this grid. A grid value of zero means no grid restriction.
- Min Pad size: Specifies a minimum pad size for testpoints. If test pads are too small, testprobe (testpin, pogo pin) may slip off during testing. No pin or via pad that is smaller than this value is chosen as a testpoint.

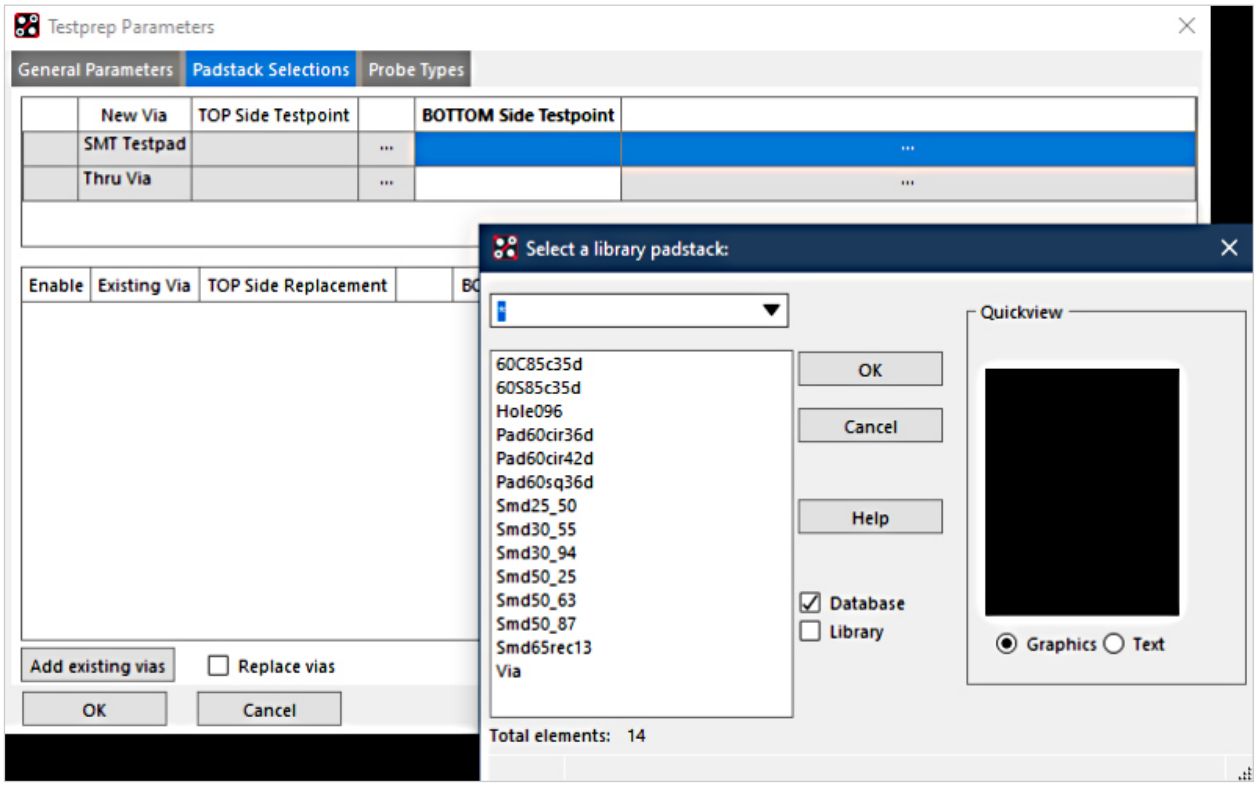
- Allow under component: Specifies if testpoint can be added under a component or not.
- Component representation: Choose to use ASSEMBLY or PLACE_BOUND data to determine the area that a component covers and the component outline for testpoint-to-component spacing design rule checking on both sides of the board.
- Disable cline bubbling: Prevents bubbling to avoid DRC errors when adding a testpoint via directly on a trace or replacing a via pad while automatically or manually generating testpoints.

Note

If the board grid is very small it is recommended to define a larger testgrid (2.54 mm for example). This accelerates the process when creating testpoints automatically. After the first run you can tighten the grid if required. The auto generator is much faster, if the test grid setting is not too small.

2.3.2 Padstack Selections

You can determine which padstack shall replace the existing one, when it becomes a testpoint. You can define multiple via sizes, thru and blind vias, for TOP and BOTTOM side testing.

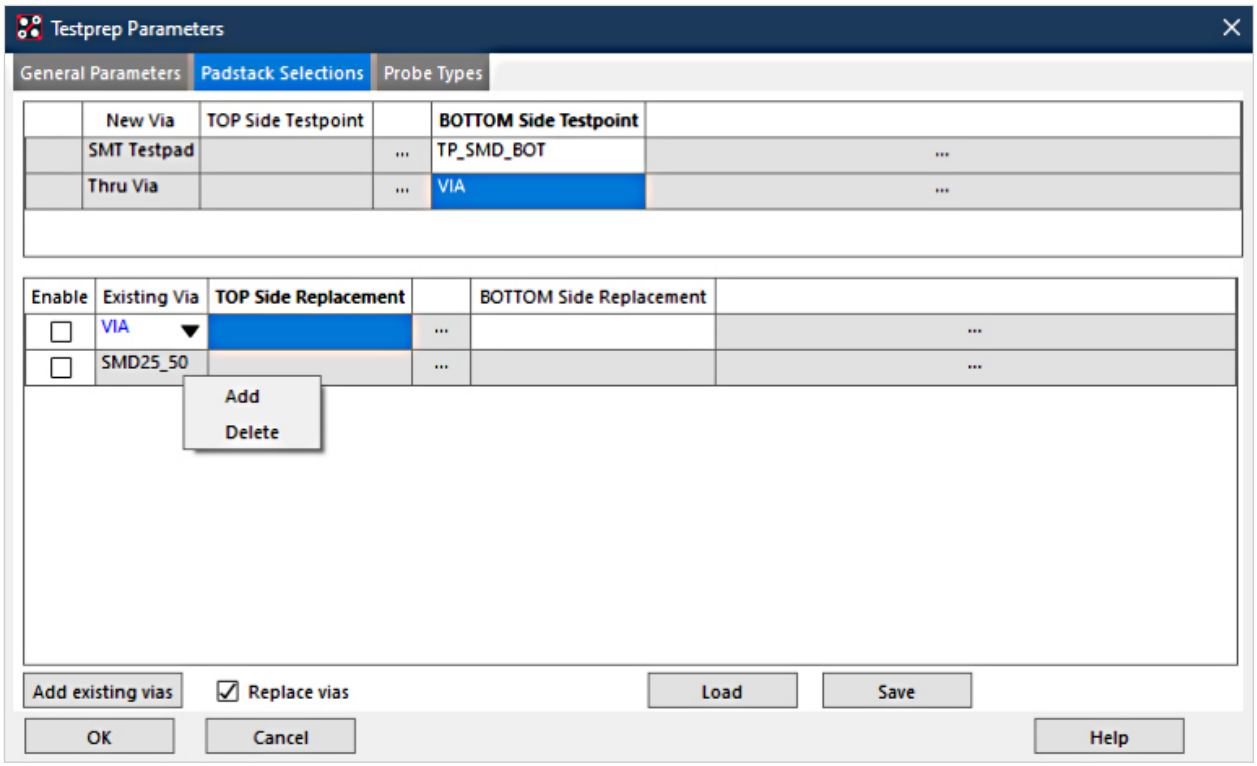


In the upper table it can be defined, which Pads or Vias are used when a new via or pad entity is being created as a testpoint.
Depending on the settings in the general Parameters, TOP Side Testpoint or Bottom Side Testpoints may be greyed out and can't be modified. (When only testpoints on the bottom side are allowed, only BOTTOM Side Testpoints are changeable.)

SMT Testpad is used when you want a single-layer surface-mount pad to be used as a testpoint (for example, when a testpoint is being added to either a TOP or BOTTOM side trace).

Thru Via is used when you want a through-hole pad to be used as a testpoint (for example, when a testpoint is being added with Testprep Automatic pin escape insertion).

Replace Existing Vias



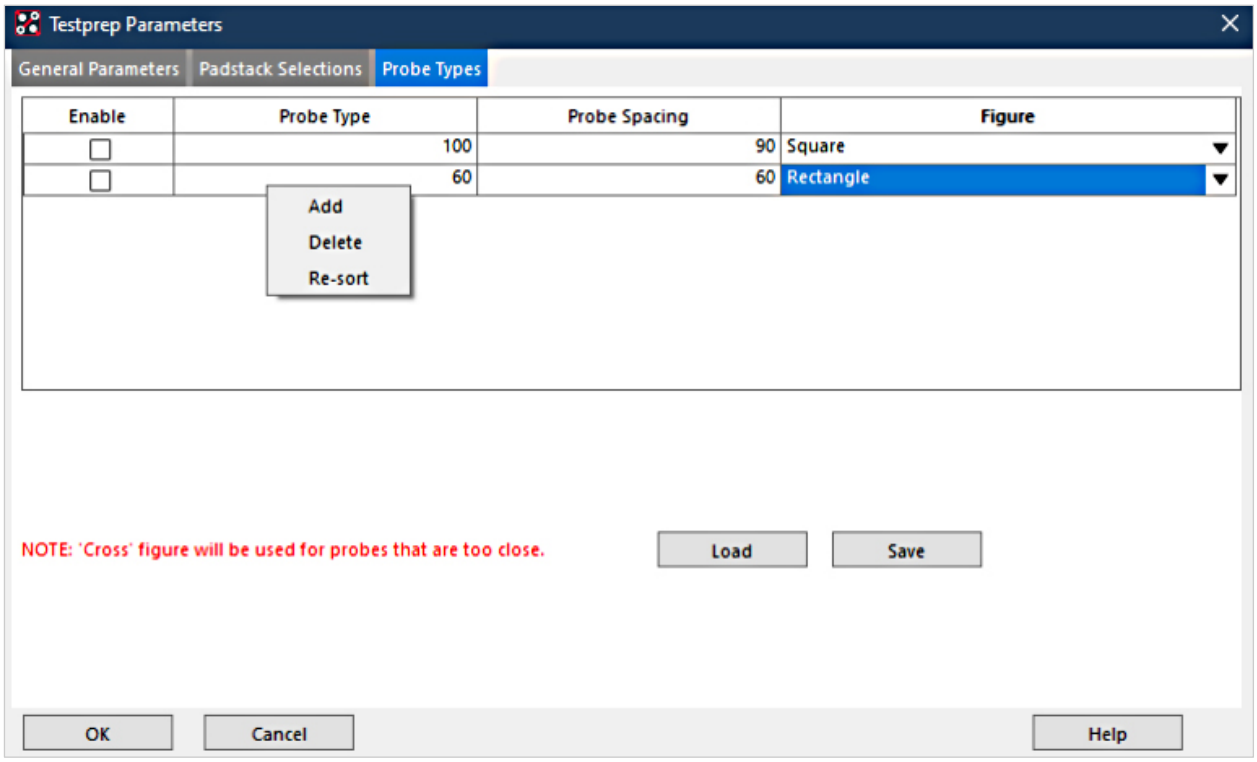
In the lower table you can define which existing testpoint via should be replaced. Initially, the table will be empty. The option **Load new existing vias** will populate the form with all vias used currently in the design.

RMB can be used to add / delete padstacks in **Existing Via** column.

RMB can be used to enable / disable all in **Enable** column.

The **Replace vias** checkbox disable the bottom column.

2.3.3 Probe Types



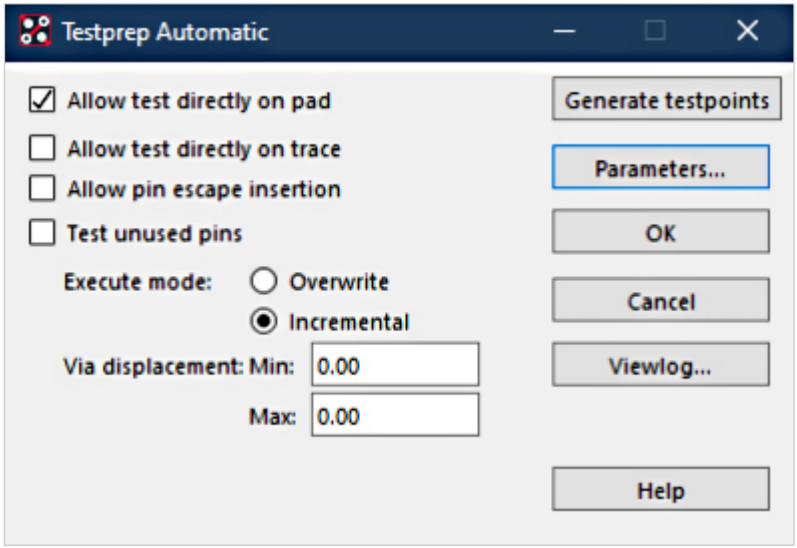
To avoid recursively running testprep to achieve optimal test coverage, you can define probe sizes and spacing combinations on the **Probe Types** tab of the Testprep Parameters Dialog Box. The Probe Types tab defines largest to smallest spacings, for example:100, 75, 50, etc., correlated to probe types, or names, used in the fixture. The greater the spacing, the more rigid the probe can be. Conversely, with tighter spacing (50 mils or less), the probes have to be thinner and are more flexible, which can create fault or structural issues in the fixture bed.

Use the Enable switch to choose the probe types that guide automatic testprep. If you enable two or more probe types and spacings, testprep runs sequentially from highest to lowest probe type. After you manually add or change test probes, you choose **Manufacture > Testprep > Resequence** with the relevant probe type settings enabled and testprep rescans the board and assigns probe types based on current spacing (further down are more explanations about the resequencing function).

When testprep creates a testpoint using a probe type / spacing combination, an internal TESTPOINT_PROBE_TYPE property (not user modifiable) attaches to the pin or via associated with it, whose value equals the probe type. If a specified testpoint cannot be added based on the first probe type/spacing combination, the layout editor attempts the other combinations in sequence until all nets get the required number of testpoints, or all probe type / spacing combinations are exhausted.

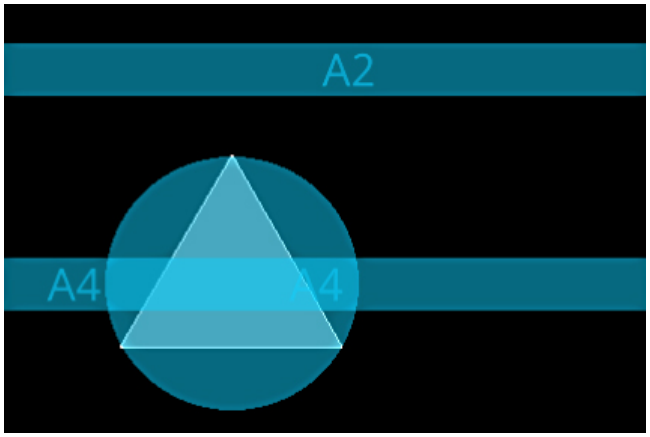
3 Automatic Testpoints Generation

Manufacture > Testprep > Automatic

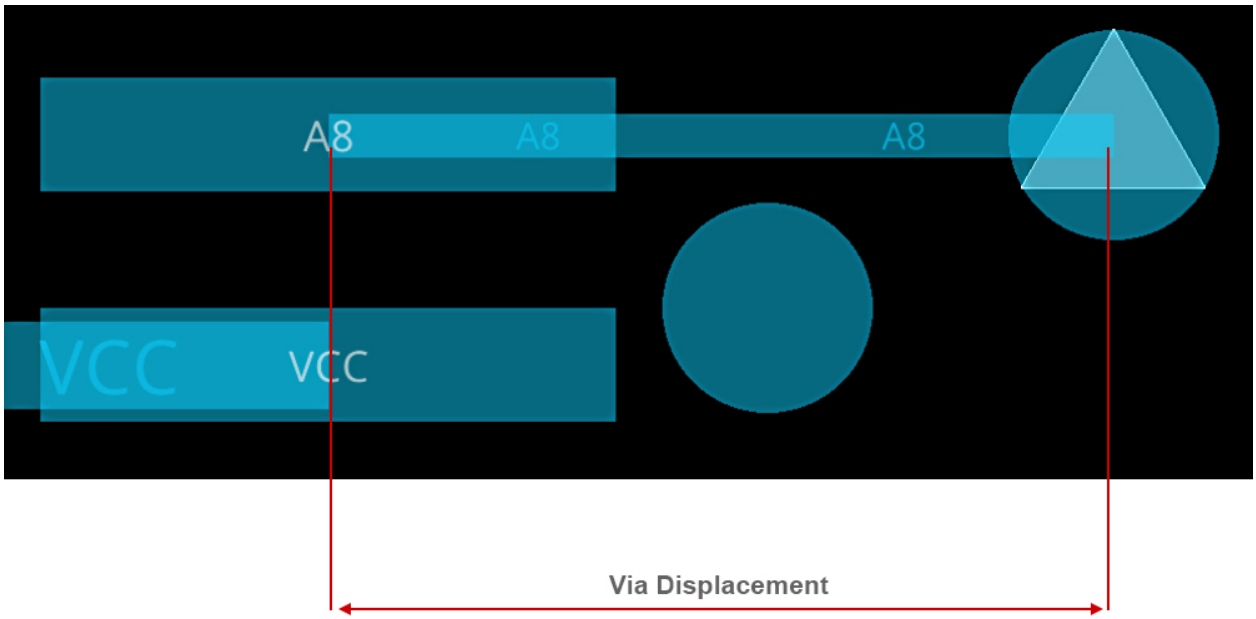


- **Allow test directly on pad:** Specifies whether a pin or via can be selected as a test point:

- **Allow test directly on trace:** Auto generates a SMT pad to connect lines on external layers following all the restrictions defined.



- **Allow pin escape insertion:** Auto generates a via if no other suitable test site exists and will follow all the restrictions defined. This works with the Test Pad / Via field in the Preferences section.



- **Via displacement:** Min / Max, distance from the pin a testpoint can be added.
  Enter a reasonable value for the maximum via displacement or begin with a little value. The bigger the maximum distance, the longer it lasts until the automatic testprep process will be finished.
- **Test unused pins:** Allows pins with no net assignment to be tested. This is done to find solder bridging.

Execute Mode

- **Overwrite**, removes and regenerates all testpoints that currently exist on the board.
- **Incremental**, will not remove existing testpoints and will add any new testpoint location. Used when you have small changes to a board and want to save the original test fixture.

3.1 Logfile

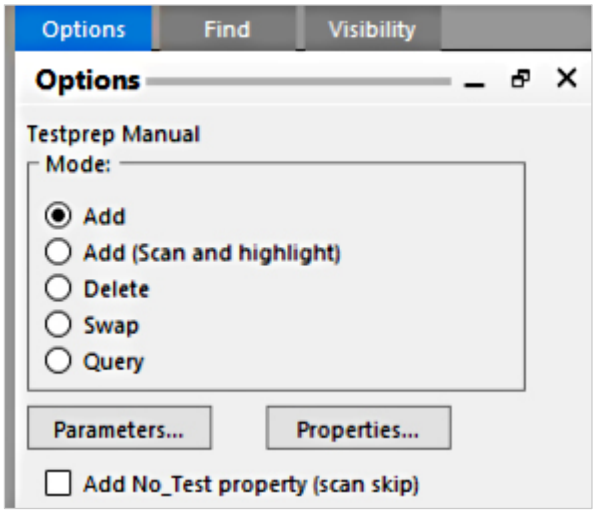
When you run testprep, the layout editor generates an ASCII file called **testprep.log** that summarizes the most recent execution of the testprep program. It lists all parameters, net names, and pin numbers for all testpoints. Other statistics are warnings, fails, completions, location (top or bottom), ignores (no test nets), and failure reasons. To access this file, click **View Log** on the Testprep Automatic dialog box or choose **File > Viewlog**.

4 Set / Modify Testpoints Manually

After you generate testpoints automatically, you can modify them interactively manual.

All the commands for editing testpoints manually, are available in **Manufacture > Testprep > Manual**:

- Add: Add a testpoint to via, pin or Cline
- Add (Scan and Highlight): Each untested nets are highlighted and fits into the window screen. So, you can check if untested net step by step.
- Delete: Removes the testpoint symbol on a via or pin and also reverts the test via to the original via padstack name if the Replace Via option was used. It also removes the physical via itself if it resulted from adding a testpoint to a trace, or from testprep automatic pin escape insertion. Removing a pin escape via removes the associated routing as well.
- Swap: Exchanges the testpoint location to another location on the same net
- Query: After selecting a net, all the property associated with the net are displayed.



5 Testpoint Report

With **Tools > Quick Reports > Testprep Report** you can generate a report. This report generates a summary of how many nets have a testpoint. You also get a list with all available nets with their corresponding testpoints and coordinates. All the nets without a testpoint are also listed.

6 Density Check

In-circuit test engineering limits the maximum number of testprobes that can be placed within a defined area or under a specific component. Dense testprobe placement can damage PCBs.

To verify the testpoint density within user-definable unit areas, choose **Manufacture > Testprep > Density Check** (**testprep density** command). You specify the maximum number of testpoints allowed per unit area in the **Max testpoints per Unit Area** field. Exceeding this value creates rectangular figures that correspond to the user-defined unit areas and overlay the PROBE_DEN_TOP and PROBE_DEN_BOTTOM subclasses of the MANUFACTURING class.

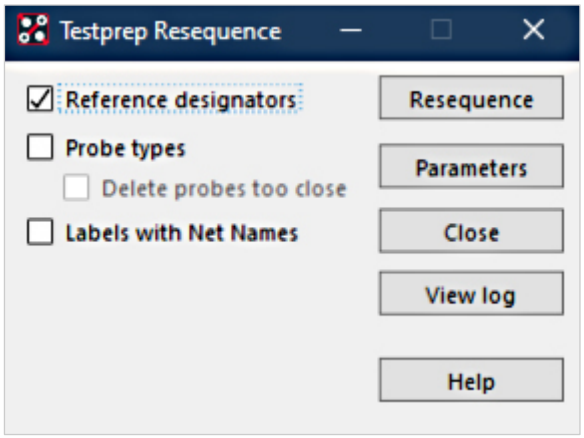
The layout editor automatically creates or clears these subclasses as required to verify the testpoint density within the areas of violation.

7 Create Fixture

Once you finished defining your testpoints, you can **create fixture** (**Manufacture > Testprep > Create FIXTURE**). This generates new subclasses (FIXTURE_TOP and FIXTURE_BOTTOM). On this subclass you'll find graphic symbols of your placed testpoints. When during a design revision you might move or change testpoints, the fixture is not modified. At the end of the design review process, you can check if all the testpoints match with the symbol on the fixture subclasses. When not, you can move the testpoints, so that they'll match again. The aim is, that you can reuse you're existing test environment.

8 Testprep Resequencing

Manufacture > Testprep > Resequencing



To test this function; Rename the refdes text of testpoints to ensure a visually sequential appearance, sorted by X / Y location from left to right and bottom to top on each side, starting with the TOP side first and then the BOTTOM side.

9 Fixing / Unfixing Testpoints

To lock testpoints, they can be fixed with following command:
Manufacture > Testprep > Fix / unfix testpoint

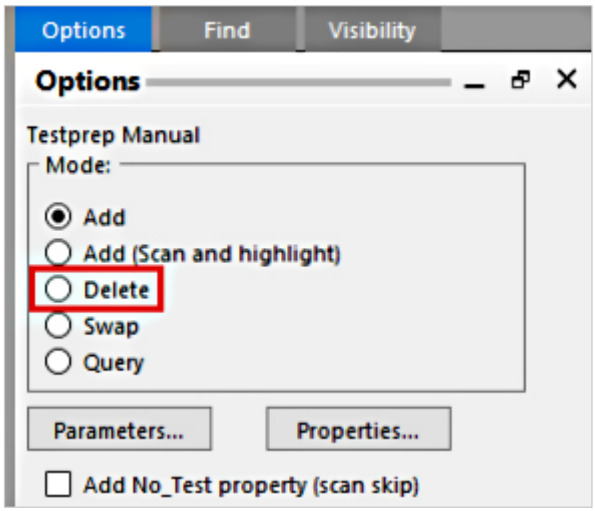
10 Create NC Drill File

This command is used to drill the test fixture. The test fixture holds pins that serve as a conductive interface between the pins on the board and the test bed. The command is located in **Manufacture > Testprep > Create NC drill data**.

11 FAQ

11.1 How to Delete Testpoints

Use **Manufacture > Testprep > Manual** and select **Delete** in the options window:



By selecting a testpoint you can delete a single testpoint. It's also possible to use area select to delete multiple testpoint at once.

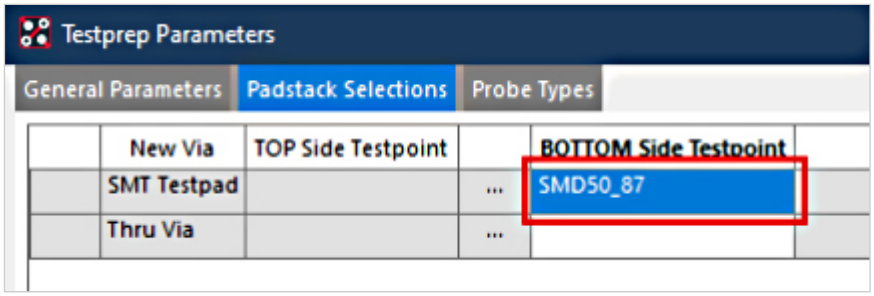
11.2 Use Testprep Together With Custom Testpoint

Synchronize Testprep is a FloWare module, that automates the testpoint assignment on dummy testpoint symbols, which have been defined in the schematic.

Closer information can be found in » FloWare Description, on page 144.

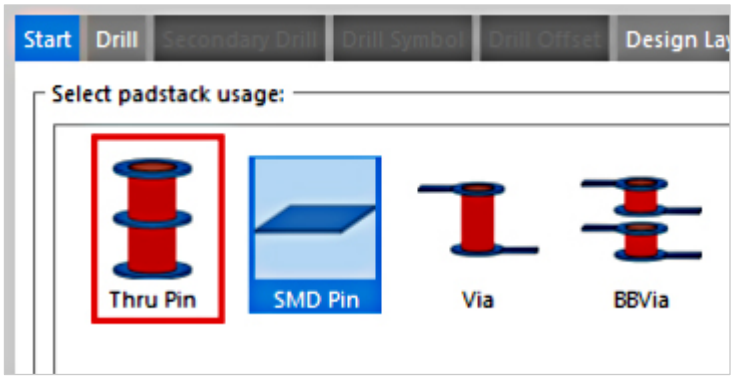
11.3 SMT Testpoint Bottom Pad Definition

Here you can see, how to create a SMT pad which can be used as a testpoint on Bottom side:

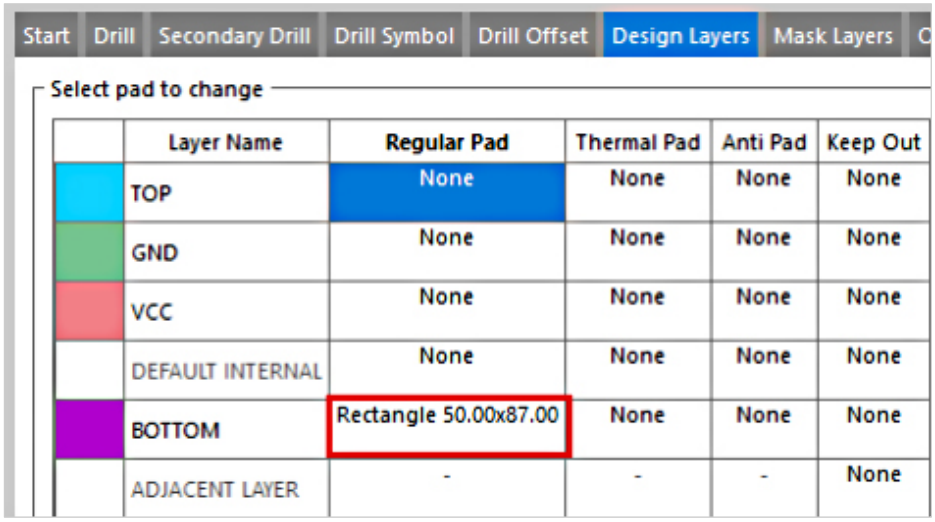


In the **Padstack Editor** follow these steps:

1. Switch Padstack usage from SMD Pin to **Thru Pin**:

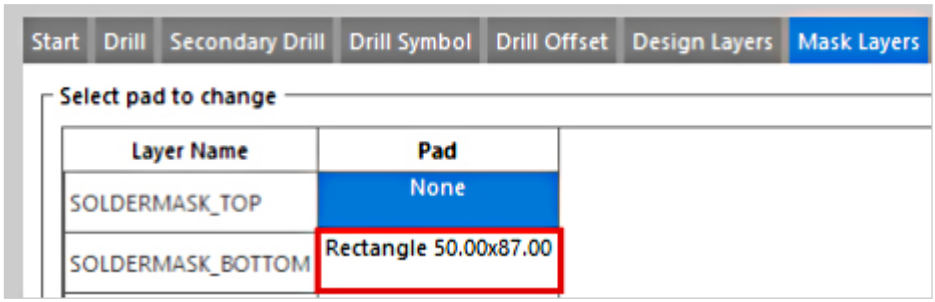


2. Define Pad on Bottom and delete pad on Top:



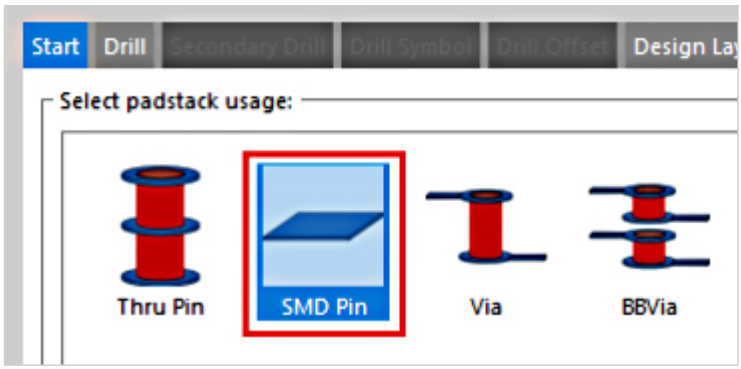
Layer Name	Regular Pad	Thermal Pad	Anti Pad	Keep Out
TOP	None	None	None	None
GND	None	None	None	None
VCC	None	None	None	None
DEFAULT INTERNAL	None	None	None	None
BOTTOM	Rectangle 50.00x87.00	None	None	None
ADJACENT LAYER	-	-	-	None

3. Define Pad on SOLDERMASK_BOTTOM:



Layer Name	Pad
SOLDERMASK_TOP	None
SOLDERMASK_BOTTOM	Rectangle 50.00x87.00

4. Switch Padstack back to SMD Pin:



5. Save Padstack.

11.4 What to Check if Testprep is Very Slow

In some cases, especially in large boards with many nets Testprep can be slow. If this problem occurs check following:

- Turn off **Auto Silk**, if enabled.
- Set a reasonable Test grid if the Design Grid is very small.
- Check the Max **Via displacement** value. If this value is very large, it slows down Testprep. Reduce this to a reasonable value.

11.5 Change the Text Size of the Testpoint Names

Use **Edit > Change** and define the desired text block size in the options Window. Afterwards you can select one testpoint text or you can select an area with the right mouse button on which the text size should be changed.