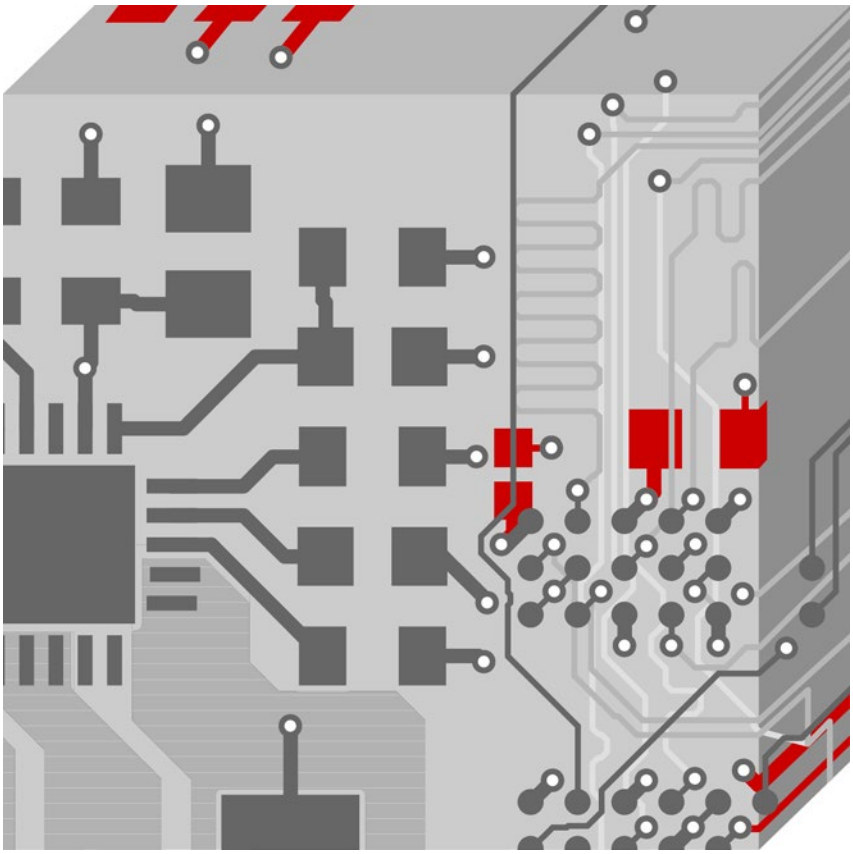
FlowCAD

Electrical Constraining Setup & Basics



Allegro PCB Editor with Performance Option

Application Note | V2.0

FlowCAD

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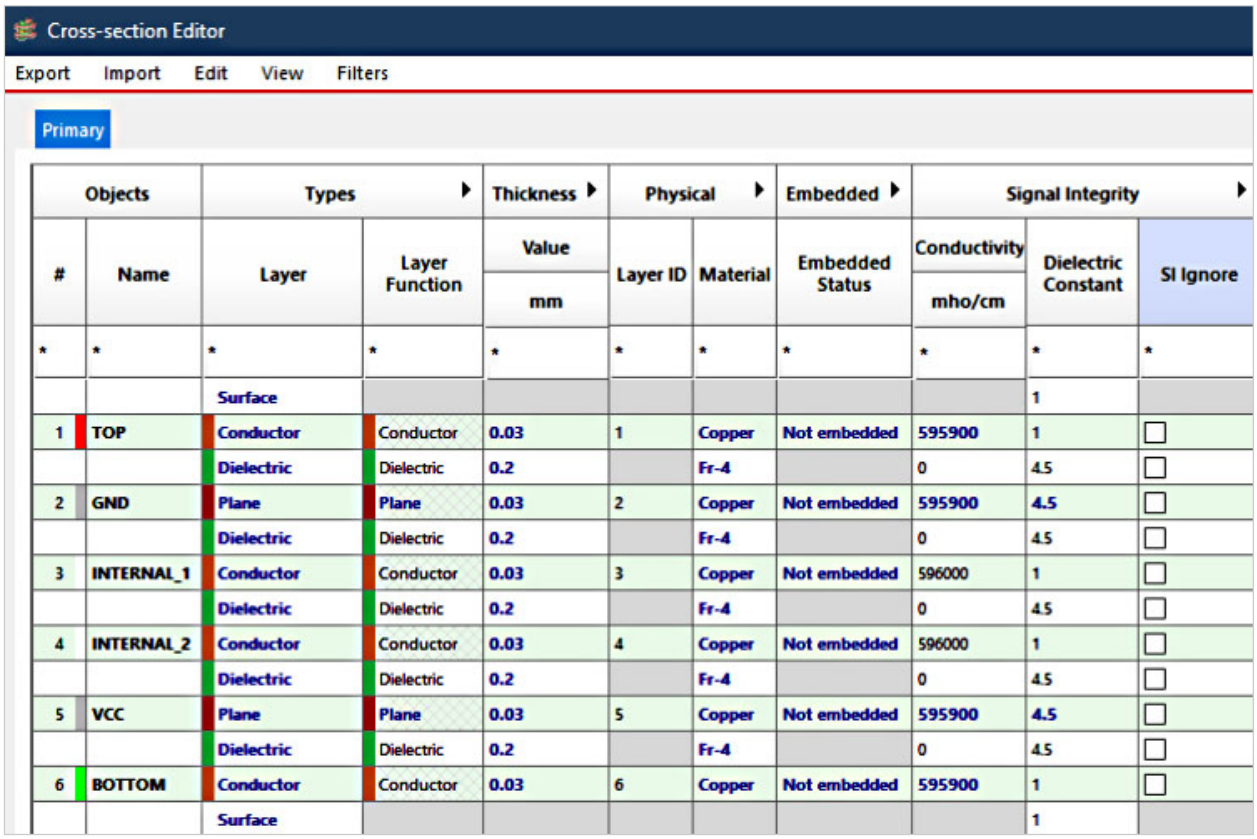
1 Cross Section

The definition of Cross Section is the first step if you want to work with electrical rules, cause e.g., for impedance calculation material and thickness is essential.

1.1 Cross Section Overview

The Cross Section Editor table is split into different sections for different thinks to be set up, like Thickness, Physical values, Embedding and so on.



Objects		Types		Thickness	Physical		Embedded	Signal Integrity		
#	Name	Layer	Layer Function	Value mm	Layer ID	Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore
*	*	*	*	*	*	*	*	*	*	*
		Surface							1	
1	TOP	Conductor	Conductor	0.03	1	Copper	Not embedded	595900	1	☐
		Dielectric	Dielectric	0.2		Fr-4		0	4.5	☐
2	GND	Plane	Plane	0.03	2	Copper	Not embedded	595900	4.5	☐
		Dielectric	Dielectric	0.2		Fr-4		0	4.5	☐
3	INTERNAL_1	Conductor	Conductor	0.03	3	Copper	Not embedded	596000	1	☐
		Dielectric	Dielectric	0.2		Fr-4		0	4.5	☐
4	INTERNAL_2	Conductor	Conductor	0.03	4	Copper	Not embedded	596000	1	☐
		Dielectric	Dielectric	0.2		Fr-4		0	4.5	☐
5	VCC	Plane	Plane	0.03	5	Copper	Not embedded	595900	4.5	☐
		Dielectric	Dielectric	0.2		Fr-4		0	4.5	☐
6	BOTTOM	Conductor	Conductor	0.03	6	Copper	Not embedded	595900	1	☐
		Surface							1	

In this document we'll concentrate on the parameter relevant for electrical constraining.

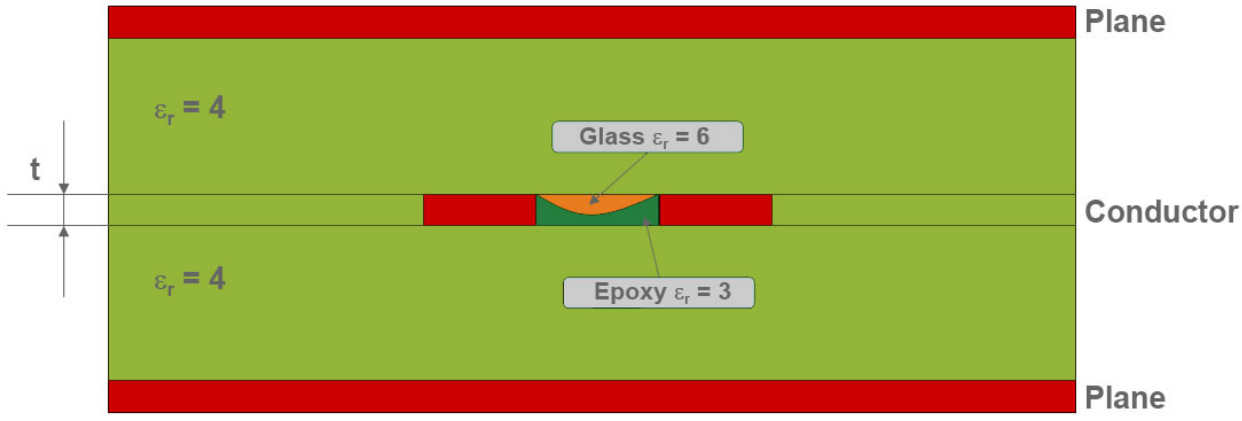
Parameter	Description
Type	The Type of the layer can be **Conductor** for signal layers, **Plane** for plane layers or **Dielectric** for non-electrical layers.
Material	Material of the layer. Material information is stored in the material.dat file. The default file is located in the installation in <cdsroot>share\pcb\text\materials. With **Setup > User Preferences > Paths > Config > materialpath** you can change this folder to use your own material.dat files.
Thickness	The Thickness is stored in material.dat file, but can be changed in the Cross Section.

Parameter	Description
Conductivity (mho/cm)	Conductivity is the specific value of the material. E_CONDUCTIVITY > 100,000 mhos/m = conductive (electrical) E_CONDUCTIVITY < 100,000 mhos/m = non-conductive (dielectric) Is also stored in material.dat but can be changed in the Cross Section.
Dielectric Constant	Dielectric Constant in ε_r of the material. Is also stored in material.dat, but can be changed in the Cross Section.
Width	The Width is used for Impedance calculation within the Cross Section Editor. The value is not automatically used in Constraint Manager.
Impedance	Single ended impedance of lines on the dedicated layer
Loss Tangent	Loss Tangent is the dielectric loss. The impedance value changes when you modify the Loss Tangent value. Is also stored in material.dat, but can be changed in the Cross Section.
Shield	Shield marks the reference layers as homogeneous planes for impedance calculation.
Freq. Dep. File	Frequency dependent material property file for the layer.
Etch Factor	Etch factor of the copper in degrees of arc. See **Chapter 1.6.2.**
Diff Coupling Type	Edge or Broadside coupling of differential pairs on the layer. Also enables differential impedance calculation.
Diff Spacing	Spacing of the members of a diffpair, used for impedance calculation.
Diff Z0	Differential Impedance of diff pairs on that layer.
SI Ignore	Ignores layer in SI simulation.

Note

We recommend using a material.dat file on Site level and putting in values for standard materials, e.g., for the different prepregs. This reduces effort and avoids errors setting up the stack-ups.

1.2 ε_r on Copper Layers



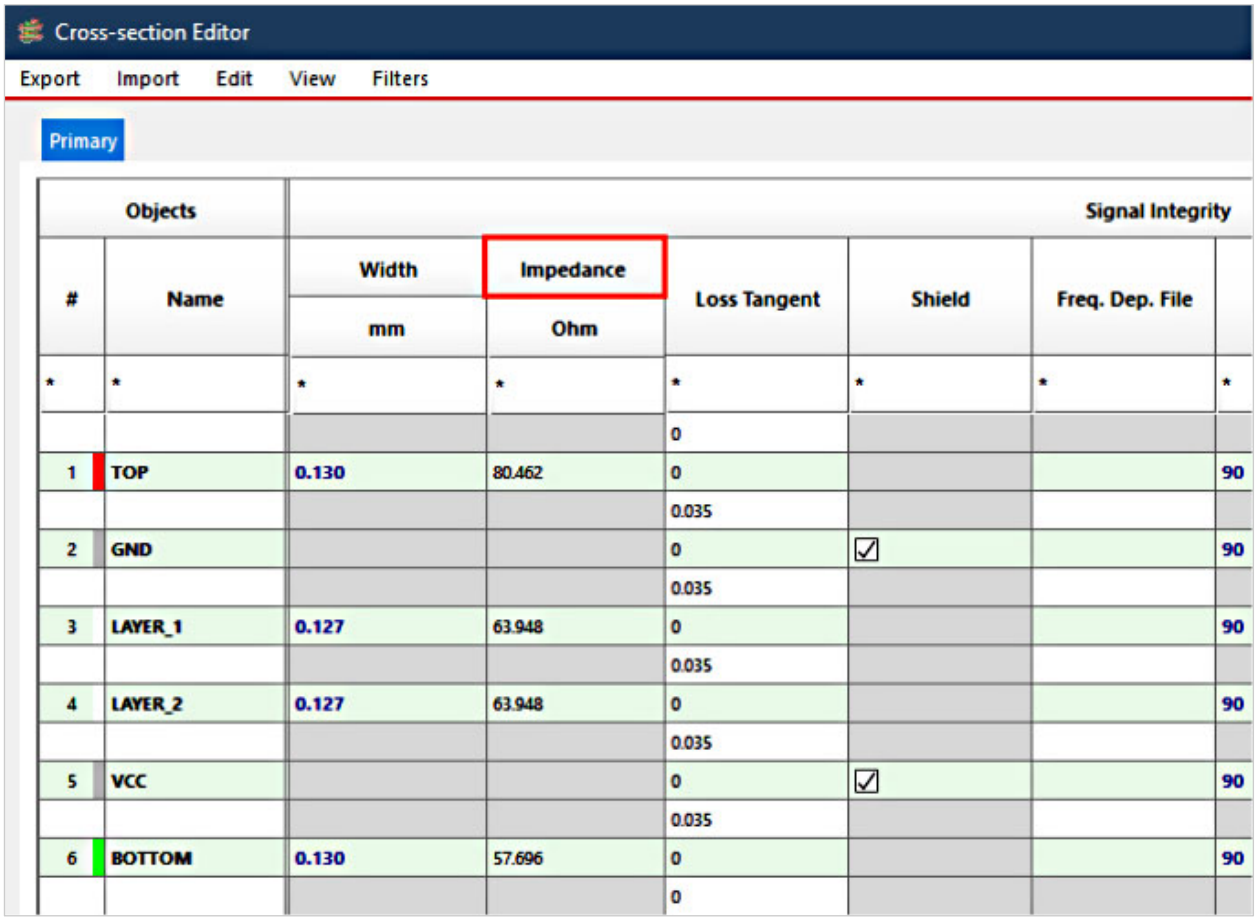
The value of ε_r on electrical layers is not for the copper. It's for the dielectric between the clines.

Prepregs and cores are made out of glass and resin. Both materials have different ε_r. After laminating the board, the distribution between the layers is homogeneous. The value for ε_r is 4 to 4.5. There are also glass and resin between the clines on the layers. If the spacing is large enough you also have a homogeneous distribution but when they are smaller you have more resin than glass in the spacings and the ε_r is different.

Normally you can use the same ε_r for electrical layers and dielectric. When the design is very critical, please talk to your PCB manufacturer to get the right values. They often have a good experience in creating the right values for impedance-controlled designs.

1.3 Single Ended Impedance

Using thickness and material values, the Cross section offers a calculation of the single ended impedance.



Objects		Signal Integrity					
#	Name	Width	Impedance	Loss Tangent	Shield	Freq. Dep. File	
		mm	Ohm				
*	*	*	*	*	*	*	*
				0			
1	TOP	0.130	80.462	0			90
				0.035			
2	GND			0	☑		90
				0.035			
3	LAYER_1	0.127	63.948	0			90
				0.035			
4	LAYER_2	0.127	63.948	0			90
				0.035			
5	VCC			0	☑		90
				0.035			
6	BOTTOM	0.130	57.696	0			90
				0			

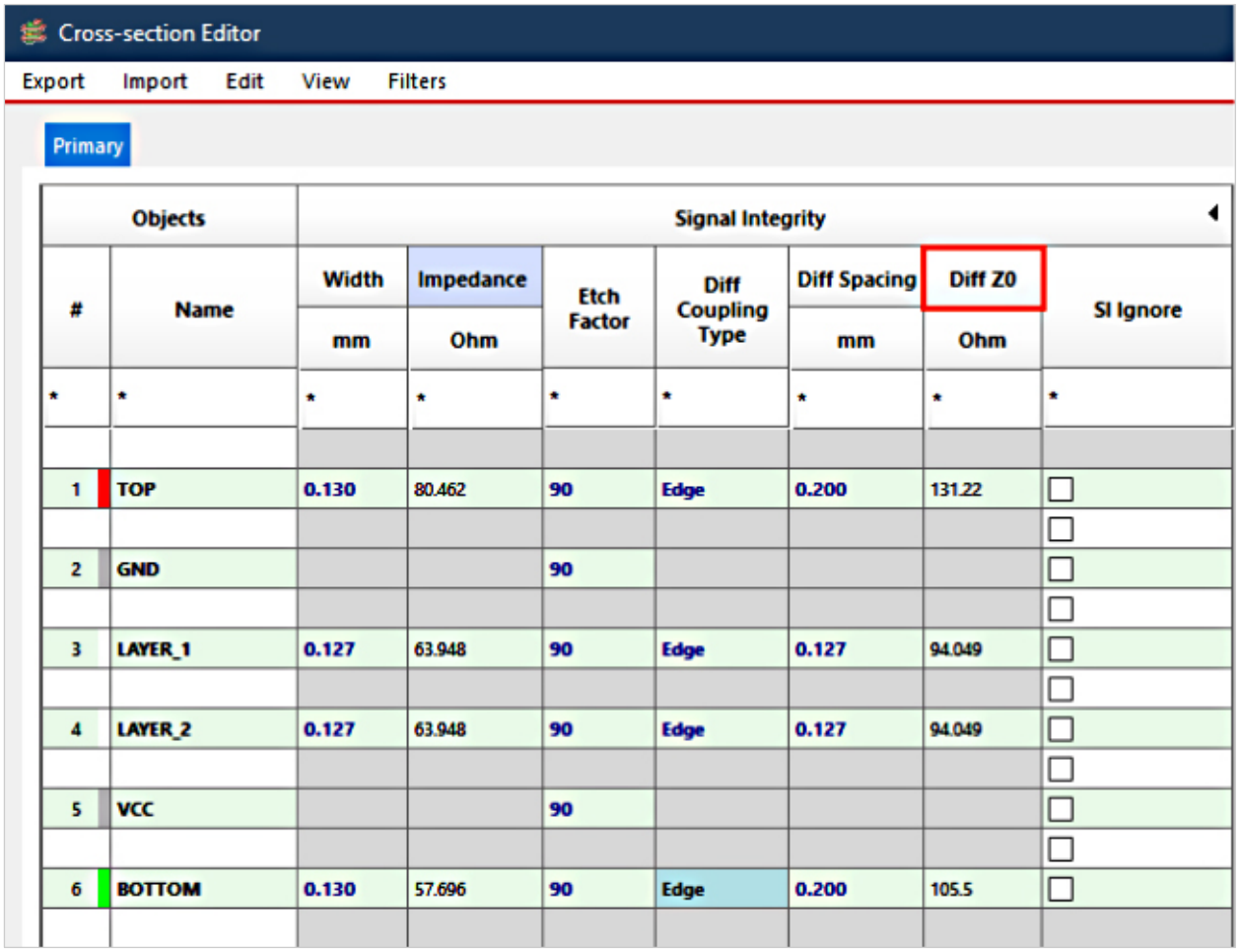
Changing impedance will recalculate the line width, which is required to achive the impedance and vice versa.

Note

This is only for calculation purpose. Values are not automaticllay taken over into the Constraint Manager.

1.4 Differential Impedance

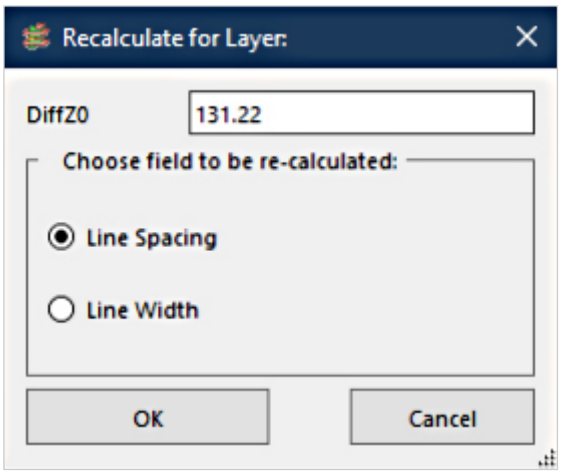
As well as single ended impedance, it is also possible to calculate differential impedance:



Objects		Signal Integrity						
#	Name	Width	Impedance	Etch Factor	Diff Coupling Type	Diff Spacing	Diff Z0	SI Ignore
		mm	Ohm			mm	Ohm	
*	*	*	*	*	*	*	*	*
1	TOP	0.130	80.462	90	Edge	0.200	131.22	☐
2	GND			90				☐
3	LAYER_1	0.127	63.948	90	Edge	0.127	94.049	☐
4	LAYER_2	0.127	63.948	90	Edge	0.127	94.049	☐
5	VCC			90				☐
6	BOTTOM	0.130	57.696	90	Edge	0.200	105.5	☐

To enable differential impedance calculation, the Diff Coupling Type has to be selected.

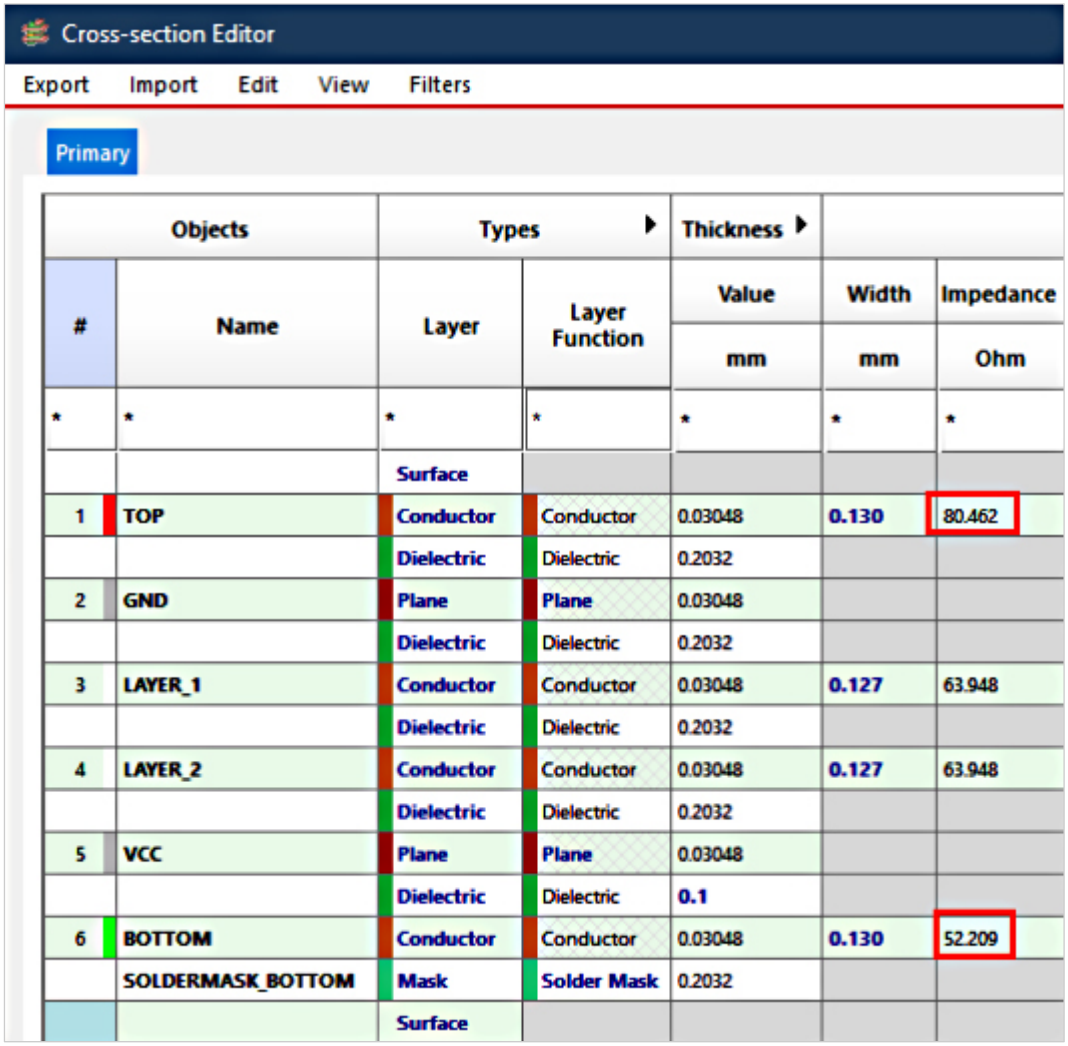
When Width or Diff Spacing are changed the differential impedance (Diff Z0) will be recalculated.



When the impedance is changed, a selection, whether Line Spacing or Line Width should be recalculated comes up.

1.5 Solder Resist

On inner layer the solder resist has no influence on the impedance. But the influence on the outer layer can be quite high.



Objects		Types		Thickness		
#	Name	Layer	Layer Function	Value	Width	Impedance
				mm	mm	Ohm
*	*	*	*	*	*	*
		Surface				
1	TOP	Conductor	Conductor	0.03048	0.130	80.462
		Dielectric	Dielectric	0.2032		
2	GND	Plane	Plane	0.03048		
		Dielectric	Dielectric	0.2032		
3	LAYER_1	Conductor	Conductor	0.03048	0.127	63.948
		Dielectric	Dielectric	0.2032		
4	LAYER_2	Conductor	Conductor	0.03048	0.127	63.948
		Dielectric	Dielectric	0.2032		
5	VCC	Plane	Plane	0.03048		
		Dielectric	Dielectric	0.1		
6	BOTTOM	Conductor	Conductor	0.03048	0.130	52.209
	SOLDERMASK_BOTTOM	Mask	Solder Mask	0.2032		
		Surface				

In this example only the Bottom side of the PCB has solder resist.

Resulting impedance is 80 Ω on Top versus 52 Ω on Bottom.

1.6 Imprint and Etch Factor

Imprint and Etch Factor have an impact on impedance calculation.

Cross-section Editor

Export Import Edit View Filters

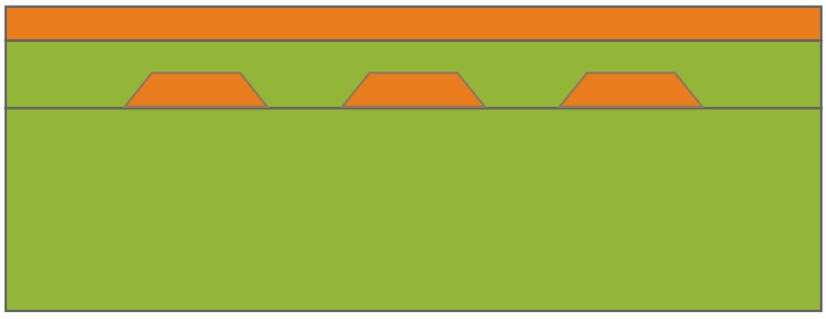
Primary

Objects		Thickness		Signal Integrity	
#	Name	Value mm	Etch Factor	Diff Coupling Type	Diff Spacing mm
*	*	*	*	*	*
1	TOP	0.03048	90	None	
		0.2032			
2	GND	0.03048	90		

Please check for realistic values with your PCB manufacturer.

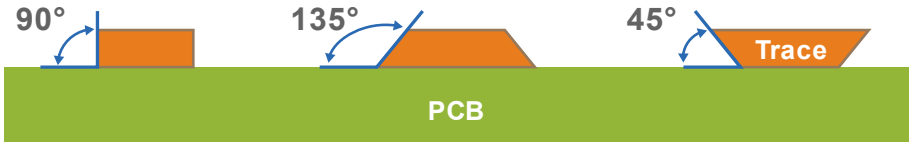
1.6.1 Imprint

Copper is pressed into the soft prepreg, therefore for the impedance calculation, the FR4 height above the transmission line in pressed condition is relevant, not the initial thickness of the prepreg.



1.6.2 Etch Factor

Also, the Etch Factor has an impact on single ended as well as differential impedance values.



2 Transmission Line Styles

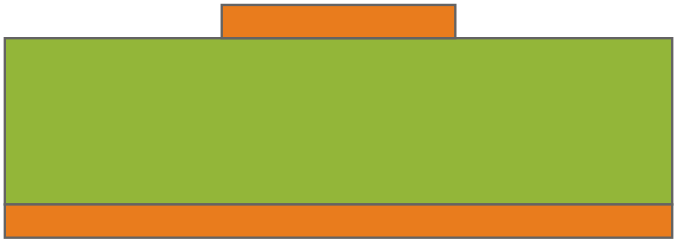
In this chapter the different configurations of transmission line are listed as an overview.

2.1 Microstrip Transmission Lines

Microstrip transmission lines are lines with one referencing plane layer. On outer layer you normally have microstrip lines.

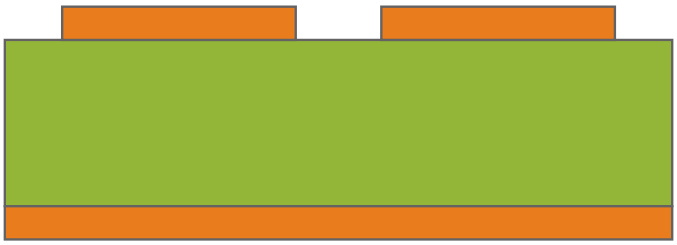
2.1.1 Surface

Surface lines are on an outer layer without resist.



2.1.2 Surface Differential

Surface differential lines are differential pairs on outer layer without resist.

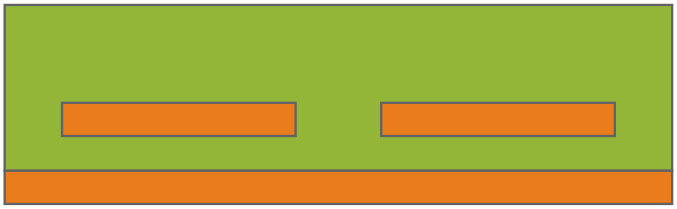


2.1.3 Embedded

Embedded lines can be on outer layers with resist or inner layers.

2.1.4 Embedded Differential

Embedded differential lines are differential pairs on outer layers with resist or inner layers.

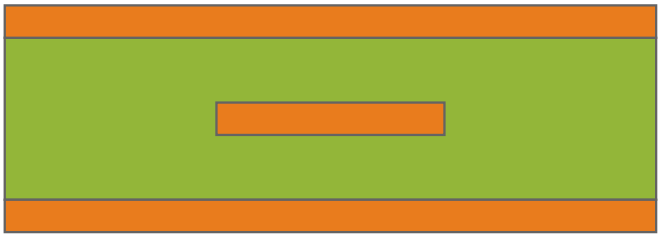


2.2 Stripline Transmission Lines

Stripline transmission lines are lines with two referencing plane layers. Stripline are possible only on inner layer.

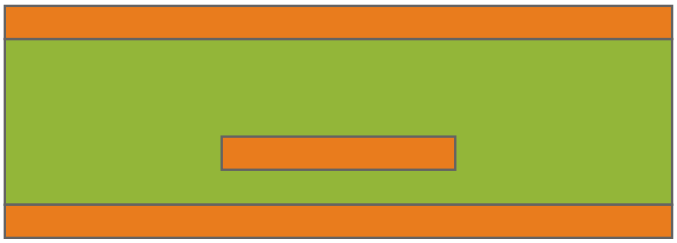
2.2.1 Balanced

Balanced striplines are in the middle of two plane layers.



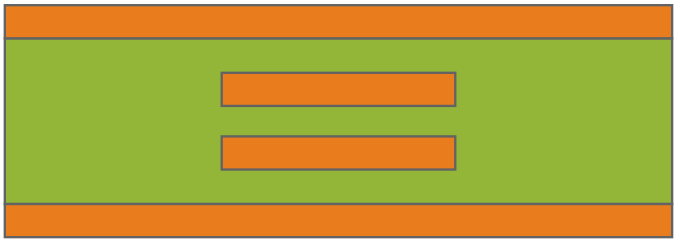
2.2.2 Unbalanced

Unbalanced striplines are out of the middle of two plane layers.



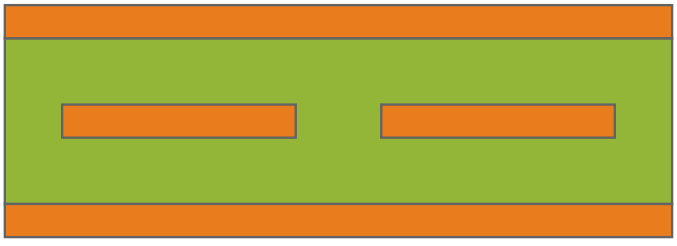
2.2.3 Broadside Coupled Differential Stripline

Broadside coupled differential striplines are differential pairs which are routed on two different layers.



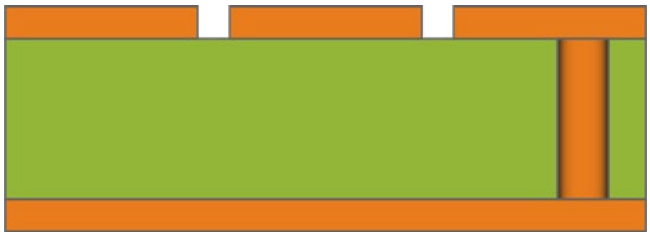
2.2.4 Edge Coupled Differential Stripline

Edge coupled differential striplines are differential pairs which are routed on one layer.

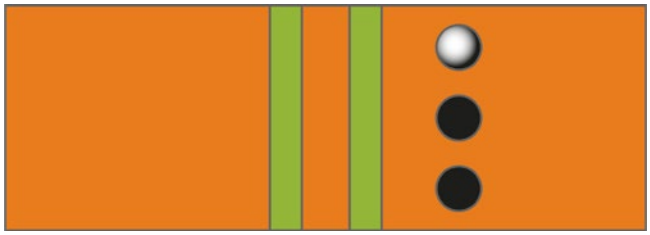


2.3 Coplanar Transmission Line

Coplanar lines are shielded by copper planes on the same layer. The edge of the planes is often stitched with via to a referencing plane layer.

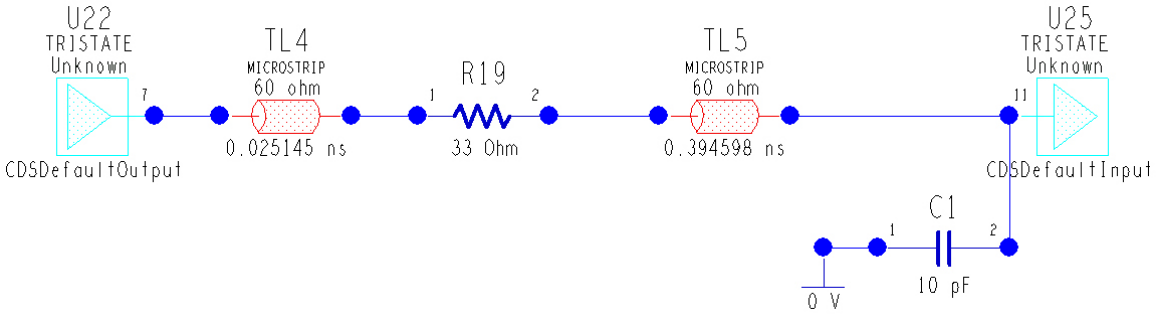


Top view

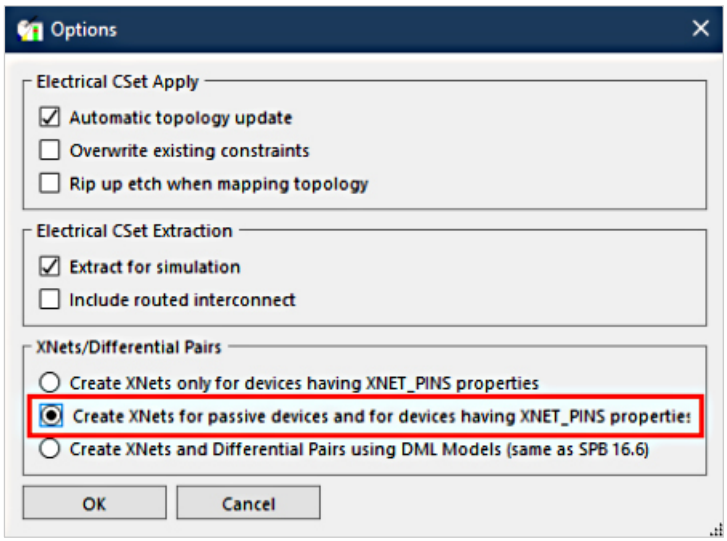


3 DC-Nets and Voltage Property

Setting up DC nets is necessary for correct definition of Xnet.



By default, Xnet are automatically created by the tool through passive devices and devices having **XNET_PINS** property.

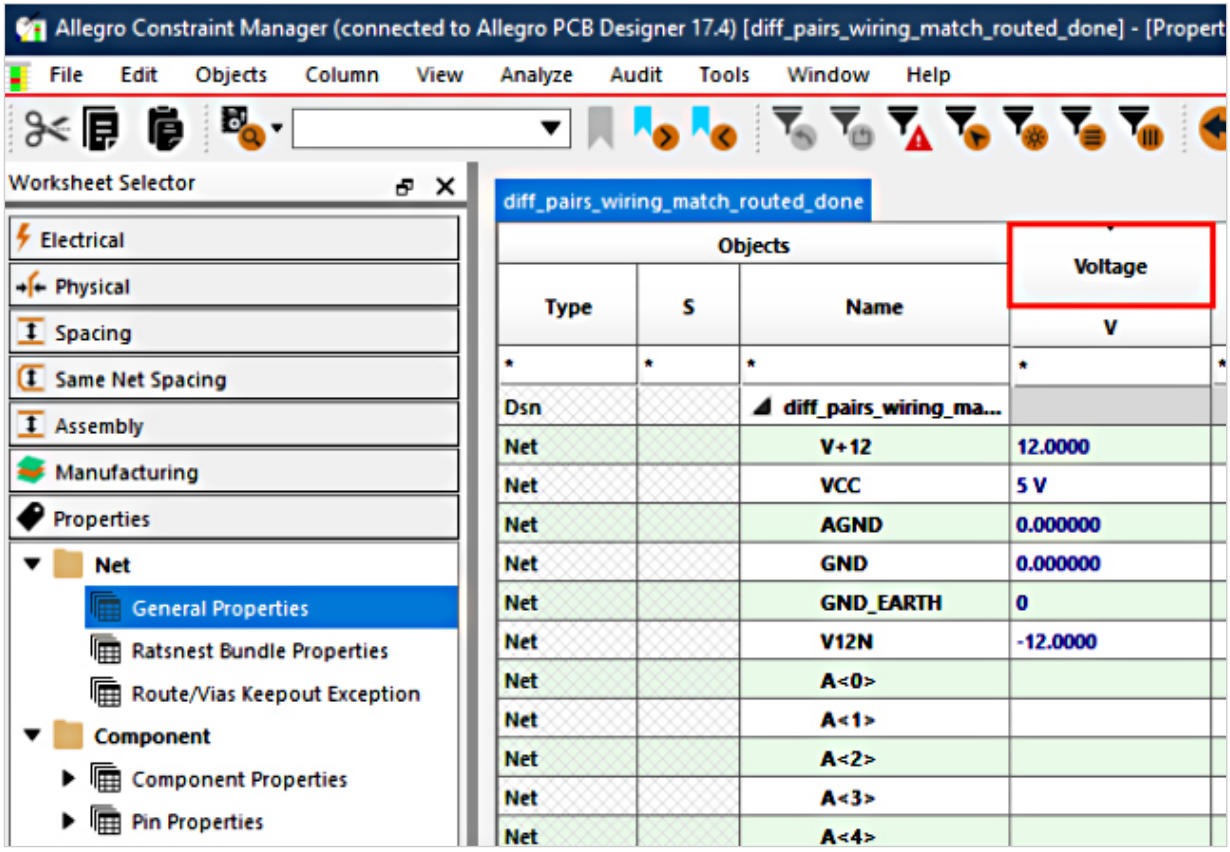


In the example, an XNet would be generated through C1 to the gnd net. The voltage property (0V) on the gnd net prevents the Xnet generation through C1.

3.1 Defining a Voltage Property

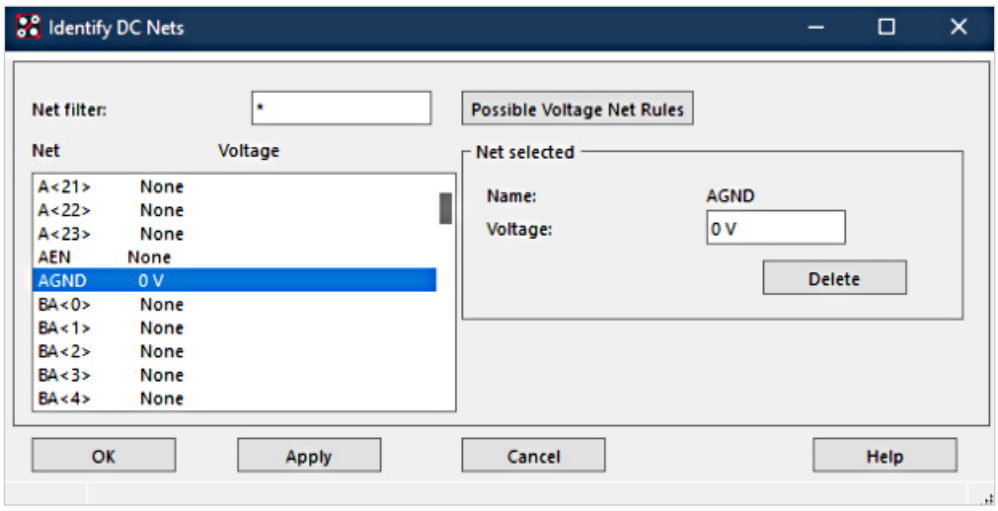
There are different ways to set the voltage property.

Easiest way it to define voltage property in the Properties section of the Constraint Manager.



Here it does not make any difference, whether the Constraint Manager is startet out of the schematic entry or PCB Editor.

Other possibility inside of the PCB Editor is to use **Logic > Identify DC Nets**.



4 Component Classes

The component classes are important for XNet generation. XNets are generated through components with property **CLASS = DISCRETE.**

Class- and Pinuse-Property

CLASS	Devices	Refdes	PINUSE
IC	Active digital components	IC*	IN, OUT, BIDIR, OCA, OCL, …
DISCRETE	Passive	R*, L*, C*	UNSPEC
IO	Connectors	X*	UNSPEC

For passive components (R, L and C) always use:

CLASS = DISCRETE and PINUSE = UNSPEC

For active components:

CLASS = IC and PINUSE according to datasheet

Recommendation

CLASS and PINUSE should be defined in the library.

5 Electrical Constraints

This chapter gives an overview of the different worksheets of the electrical domain of the Constraint Manager. More detailed description can be found in the Cadence documentation and additional app notes.

5.1 Wiring

In different to low-speed design for high-speed design the routing topology or wiring plays a major role, because it has to be guarantied, that signal reach the receivers at a dedicated point in time and order.

Following values can be defined within the Wiring worksheet:

- Stub length
  Maximal length of a stub, e.g., pin a escape
- Exposed Length
  Maximal length on outer layer, above plane layer, where the signal is not shielded
- Parallel
  Max Parallel constraint is used to prevent nets from running parallel for long stretches to control crosstalk
- Layer Sets
  Routing only on dedicated layers

5.2 Vias

In the Vias worksheet the number of the vias within the signal routing can be controlled. Target is, that all signale e.g., of a bus are routed in the same fashion.

It is possible to define the maximal number of vias to be used or that all routing traces should have the same number of vias.

In addition, it is also possible to define, what via structures have to be used.

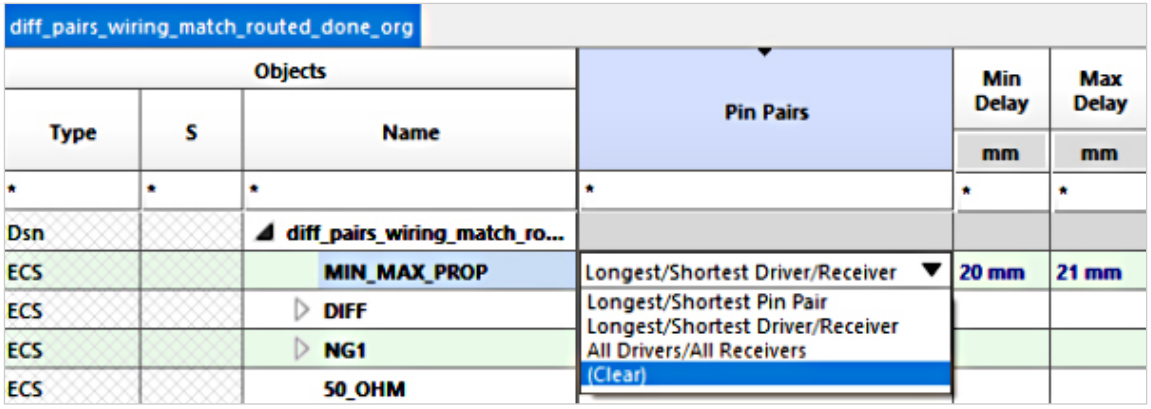
5.3 Impedance

In the Impedance worksheet, it is possible to define the target single ended impedance for signals and also the tolerance. By this, the line width is automatically set to the right values during routing.

5.4 Min. / Max. Propagation Delay

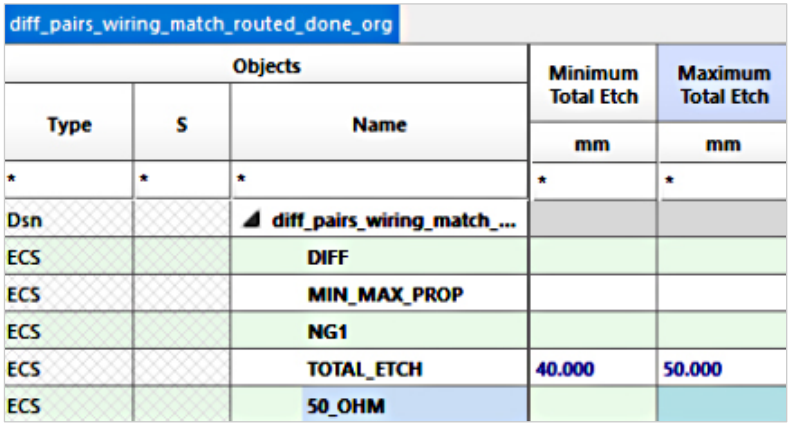
Within the Min. / Max. Propagation Delay worksheet it is possible to set the minimum / maximum delay from driver to receiver.

Here it is possible to set whether the longest / shortest pin pair, the longest / shortest Driver / Receiver pair or all driver / all receiver should be taken into account.



5.5 Total Etch Length

Total Etch length can only control the complete routing length of a net.



For critical high-speed nets controling of complete routing length is not sufficient. Total Etch Length should only be used for uncritical net to avoid they might be routed to long.

5.6 Differential Pairs

In the Differential Pairs Worksheet all parameters for differential routing can be defined.

» Have a look at FlowCAD App Note Differential Pairs.

5.7 Relativ Propagation Delay

Relativ Propagation Delay is used to guarantee, that e.g., all signal of a bus arrives at the receivers at the same point in time.

diff_pairs_wiring_match_routed_done_org

Objects			Pin Pairs	Pin Delay		Scope	Relative Delay				Length	Delay
Type	S	Name		Pin 1	Pin 2		Delta:Tolerance	Actual	Margin	+/-		
				mm	mm		mm				mm	ns
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		diff_pairs_wiring_match_routed_...							0.033 mm			
MGrp		GROUP1(8)							0.033 mm			
MGrp		GROUP2(16)	All Drivers/All R...			Glo...	:1 mm		0.396 mm			
PPr		IO<0>.T.1:U26.37 [IO<0>]				Glo...	0 mm:1 mm	0.604 mm	0.396 mm	-	21.712	0.12379
PPr		IO<0>.T.1:U27.37 [IO<0>]				Glo...	0 mm:1 mm	TARGET			22.316	0.12941
PPr		IO<1>.T.1:U26.38 [IO<1>]				Glo...	0 mm:1 mm	0.596 mm	0.404 mm	-	21.720	0.12383
PPr		IO<1>.T.1:U27.38 [IO<1>]				Glo...	0 mm:1 mm	0.028 mm	0.972 mm	-	22.288	0.12926
PPr		IO<2>.T.1:U26.40 [IO<2>]				Glo...	0 mm:1 mm	0.184 mm	0.816 mm	-	22.133	0.12619
PPr		IO<2>.T.1:U27.40 [IO<2>]				Glo...	0 mm:1 mm	0.364 mm	0.636 mm	+	22.680	0.13151
PPr		IO<3>.T.1:U26.41 [IO<3>]				Glo...	0 mm:1 mm	0.251 mm	0.749 mm	+	22.567	0.12866
PPr		IO<3>.T.1:U27.41 [IO<3>]				Glo...	0 mm:1 mm	0.356 mm	0.644 mm	+	22.672	0.13147
PPr		IO<4>.T.1:U26.43 [IO<4>]				Glo...	0 mm:1 mm	0.263 mm	0.737 mm	-	22.053	0.12573
PPr		IO<4>.T.1:U27.43 [IO<4>]				Glo...	0 mm:1 mm	0.355 mm	0.645 mm	+	22.671	0.13144
PPr		IO<5>.T.1:U26.44 [IO<5>]				Glo...	0 mm:1 mm	0.536 mm	0.464 mm	-	21.780	0.12418
PPr		IO<5>.T.1:U27.44 [IO<5>]				Glo...	0 mm:1 mm	0.193 mm	0.807 mm	+	22.510	0.13052
PPr		IO<6>.T.1:U26.46 [IO<6>]				Glo...	0 mm:1 mm	0.428 mm	0.572 mm	-	21.889	0.1248
PPr		IO<6>.T.1:U27.46 [IO<6>]				Glo...	0 mm:1 mm	0.059 mm	0.941 mm	-	22.257	0.12904
PPr		IO<7>.T.1:U26.47 [IO<7>]				Glo...	0 mm:1 mm	0.159 mm	0.841 mm	-	22.157	0.12633
PPr		IO<7>.T.1:U27.47 [IO<7>]				Glo...	0 mm:1 mm	0.146 mm	0.854 mm	-	22.170	0.12854

There are three different ways to define relative propagation delay:

- Same length without Target:
  - Delta / Tolerance Format: **: 5mm**
  - All lines have to have the same lengt, within a tolerance (in this example 5mm).
- Same length with Target:
  - Delta / Tolerance Format: **0mm : 5mm**
  - All lines have to have the length of the target within a tolerance (in this example 5mm).
- Length in relation to Target:
  - Format: 20mm : 5mm
  - All lines have to have the same length as the target with an offset. Offset: 20mm

In addition, the Scope is important, since it defines whether all pin pairs must meet rule or just the once within one XNet.

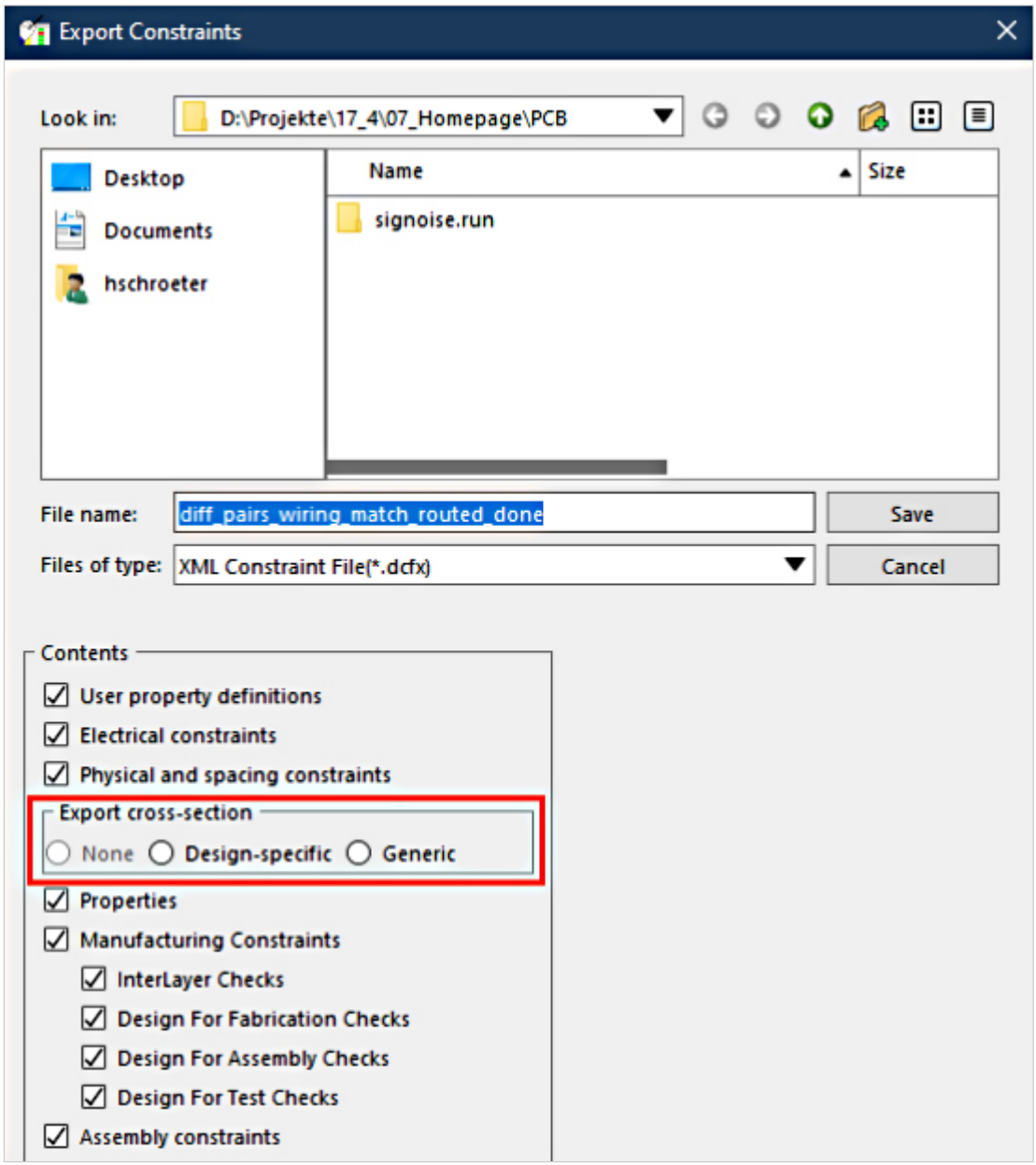
- Global: All pin pairs must meet rule
- Local: Only pin pairs within one XNet must meet rule

6 Reusing Constraints

By importing and exporting constraints it is possible to reuse constraints in different boards and build up a constraint's library.

6.1 Export Contraints

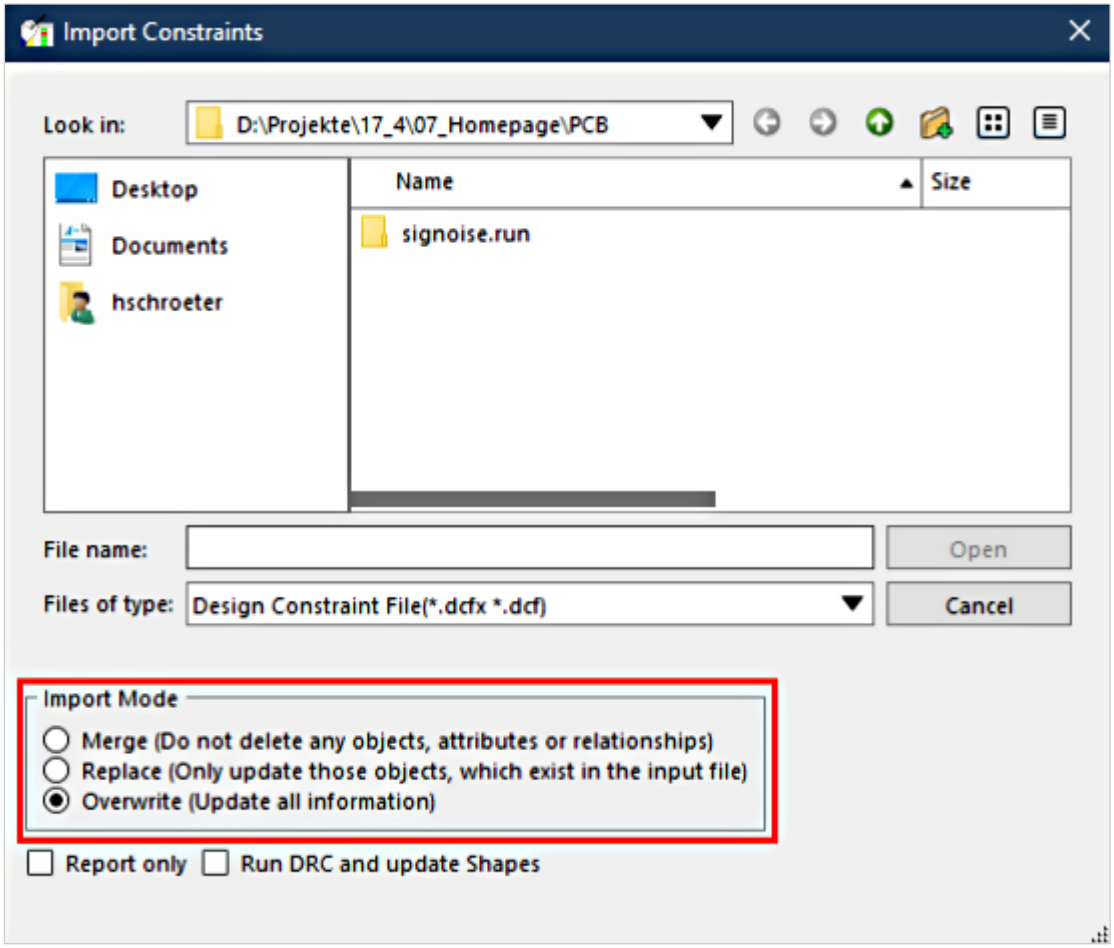
During export by **File > Export > Constraints** in the Constraint Manager, it is possible to decide, whether the cross section is also exported and design specitic constraints are created.



Other possibility is to create genetirc constraint files, which can be used in any stackup.

6.2 Importing Constraints

Constraints can be imported into the Constraint Manager by **File > Import > Constraints**. While importing it is possible to decide how constraints are handled.



In the Import Mode following setting can be used:

- Merge
  - The merge constraints option preserves data in the design and reads in new data from the constraint file.
  - If a constraint exists in design, but not in constraint file, it remains unchanged.
  - If a constraint exists in design and also in constraint file, constraint file overwrites design.
- Replace
  - Only update those objects, which exist in the constraint file.
  - If an object in the design is constrained but the object in the constraint file is not, Constraint Manger removes the constraints from the design.
  - If a constraint exists in design and also in constraint file, constraint file overwrites design.
- Overwrite
  - Clears all exsiting constraints and objects.
  - And adds everything defined in the constraint file.

Examples

Source Design

Constraints

Objects			Referenced Electrical CSet	Single-line Impedance			
Type	S	Name		Target	Tolerance	Actual	Margin
				Ohm	Ohm	Ohm	Ohm
*	*	*	*	*	*	*	*
Dsn		Constraints					
DPr		DP1	DIFF_PAIR_SET				
Net		NET_1	DIFF_PAIR_SET				
Net		NET_2	DIFF_PAIR_SET				
Net		NET_3	50OHM	50	2 %		
Net		NET_4					

DP1 of NET_1 and NET_2 constraint with DIFF_PAIR_SET

NET_3 constraint with 50OHM Set

NET_4 without constraints

Target Design

empty

Objects			Referenced Electrical CSet	Single-line Impedance			
Type	S	Name		Target	Tolerance	Actual	Margin
				Ohm	Ohm	Ohm	Ohm
*	*	*	*	*	*	*	*
Dsn		empty					
Net		NET_1					
Net		NET_2					
Net		NET_3					
Net		NET_4	60OHM	60	2 %		

Before importing constraints, only NET_4 is constraint with 60OHM Set.

Target design after importing constraints using Merge

empty

Objects			Referenced Electrical CSet	Single-line Impedance			
Type	S	Name		Target	Tolerance	Actual	Margin
				Ohm	Ohm	Ohm	Ohm
*	*	*	*	*	*	*	*
Dsn		empty					
DPr		DP1	DIFF_PAIR_SET				
Net		NET_1	DIFF_PAIR_SET				
Net		NET_2	DIFF_PAIR_SET				
Net		NET_3	50OHM	50	2 %		
Net		NET_4	60OHM	60	2 %		

DP1 of NET_1 and NET_2 generated and constraint with DIFF_PAIR_SET

NET_3 gets constraint with 50OHM Set

NET_4 remains unchanged

Target design after importing constraints using Replace

empty

Objects			Referenced Electrical CSet	Single-line Impedance			
Type	S	Name		Target	Tolerance	Actual	Margin
				Ohm	Ohm	Ohm	Ohm
*	*	*	*	*	*	*	*
Dsn		empty					
DPr		DP1	DIFF_PAIR_SET				
Net		NET_3	50OHM	50	2 %		
Net		NET_4					

DP1 of NET_1 and NET_2 generated and constraint with DIFF_PAIR_SET

NET_3 gets constraint with 50OHM Set

60OHM constraint set is removed from NET_4