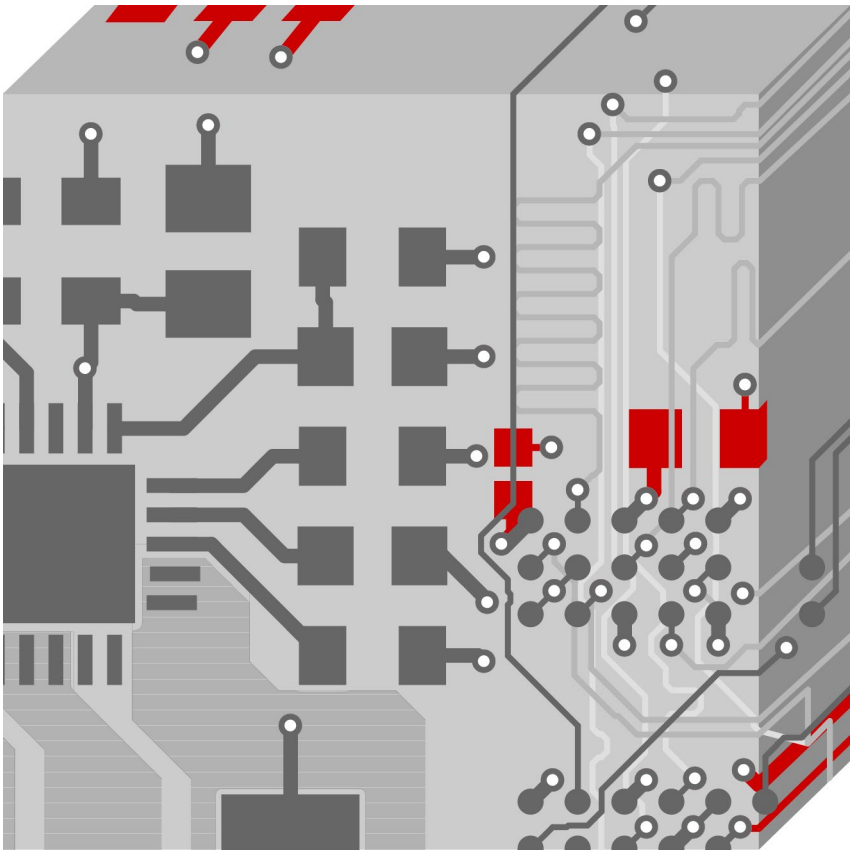
FlowCAD

Layer Cross Section Etch Factor



OrCAD / Allegro PCB Editor

Application Note | V1.1

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1 Definition of Layer Cross Section Etch Factor

The Layout Cross Section dialog box includes an **Etch Factor** column to account for manufacturing process variations, such as when a copper trace is routed within in a trapezoid rather than within a rectangle.

As shown in **Figure 1**, the Etch Factor column displays the default setting (90 degrees), for each conductor and plane layer in your design. To change the default, you simply enter a new value in the field on the appropriate row. To maintain viable angles, values are restricted to within 45 degrees of vertical, thus between 45 to135 degrees or between 225 to 315 degrees.

Primary

Objects		Signal Integrity						
#	Name	Dielectric Constant	Width mil	Impedance Ohm	Loss Tangent	Shield	Freq. Dep. File	Etch Factor
*	*	*	*	*	*	*	*	*
		1			0			
1	TOP	1	5.00	58.654	0			90
		3.95			0			
2	GND2	3.95			0	☑		90
		3.95			0.035			
3	INT3	3.95	5.00	46.138	0			90
		3.95			0			
4	INT4	3.95	5.00	46.138	0			90
		3.95			0.035			
5	VCC5	3.95			0	☑		90
		3.95			0.035			
6	BOTTOM	1	5.00	58.654	0			90
		1			0			

Figure 1: Layer Cross Section

You can set a different degree of angle for every cline on a specific conductor / plane layer.

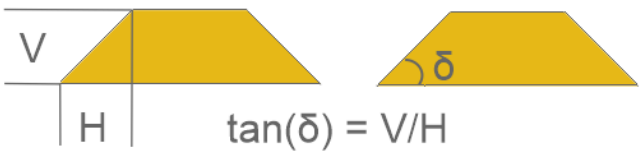


Figure 2: Etch Factor Calculation

These trapezoids can be upright or inverted, depending on the layer and the process used.

Figure 3 shows the relationship between the angle used to represent the deviation of the trace-to-trace geometry and the range of values used to represent various orientations.

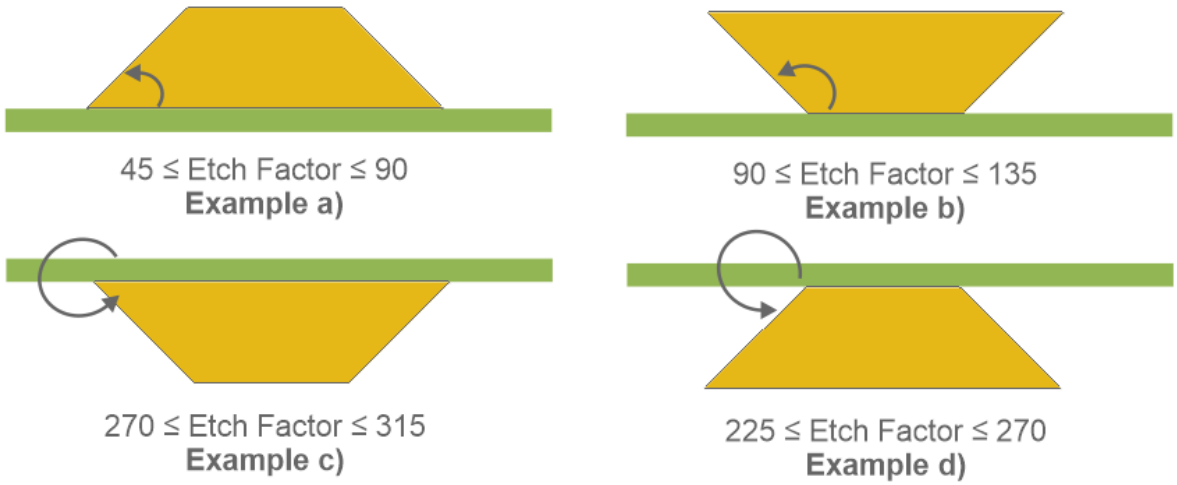
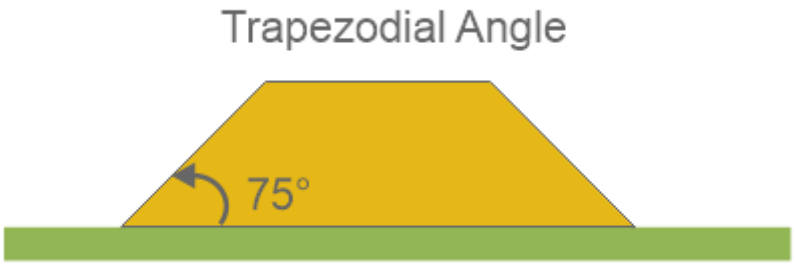


Figure 3: Trace Geometry Variations

2 Example

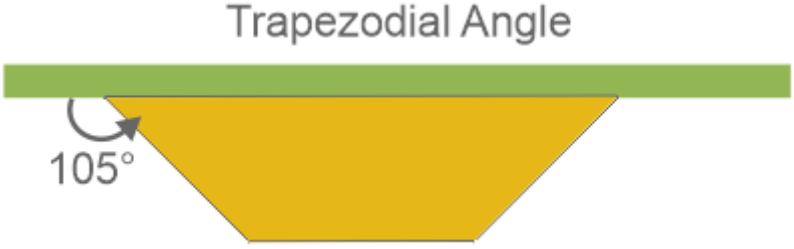
As an **example**, in the following stack-up, the top-layer trapezoidal angle is 75 degrees. When the top-layer routed trace trapezoidal angle is less than 90 degrees, what will be the bottom-layer routed trace trapezoidal angle to get the same impedance?



What will be the bottom-layer trapezoidal angle?

Solution

At the bottom layer, we have to consider the following situation, because at the bottom, the trace is upside down.



Currently, if you want the trace on the bottom layer to have the same impedance as that on the top layer, the angle of the bottom layer should be in alignment to **Figure 3 example c): "180 + (180 minus top-layer angle)**, which equals to: 180 degrees + (180 -75) degrees = 180 degrees + 105 degrees = **285 degrees.**

#	Name	Layer	Width mil	Impedance Ohm	Shield	Etch Factor
*	*	*	*	*	*	*
		Surface				
1	TOP	Conductor	5.00	61.699	45 ≤ Etch Factor ≤ 90 Example a)	75
		Dielectric				
2	GND2	Plane			☑	90
		Dielectric				
3	INT3	Conductor	5.00	51.58	270 ≤ Etch Factor ≤ 315 Example c)	285
		Dielectric				
4	INT4	Conductor	5.00	51.58	45 ≤ Etch Factor ≤ 90 Example a)	75
		Dielectric				
5	VCC5	Plane			☑	90
		Dielectric				
6	BOTTOM	Conductor	5.00	61.699	270 ≤ Etch Factor ≤ 315 Example c)	285
		Surface				

Figure 4: Allegro PCB Layer Stackup Calculations