

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingsprache ist deutsch, falls nicht anders angekündigt.

Allegro Design Reuse

Description

This is an Engineer Explorer class that is designed around more advanced topics and exploration of the tool. This course does not teach basic tool operations. Please see Course Prerequisites.

Design Reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse.

Any EDA user who has time-to-market pressures will benefit from Design Reuse. Design Reuse adds scalability and modularity to your design process, saving time and reducing error by facilitating the reuse of known good IP.

Learning Objectives:

- Create a subdesign state file
- Create a layout module file
- Document and store the reuse design
- Use properties to control reuse packaging
- Work around hierarchical constraint limits
- Make changes to subdesigns while in reuse
- Customize packaging with Occurrence Edit
- Use macros and parameters
- Search for related solutions on SourceLink.

Audience

- Engineering Managers
- PCB Designers
- Design Engineers

Prerequisites

The student must have completed the following before taking this class:

- Allegro Design Entry HDL Front to Back Flow_

Course Agenda

- Getting Started
- Creating a Reuseable Block
- Reusing the Block in Other Designs
- Managing Changes
- Advanced Topics