TRAINING

FlowCAD

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Allegro PCB SI630 MGHz Signal Design

Overview

Description

This is an Engineer Explorer class that is designed around more advanced topics and exploration of the tool. This course does not teach basic tool operations. We require that students who are not actively using the tool first complete either the Allegro PCB SI Foundations course or the Allegro Design Entry SI course.

This training material is intended to bring users up to speed on the technical aspects of Allegro PCB SI 630 MGH Signal Design.

Recent advances in silicon technology and high-speed communications have introduced buffers with data rates in the multi-Gigabit range. Simulation models need to be modeled for buffers and vias to enable accurate simulation results in this frequency range.

With the 15.2 software release, Cadence Design Systems has introduced an approach to modeling and simulating these very high-speed structures. Using MacroModels you can build buffer models that accurately operate in the multi-Gigabit range. Additionally, new algorithms have been developed to more accurately model vias. Among the new algorithms is a Scattering Parameters (S-Parameter) model for the vias. The behavior of this type of model can be accurately characterized over a wide frequency range.

You can also use S-Parameters to model your channel interconnect from one board to another, thus facilitating the simulation of the complete serial channel through a backplane to its destination. The new Channel Analysis functionality allows you to design a channel such that the eye pattern seen at the receiver meets its requirements for eye opening and jitter.

This training will cover all of this functionality.

Learning Objectives:

- Use MacroModels for MGH applications
- Create via models using the new Via Model Generator
- Generate S-Parameter models and perform simulation analysis using these models
- Perform Channel Analysis to quickly run large data bit simulations and optimize your channel.

Audience

- Electrical Engineers
- Digital IC Designers
- Design Engineers

This course is for electrical engineers whose design responsibilities include PCB signal analysis and designers who are concerned with the problems associated with high-speed designs.

Software

You need either the Allegro PCB SI 610 series product version 15.2 software OR the Allegro PCB SI 630 series product version 15.2 software.

The Channel Analysis functionality does not come with the standard software release. It is packaged as an overlay that you install after you have installed the Allegro PCB SI 630 series product version 15.2 software. The overlay is available from SourceLink.

Prerequisites

Allegro Design Entry HDL SI
Allegro PCB SI Foundations 610

Additionally, the student should be familiar with the following:

- Basic understanding of the UNIX and Windows operating systems and commands
- Familiarity with digital/analog circuit design methodologies
- Working knowledge of printed circuit board design and signal analysis (some SPICE simulation processes; characteristics of electro-magnetic theory; transmission line theory)

Course Agenda

- Using a MacroModel in SigXplorer
- MacroModel for Pre/De-emphasis
- Backplane Via Stub Models
- Backplane Via S-Parameter models
- High-Capacity Simulation using Channel Analysis
- Pre-Emphasis Optimization using Channel Analysis
- Data Rate What-Ifs Designs using Channel Analysis