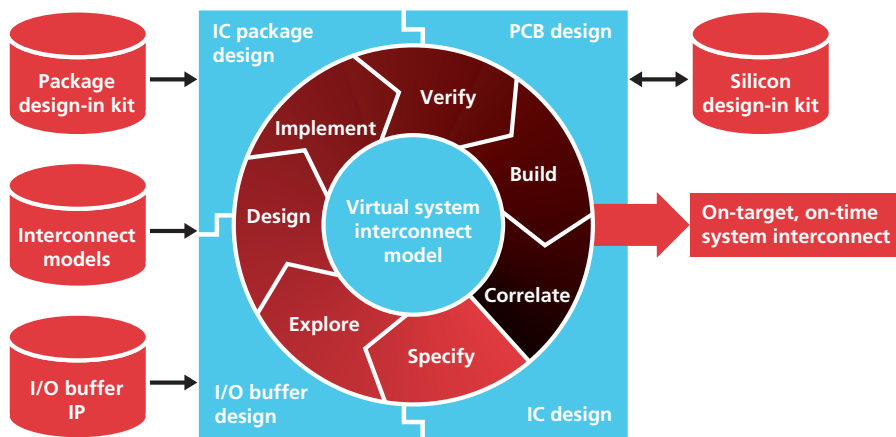


ALLEGRO SILICON DESIGN-IN KITS

Cadence® Allegro® silicon design-in kits are part of the Allegro system interconnect design platform’s co-design solution. Working within the Allegro PCB SI design and analysis environment, the design-in kits allow PCB designers direct use of accurate transceiver models earlier in the design cycle, saving time and money. IC manufacturers can help shorten their customers’ time to design for new, complex silicon devices by providing an executable version of their design guides in the form of high-speed design-in kits.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect — between I/O buffers and across ICs, packages, and PCBs — to eliminate hardware re-spins, decrease costs, and reduce design cycles. The Allegro constraint-driven flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With silicon design-in kits, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter™ and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

STREAMLINE IC IMPLEMENTATION IN PCB SYSTEMS

Time-to-volume production for IC manufacturers depends on quick adoption of new devices by systems companies. But differing design environments, complex I/O structures, and multigigabit-speed data rates all conspire to make new device simulation and implementation into a PCB system a complex and expensive process.

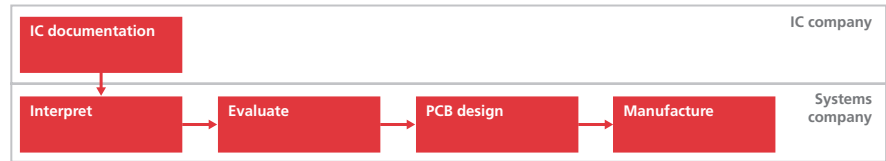
Innovative silicon design-in kits from Cadence tackle these issues. Using technology available in the Allegro PCB SI design and analysis environment, IC manufacturers can develop and distribute design-in kits that PCB designers can use to implement new silicon devices into system products. A design-in kit instantly increases a PCB designer's productivity. It also allows engineers to develop and use optimal constraints to drive PCB floorplanning, routing, and verification processes. Using silicon design-in kits, systems companies and IC manufacturers save an average of eight to ten weeks, depending on design complexity.

ALLEGRO PCB SI SILICON DESIGN-IN KITS

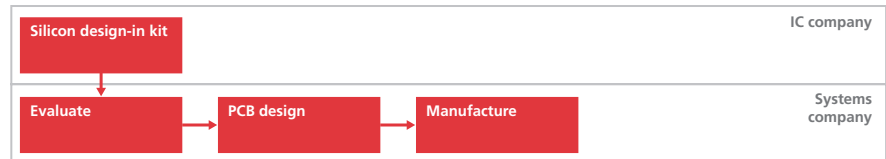
Allegro silicon design-in kits act as electronic blueprints for the implementation of silicon in a system. They leverage system design work normally accomplished during the IC design process and allow IC producers to share design intent with PCB designers via electronic plug-and-play modules, in which constraints are well defined. Depending on the IC manufacturer's specifications, the contents may vary, but high-speed silicon design-in kits generally contain the following:

- Ready-to-simulate system-level topologies for typical use of the device on the board/system
- Verified I/O buffer models
- Large package model
- Testbench and correlation data
- Connector models for backplane applications

DESIGN-IN KITS ACCELERATE DESIGN START TIME



Traditional design process for designing-in complex devices with high-speed digital I/Os



High-speed design-in kits shave weeks or months off of your design cycle

- Constraints embedded into reference design to enable constraint-driven placement and routing of the device on the PCB system
- Device-specific scripts and tools to evaluate simulation results
- Tutorial movies that describe how to get started with the design kit in the end user's environment

CREATING A SILICON DESIGN-IN KIT

Design-in kits leverage system design work normally performed during the IC design process. They provide electronic files to systems companies, allowing them to work concurrently to prepare products during the final stages of IC development. In this way, systems are ready earlier and both IC manufacturers and systems companies achieve volume production sooner.

Most systems companies expect their IC vendors to provide input/output buffer information specification (IBIS) models for new devices. To do this, IC engineers have to translate SPICE (silicon) models into IBIS (behavioral) models, which is a manual and time-consuming process. Since many multigigabit transceivers cannot be modeled accurately with IBIS, systems companies have recently been asking IC vendors to provide models in alternative formats. The Allegro PCB SI design and analysis environment

provides the direct use of both IBIS and alternative formats (silicon-level SPICE, DML MacroModels), enabling the simulation of devices containing multigigabit transceivers. The rich modeling options of Allegro PCB SI allow for quick and efficient creation of design-in kits.

CADENCE SILICON DESIGN CHAIN INITIATIVE

The Cadence Silicon Design Chain® initiative collaborates with other industry leaders to provide optimized solutions that help IC manufacturers and systems companies accelerate their time to volume. Using a silicon-ready approach, we validate the processes and flows necessary for first-time silicon success at advanced technology nodes.

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or a value-added reseller (VAR) in your area, visit www.cadence.com/contact_us.