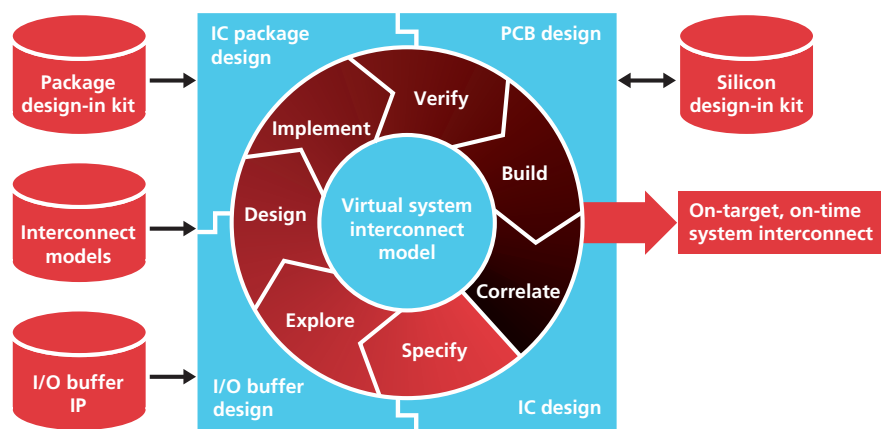


ALLEGRO PACKAGE DESIGNER 610/620

Cadence® Allegro® Package Designer 610 and Allegro Package Designer 620—600 series products within the Allegro system interconnect design platform take IC package and IC package co-design to the next level. They combine new chip-level co-design capabilities for I/O feasibility planning with industry-leading IC package design tools to deliver a co-design methodology for Cadence First Encounter®. An embedded 3D field solver also enables full package-level simulation models that can help PCB designer design-in new devices faster and more accurately.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The Allegro constraint-driven flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With silicon design-in kits, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter™ and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

SEAMLESS CO-DESIGN FLOW BETWEEN IC AND PACKAGE

The existing serial design methodology between IC and package design can no longer meet the cost, performance and time-to-market pressures of today's complex, leading-edge devices. Electrical and physical feasibility studies and chip/package design trade-offs must take place early in the design phase, before implementation decisions are made and options become limited. During this stage it is crucial to consider the impact of physical design choices on the electrical performance of the IC, and vice versa. Once the chip design has progressed to the point at which driver optimization can no longer take place, the burden falls on the package designer to meet the requirements, which may not always be possible. Enabling a true co-design methodology, through the use and exchange of IC abstracts, allows designers to make simultaneous physical and electrical design trade-offs to ensure that the IC meets its performance and cost objectives in the shortest time possible.

ALLEGRO PACKAGE DESIGNER 610

Allegro Package Designer 610 — a 600 series product within the Allegro system interconnect design platform— provides a unique IC packaging design environment. Allegro Package Designer 610 is a complete constraint-driven physical design solution targeted at single fixed/static die designs. It supports all packaging methods, including PGA, BGA, micro-BGA, chip scale using both flip-chip and wirebond die attach methods. It simplifies and speeds the design process—from direct data entry from IC tools to full documentation with automatic design features.

COMPREHENSIVE, CONSTRAINT-DRIVEN PHYSICAL LAYOUT

Allegro Package Designer 610 includes all the functionality and features you need to design today's advanced packages. It supports all packaging methods, including PGA, BGA, micro-BGA, chip scale, as well as flip-chip and wirebond attach methods. Full online design-rule checking supports the complex, unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multiple cavities, complex shapes, and interactive and automatic wirebonding are all supported. The easy-to-use Design Wizard within Allegro Package Designer 610 walks you through each task and automates the process of creating the building blocks of an IC/package, such as the creation of die, package, plating bars, and power/ground rings. The die and BGA wizards automate definition of these library elements with your choice of text file standard formats (such as D.I.E., Excel, and AIF2), or a form-driven user interface, such as the BGA Wizard.

SOPHISTICATED SUBSTRATE MODELING AND RULE CHECKING

A key advantage of Allegro Package Designer 610 is its ability to verify design accuracy against a complete set of physical and electrical design rules (constraints). Physical constraints are physical design guidelines, established in a user-defined technology file, that ensure manufacturability. Electrical constraints are signal delay and distortion specifications for critical nets. Allegro Package Designer 610 dynamically checks the design against these constraints throughout the design process to ensure the design is meeting manufacturing and electrical specifications, and it provides immediate feedback to the designer by way of DRC markers.

DESIGN REUSE FOR INCREASED EFFICIENCIES

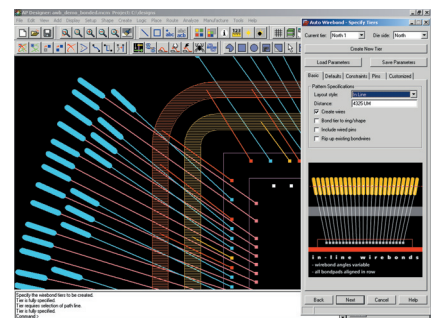
Allegro Package Designer 610 captures both substrate stack-up and constraint information in a technology file, which can then be reused for other designs of similar structure, further

reducing cycle time on future designs. Substrate suppliers can provide techfiles that will typically contain critical design rules to help drive a correct design methodology. Multiple techfiles can be used from different suppliers to assure manufacturability at secondary suppliers.

TOOL FLEXIBILITY FOR WIREBOND FINGER AND FLIP-CHIP ESCAPE PATTERNS

If the design uses wirebond interconnects, the bond finger patterns will vary from in-line or inline radial to multi-tiered, arc-based patterns, depending on package technology and density of chip I/Os. Stacked-die configurations may require the interweaving of bond fingers, resulting in extremely complex patterns. Allegro Package Designer 610 can automatically create the appropriate pattern based on specific, user-defined constraints. These may include:

- Bond finger dimension
- Bond finger, wire, and route spacing
- Minimum and maximum wire length and crossing rules
- Maximum bond wire angle (only for radial)
- Number of rows in stagger or shelves, if applicable

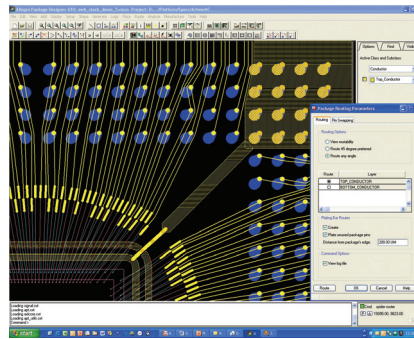


New wirebonding capability delivers a robust set of wirebond rules and enhanced features to address the unique requirements for stacked die

Alternatively, Allegro Package Designer 610 can automatically calculate the best pattern based on more general design criteria. Once created, design requirements may dictate that these patterns be modified. For this, Allegro Package Designer 610 provides you with a powerful wirebond editing environment that offers great flexibility in modifying the patterns while still adhering to the established design rules. For flip-chip technology, Allegro Package Designer 610 provides a robust set of tools to assist the user in creating the complex routing escape patterns found in today's high-density interconnect (HDI) designs. HDI or micro-via technology dictate that these complex via escape patterns be specifically constructed to meet manufacturing requirements. Allegro Package Designer 610 includes both automatic and semi-automatic tools to help speed up this process. The automatic tools quickly create all combinations of blind and buried via patterns that are then available in a library. A semi-automatic complex via structure tool provides a mechanism for creating the intricate via and route escape patterns often found in HDI designs, and quickly propagates them around the die.

AUTO AND MANUAL OPTIMIZATION OF CHIP-TO-PACKAGE INTERCONNECTS PROVIDE FLEXIBILITY READING NETLISTS IN MULTIPLE FORMATS

The "netlist-less" design philosophy available in Allegro Package Designer 610 lets you optimize the chip-to-package interconnect without a predefined netlist. If routability and delay drive chip-to-package connectivity, use automatic and interactive assignment utilities to achieve optimal results. The interactive assignment utility allows you to create new nets, assign specific pins, delete pins, or delete nets. If a plating bar exists, you can also build the package I/O to plating bar connectivity. If a netlist does exist, you don't have to worry about its format. The netlist Text Wizard reads virtually any ASCII file. Allegro Package Designer 610



Spiderroute offers 45-degree or true any-angle routing and routability analysis that is ideal for wirebond attach substrates.

can import AIF2 or LEF/DEF files as well. If you need to distribute power and ground through "rings," use the power/ground Ring Wizard to generate the conductor shape automatically. If you've created your die flag in another tool such as AutoCAD, then you can use the DXF interface to import the geometry. Once in Allegro Package Designer 610, you can then assign the proper voltage to the die flag.

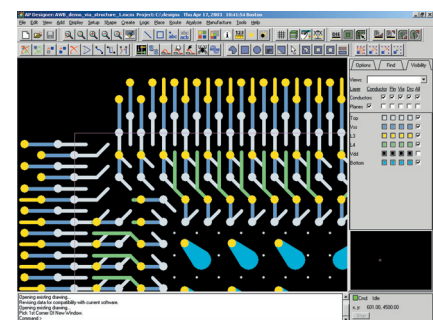
Spiderroute offers 45-degree or true any-angle routing and routability analysis that is ideal for wirebond attach substrates.

ALLEGRO PCB ROUTER 610 AND SPIDERROUTE FOR INTERACTIVE OR AUTOMATIC RULES-BASED ROUTING

The most important and time consuming step in any design is routing. By their very nature, complex IC packages are a routing challenge. Whether it's an all-angle, single-layer, wirebonded design with a plating bar, or a flipchip on a multilayer build-up substrate, each technology presents its own unique set of challenges. Allegro Package Designer 610 overcomes this problem by providing the designer with a toolbox of routing functionality — from interactive to automatic. For dynamic interactive routing, Allegro Package Designer 610 has the most powerful set of interactive routing tools available today. Allegro Package Designer 610 enables fast and accurate routing of any type of IC package design—from all-angle wirebonded to orthogonal flip-chip. Any electrically

constrained nets, such as those with controlled impedance and matched delay, are easily routed to those constraints with dynamic feedback when rule violations occur. Two new features in Allegro Package Designer 610 are tandem differential pair routing and the ability to dynamically plow/heal through power and ground planes. In addition to the interactive tools, Allegro Package Designer 610 also provides automatic routing capability and includes two routers: Allegro PCB Router 610 and SpiderRoute. Depending on the interconnect technology of your design—wirebond or flip-chip—you can choose which router is more appropriate. For multilayer flip-chip designs, which typically have a large amount of electrically constrained nets, Allegro PCB Router 610 is a powerful shape based router that can manage these complex design challenges. For all-angle, wirebonded designs, which can be extremely dense and require a different set of routing algorithms, SpiderRoute is the right choice. SpiderRoute is a schedule-based router that evaluates available routing channels and optimizes routing based on spacing rules. SpiderRoute automatically creates and sends orthogonal routes out to the plating bar.

Complex HDI breakout via patterns can be defined, stored and re-used as array patterns.



Complex HDI breakout via patterns can be defined, stored and re-used as array patterns

REAL-TIME ANALYSIS ENSURES ELECTRICAL INTEGRITY

Beyond innovative packaging and routing facilities, what really sets Allegro Package Designer 610 apart is its ability to ensure electrical integrity by performing real-time analysis. You can do this in two ways:

- Dynamic RLC displays line parasitic data in real time as you enter traces, reflecting resistance, inductance, and capacitance
- Check the design against electrical design constraints for crosstalk thresholds, delay, and line impedance

EXTENSIVE MANUFACTURING OUTPUT CAPABILITIES

This total solution's philosophy demands as much attention to outputs as to internal capabilities. Allegro

Package Designer 610 can generate all the types of manufacturing data likely to be required—from documentation to tooling. You can easily create bond diagrams, dimension documents, format drawings, and various output files containing critical package data. Manufacturing output supports Gerber 4X00 and 6X00 series, 274X, Barco, DXF, AIF2, and GDSII.

Many of today's foundries already use Allegro Package Designer 610. This means you can send an Allegro design database to the foundry directly as manufacturing input, greatly compressing throughput times and preempting potential inaccuracies. The foundry can use the database to enhance manufacturing yields and implement any last-minute changes to the package without inadvertently compromising the original specifications. (Contact your foundry to confirm their specific capabilities.)

PCB SYSTEM-LEVEL HAND-OFF

Allegro Package Designer 610 not only bridges the gap between silicon and package design but also links package and circuit board design, automatically generating all data required for PCB-level floorplanning and layout:

- Physical footprint
- Schematic symbol
- Device models in SPICE, IBIS, or Allegro PCB SI format

These capabilities compress set-up time and increase data accuracy for systems designers.

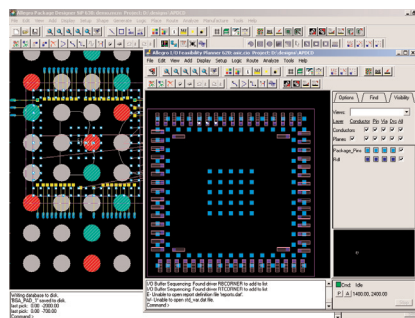
ADDITIONAL FEATURES

Allegro Package Designer 610 is truly a total packaging solution, addressing the full design flow from end-to-end. Additional features include:

- Integration with silicon design
- Full UNIX/Windows interoperability
- Free web-downloadable viewer
- Special routing for "dog-bone" fanout vias, with or without tangent fillet, for both chip and package
- "Auto smoothing" of traces to any angle, diagonal, or arc
- Dynamic pad filleting
- Online, dynamic RLC parasitic calculation
- Design reuse features for utilizing prior designs with new ICs
- GDSII, DXF, Gerber, and IDF bi-directional data transfer
- Full database compatibility with Allegro Package Designer 620 and Allegro Package SI 620

ALLEGRO PACKAGE DESIGNER 620

Allegro Package Designer 620 builds on the solid fixed-die substrate design foundation established by Allegro Package Designer 610 and extends package design to include IC/Package co-design. The 620 product also comes with an embedded 3D model generation engine that allows



IC die abstracts can be imported into the I/O Feasibility Planner for substrate-level optimization of the bump matrix, or created from scratch and handed off to the IC design team

designers to extract a full package model that can then be used for post-layout verification in the Allegro Package SI 620 simulation environment.

Allegro Package Designer 620 provides new chip-level I/O planning capabilities, it contains functionalities targeted at streamlining the ECO flow between IC and package design. Based on the LEF/DEF or OpenAccess 2.2 protocols—the standard formats for IC data exchange—Allegro Package Designer 620 includes a robust set of import/export capabilities, enabling IC and package designers to send die abstract changes back and forth robustly in order to reduce design time and realize an optimized IC die pad-ring/bump matrix and package substrate.

BENEFITS

- Die abstract and package substrate co-design reduces package complexity and optimizes substrate performance and cost
- Robust bi-directional die-abstract ECO exchange with Encounter platform via LEF/DEF and OA2.2
- Allows users to determine best package and substrate technology early in the IC design cycle

- Enables users to create accurate 3D package models for system level simulation
- Supports a full package-driven design flow, from design capture through manufacturing output, with all the industry standards

FEATURES

NEW DIE ABSTRACT EDITOR

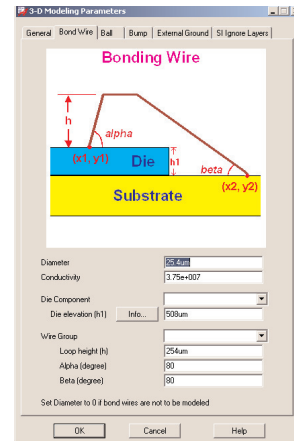
- Main package substrate editor spawns DIE Abstract I/O Feasibility Planner when a co-design die needs to be edited, imported or created.
- I/O Feasibility Planner provides IC/Package co-design through its ability to create or import & edit IC die abstracts (as LEF/DEF or OA2.2) that contain IO padding definition, die bump matrix and IO to bump connectivity assignment.
- Allows the user to establish variable bump matrices tied to unique grids across the die surface—designers can create unique grids, including pitch-free grids, for areas such as core power/ground and mixed signal
- Provides a set of bump matrix editing capabilities that enable designers to add, move, swap, delete, and modify bumps to achieve an optimized bump pattern. This is especially helpful for meeting timing requirements or escape routing
- Offers a completely new set of pin numbering schemes and controls that can cover virtually any numbering

scheme designers want to use, including user-defined prefixes or JEDEC labeling

- Supports new tiling features
- Spreadsheet-based I/O placement and sequencing environment provides an easy methodology for the manipulation of I/O sequencing to enable chip/package trade-offs during the package feasibility stage
- Connectivity assignment between the die abstract and package can be displayed in the spreadsheet for an alternate view of the data with the ability to sort/view/manipulate cells similar to other spreadsheets
- The import/export capability enables easy transfer of data between existing external spreadsheets and the imbedded spreadsheet
- An automatic driver-to-bump assignment capability finds the nearest routable match, which can be sent back to the IC tools for final routing
- Die-level redistribution layer (RDL) route feasibility offers a first-order validation of drive-bump assignment viability
- Hierarchical re-usable bump matrix tiling allows the designer to create a library of pre-defined bump patterns
- Customized tiles can contain user-specified signal/reference patterns
- Tiles can contain package routing escape patterns from under the die

EMBEDDED ELECTRICAL CIRCUIT MODEL GENERATOR

- Includes a proven easy-to-use 3D field solver for full package model creation
- Allows 3D models to be used for post-layout system interconnect verification with Allegro Package SI 620 or Allegro PCB SI 630

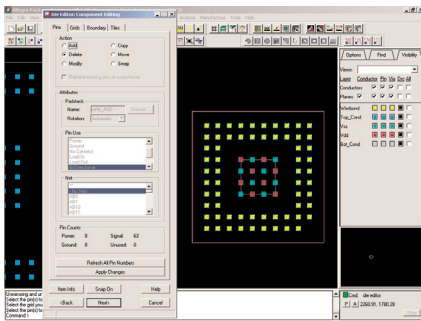


Embedded 3D field solver quickly generates accurate full package simulation models

DIE EDITOR

- Quickly generates die and package for feasibility studies
- Utilizes both silicon and package technology files to create accurate die and packages
- Eliminates the need for packaging expertise during initial feasibility studies

Spreadsheet driven I/O sequencing placement provides rapid feasibility optimization



Wizard driven die editor provides rapid creation of bump matrices and substrate ball matrices for fast what-if feasibility studies

AUTOMATIC BUMP-TO-PACKAGE PIN ASSIGNMENT

- Utilizes router-based algorithms that determine best routable assignment based on existing design rules
- Identifies differential pair-defined bumps and assigns adjacent package pins accordingly

OTHER FEATURES

- The robust bi-directional LEF/DEF interface includes a new LEF library manager
- Die-level abstract comparison/verification to ensure that package and IC tools are synchronized
- Substrate-level footprint comparison/verification to ensure that package and foundry designs are synchronized
- Net delay reports, which calculate the delay on a net-by-net basis and generate a report of the entire package, can be invoked at the feasibility phase for a rough estimate or after design completion for verification

OPERATING SYSTEM SUPPORT

- Red Hat Linux 7.3, 8.0, RHEL 3.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9
- HP-UX 11.0, 11.11i
- IBM AIX 5.1

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or value-added reseller (VAR) in your area, visit www.cadence.com/contact_us.

ALLEGRO PACKAGE DESIGNER 600 SERIES COMPARISON GRID (SPB 15.5)

	610	620
ALLEGRO PACKAGE SUBSTRATE EDITOR FEATURES		
Netlist / Crossplace / Crossprobe with Allegro Design Entry (HDL or CIS)	X	X
Padstack & Symbol Editor	X	X
Customizable / Automated Drill Legend	X	X
Multiple Via Sizes, Blind / Buried Via Support	X	X
Define, store and re-use complex via structures	X	X
Autoplacement / Quickplace Floorplanner	X	X
Dynamic Shapes with Real-Time Plowing & Healing for Copper Areas	X	X
Automatic Line Smoothing	X	X
2-D Drafting and Dimensioning	X	X
Gerber 274X, 274D, GDSII Artwork Output Generation	X	X
Multiple UNDO / REDO	X	X
Valor ODB++, ODB++(X) File Output & Universal Viewer	X	X
HTML-based Custom Reports	X	X
Stroke Editor	X	X
IntelliUSE Interactive Trace Editing	X	X
Automatic Silkscreen Generation	X	X
Split Plane Support	X	X
SKILL Runtime, Macro, and Script Support	X	X
Agilent EEsof™ Integration	X	X
CAD Interfaces - DXF (Ver. 14), IDF (Ver. 2 & 3)	X	X
EDA Interfaces - PADS® (Ver. 4 & 6), PowerPCB® (Ver. 5), P-CAD® (Ver. 8)	X	X
AIF import/export for die & package shell	X	X
Length, Parallelism, and Differential Pairs Rule Support	X	X
Pin-pair Multi/Matched Nested Group Support	X	X
Real-Time DRC and Routing of Differential Pairs & Length Rules	X	X
Interactive Delay Tuning	X	X
Complex Physical Design Rule Checking (No Electrical)	X	X
Group Routing	X	X
Measure Parasitic	X	X
Advanced Trace Glossing	X	X
Database-driven Design Reuse Modules	X	X
Technology Files	X	X
Design For Assembly Rule Checking	X	X
TestPrep for Testability Access	X	X
Real-Time DRC of Delay and Crosstalk Rules	X	X
Constraint Areas and Technology File Support	X	X
Automatic Line Width Adjustment for Impedance Rules	X	X
eXtended Net Support (x-nets)	X	X
Layer Set Rules & Routing Support	X	X
Delay, Crosstalk, and Impedance Routing Support	X	X
Allegro Constraint Manager (Routing, SI & Timing Constraints & DRC Worksheets)	X	X
Z-Axis Delay Support	X	X
Extended Timing Path Support	X	X
Group Routing (Space Control)	X	X
Differential Pair (Dynamic Phase Control)	X	X
Advanced automatic wirebonding (creation & editing)	X	X
Auto create, assign and derive nets	X	X
Auto assign pin use properties	X	X
Die generator	X	X
Die text-in wizard	X	X
BGA generator	X	X
BGA text-in wizard	X	X
LEF library manager	X	X
Offset via generator	X	X
Netlist-in wizard	X	X
DEF bump matrix import	X	X
Substrate-level reusable tile generator		X
Create plating bars	X	X
Create bondpad soldermask	X	X
Create wirebond power and ground rings	X	X

ALLEGRO PACKAGE DESIGNER 600 SERIES COMPARISON GRID (SPB 15.5)

	610	620
IO FEASIBILITY PLANNER FEATURE SUMMARY FOR PACKAGE DESIGNER 600 SERIES		
Separate IO Feasibility Planner editor for co-design		X
Import die abstract as DEF or OA2.2 from FE		X
Export die abstract as DEF or OA2.2 to FE		X
IO cell placement spreadsheet		X
RDL trial router		X
LEF layer mapping		X
IC die level reusable tile generator		X

	610	620
ALLEGRO PACKAGE ROUTER FEATURE SUMMARY FOR PACKAGE DESIGNER 600 SERIES		
256 Signal Layer Limit Router Auto/Interactive	X	X
Shape-based or grid Autorouting	X	X
SMD Fanout to Vias	X	X
Trace Width by Net and Net Classes	X	X
Staggered Pin Support	X	X
45-degree ECO Routing	X	X
Memory Pattern Routing (SMD or Through-hole)	X	X
Interactive Via Search	X	X
Interactive Routing with Shoving and Plowing	X	X
Interactive Floorplanning	X	X
Autoplacement	X	X
Online Design Rule Checking	X	X
Flip, Rotate, Align, Push, and Move Components	X	X
Placement Density Analysis	X	X
Layer Set Rules & Routing Support	X	X
Signals on Specific Layers	X	X
Width and Clearance Rules by Layer	X	X
Via Rules by Net and / or Net Class	X	X
Net and / or Net Class Rules by Layer	X	X
Crosstalk Violation Report	X	X
Trace Length Violation Report	X	X
Blind and Buried Via Support	X	X
Via Under SMD Pad Checking	X	X
Automatic Wire Bonding	X	X
Plural Vias Router	X	X
Stacked Vias	X	X
Enhanced Via Fanout	X	X
Automatic Trace Spreading	X	X
Automatic Via Reduction	X	X
Automatic Miter 90 to 45	X	X
Automatic Test Point Generation	X	X
Test Point Specific Clearance Rules	X	X
Minimum, Maximum, and Matched Length Rules	X	X
Crosstalk Controls on Same and Adjacent Layers	X	X
Virtual Pins, Which can be Moved During Autorouting	X	X
Parallelism Controlled by Length and Gap	X	X
Differential Pair Routing	X	X
Automatic Net Shielding	X	X
Design Rules by Area	X	X
Online Display of Length Tolerance	X	X
Global Violation Indicator	X	X
Dynamic Display of Available Length	X	X
Automatic Single Net Routing	X	X
Multiple Net / Bus Routing	X	X
Relative Delay Rules	X	X
Z-Axis Delay Support (Package Editor Integration Only)	X	X
Extended Timing Path Support (PCB Editor Integration Only) PCB Performance x	X	X
Pin-pair Multi/Matched Nested Group Support (Package Editor Integration Only)	X	X

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