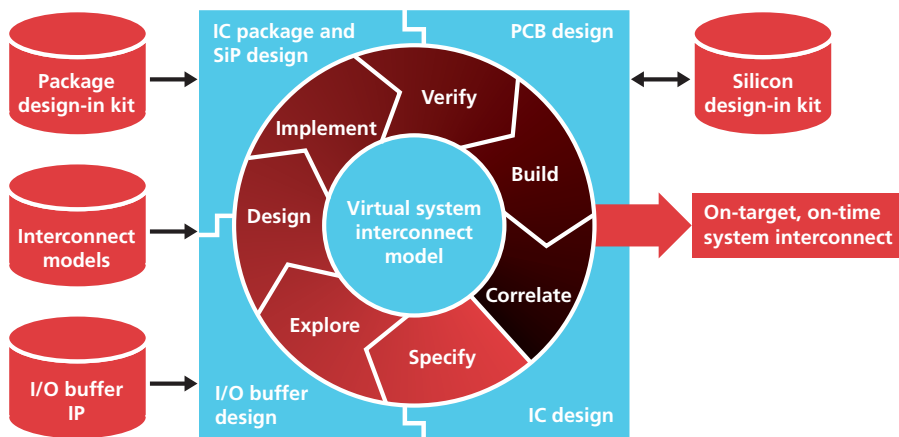


## ALLEGRO PCB SI GXL

Cadence® Allegro® PCB SI GXL provides a virtual prototyping environment for designs with signals operating in the multi-gigahertz (MGH) frequency range. It offers a completely integrated signal design and analysis solution built on top of the proven Allegro PCB SI environment. Its advanced technology shortens design cycle time and eliminates the need for multiple lab qualifications with full functional physical prototypes.



The Allegro system interconnect design platform

### THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP Portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

## ALLEGRO PCB SI GXL

Designing system interconnects with signals operating in the MGH range requires capabilities that quickly and accurately model each element of the signal's path. This is because at high frequencies the losses on a signal mount as the signal travels through different discontinuities such as vias, connectors, and different layers in one or more printed circuit boards. At gigahertz (GHz) frequencies, the loss in a transmission line can amount to approximately 0.25+ dB/inch, creating challenges for longer interconnects on PCB systems. Ensuring that losses in critical signals are acceptable is an important step in the design of MGH signals. To accomplish this, Allegro PCB SI GXL lets engineers perform loss budget tradeoffs quickly and iteratively using S-Parameters. It also provides a way to change the MGH signal's topology and view expected loss through the system interconnect within seconds.

Allegro PCB SI GXL offers engineers a highly integrated virtual prototyping environment that includes built-in productivity capabilities for MGH designs. It addresses MGH design challenges in an integrated environment that is easy to use and includes several advanced modules: SigXplorer topology exploration environment; high-capacity simulation, SPICE-based simulation subsystem; Allegro Constraint Manager; Allegro Model Integrity; floorplanner/editor and PCB Router; and EMControl.

Technological advances—such as differential signals with embedded clocks (serial links), drivers with pre-emphasis, and receivers with equalization—allow engineers to architect systems that have higher performance and throughput. However, many of the EDA solutions required to design systems such as these have not kept pace, leaving engineers forced to use disparate, stand-alone products to design systems with high-speed signals, particularly those that operate in MGH range. Allegro PCB SI GXL addresses the numerous challenges typically created

as system designers work to provide ultra-high bandwidth for data transfer against shrinking market windows.

Another key challenge for MGH designers involves ensuring that timing and voltage margins in differential signals used in serial links are met. As traditional circuit simulators are limited to approximately 1024 bits of custom stimulus pattern length, the effect of inter-symbol interference (ISI) is not adequately modeled. To accurately predict the eye opening, engineers need solutions that can simulate stimulus patterns of over one million bits. On a typical PC/Windows platform, Allegro PCB SI GXL can simulate 10,000 bits in just seconds (one million bits in an hour).

## BENEFITS

- Eliminates the need for physical prototypes for multiple qualifications through advanced simulation techniques
- Shortens design cycle time through faster tradeoffs of MGH signals using S-Parameters and single or coupled analytical via modeling
- Improves product quality, cost, and performance

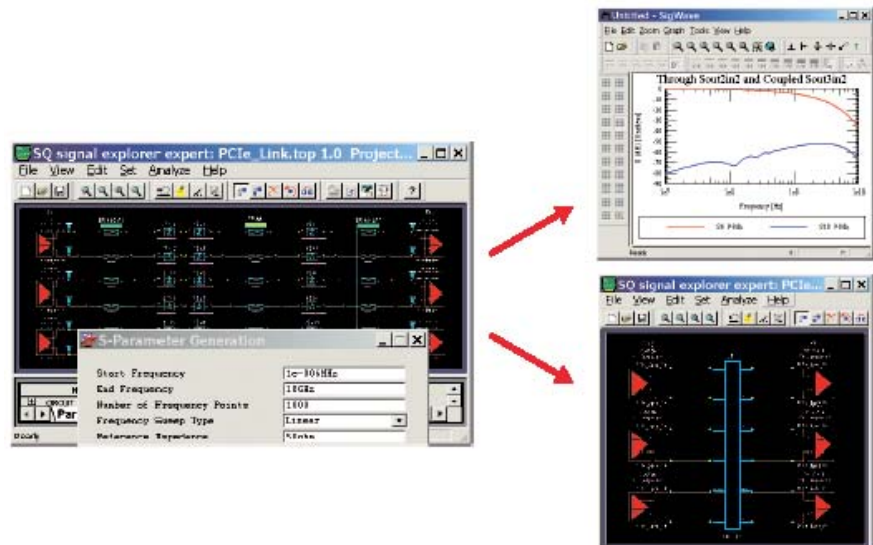
- Saves time via a virtual prototyping environment that is seamlessly integrated with other Allegro platform design products

## FEATURES

### INTEGRATED S-PARAMETER SUPPORT

Integrated S-Parameter support enables engineers to generate S-Parameters from PCB signal topologies (“Stack-up to S”) and plot in SigWave quickly and easily. Users can change topology or stack-up and do quick iterative loss budget tradeoffs. It also allows designers to concatenate multiple S-Parameters into one, simulate S-Parameters in time domain, and incorporate S-Parameters for an object into the topology and then generate S-Parameters for the entire topology.

Additionally, by incorporating S-Parameter support that is flexible, Allegro PCB SI GXL allows engineers to incorporate measurement-based S-Parameter models in native Touchstone format. S-Parameters with other interconnect topologies can also be incorporated, measured, or imported.



*Any portion of the passive interconnect can be plotted as S-Parameter in SigWave topology explorer*

## MACRO MODELING

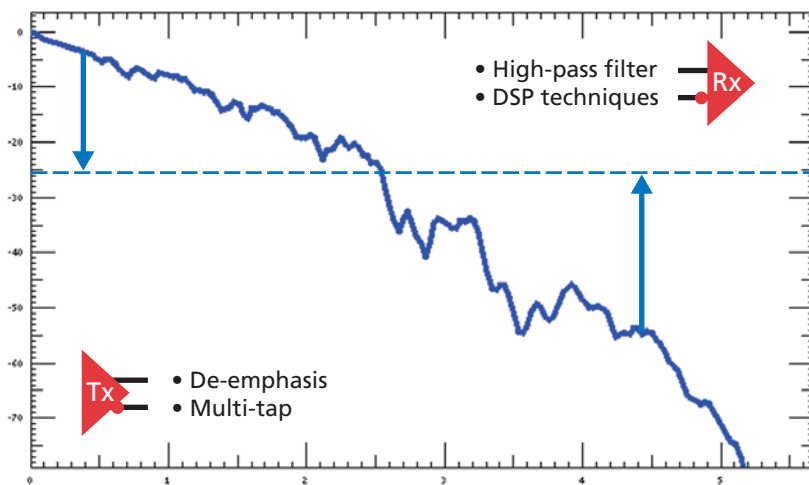
Macro modeling capabilities enable engineers to model and simulate MGH drivers and receivers faster and more accurately—with simulation performance improvements of 20x to 400x over transistor-level simulation.

## VIA MODEL GENERATOR

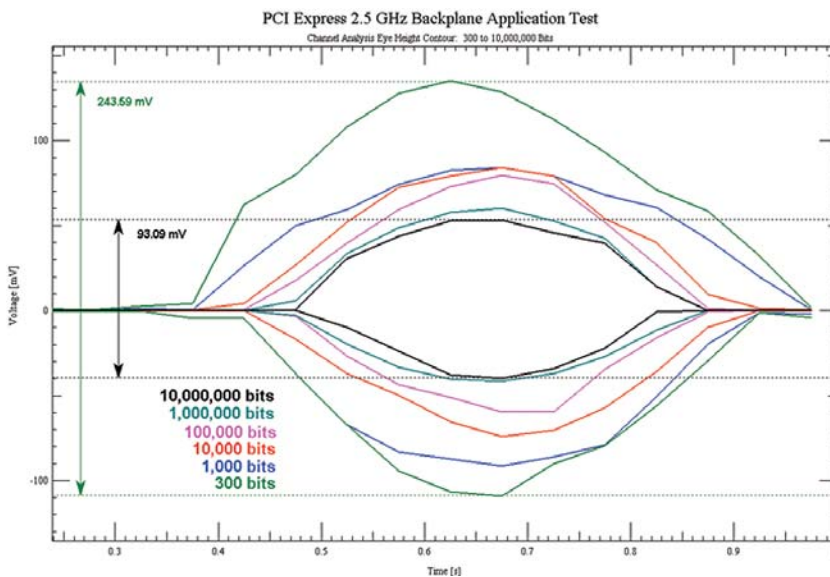
Users can quickly create accurate via models (wideband, narrowband, S-Parameter) to simulate via stub effects at MGH frequencies for single vias, differential vias, and vias coupled with ground/power vias.

## HIGH-CAPACITY, HIGH-PERFORMANCE SIMULATION

The Channel Analysis module within Allegro PCB SI GXL addresses the need for high-capacity simulation that can ensure timing and voltage margins are met for MGH signals. The Channel Analysis module allows users to simulate up to 10 million bits very rapidly. On a typical PC/Windows platform, it can simulate 10,000 bits in just seconds, a million bits in an hour. Users can quickly develop meaningful configurations (“tap settings”) for a complex driver or receiver. To



Users need proven advanced macro modeling capabilities for devices with preemphasis of receiver equalization without sacrificing simulation performance



Eye shrinks with number of bits in stimulus pattern. A good eye diagram is important for accurate jitter, insertion loss, and BER prediction

determine optimal settings, designers get a recommendation for a specific topology in seconds, saving weeks of simulation time.

## SIGXPLOER TOPOLOGY EXPLORATION ENVIRONMENT

SigXplorer is used for pre-route topology design and analysis, even before a schematic is created. This type of analysis is common at the earliest stages of the design cycle when designers assess the impact of using a new device technology or of increasing bus transfer rate. SigXplorer can be used to build and validate detailed electrical topology models and prove the viability of a new technology—before the detailed design process begins.

Integrated solution space exploration is provided through the SigXplorer topology editor and simulation cockpit. Engineers can model frequency-dependent losses and skin effect accurately for MGH signals with an integrated field solver. Quick trial implementation is possible using the tightly integrated Allegro PCB Router XL.

## SPICE-BASED SIMULATION SUBSYSTEM

The Allegro PCB SI GXL circuit simulation engine (TISim) is a proven SPICE-based simulator that combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. TISim includes the capability to simulate S-Parameters in time domain. By combining both structural and behavioral modeling techniques, TISim enables engineers to accurately and efficiently model complex device behavior. TISim also includes a lossy coupled, frequency-dependent transmission line model that accurately predicts the distributed behavior of PCB traces into the GHz range.

## ALLEGRO CONSTRAINT MANAGER

Allegro Constraint Manager allows users to capture, manage, and validate various rules in a hierarchical fashion. It provides a real-time display of high-speed rules and their status based on the current state of a design. With

Allegro Constraint Manager designers can group all of the high-speed constraints for a collection of signals and form an electrical constraint set (ECset) that is then associated with those nets to manage their actual implementation. ECsets can be used to drive the PCB layout design process, shortening the design cycle time.

### ALLEGRO MODEL INTEGRITY

The Model Integrity module allows designers to quickly create, manipulate, and validate models in an easy-to-use editing environment. Device model formats supported include:

- IBIS 4.1 External Model support for Verilog<sup>®</sup>-A, Spectre<sup>®</sup>, HSPICE, Cadence eSpice models
- Mentor/Quad XTK
- Cadence Device Modeling Language (DML)

A Spectre-to-DML conversion module assists in creating DML models from Spectre simulation runs. With the output of the Spectre simulation run buffer options file, users can quickly create DML models. Model integrity identifies V-I and V-T tables for typical, maximum, and minimum corner cases from the Spectre run file. A proven, intelligent best-curve-fitting algorithm provides an accurate DML model. An HSPICE-to-IBIS conversion module allows users to create IBIS models from HSPICE simulation runs.

Complete library management through Model Integrity lets users read and write touchstone format S-Parameters, check passivity of S-Parameters, and plot S-Parameters—all with the click of a button.

### FLOORPLANNER/EDITOR AND PCB ROUTER

The floorplanner provides a graphical view of the PCB database allowing users to view, simulate, and edit the PCB design. Designers can quickly and easily evaluate the effects of different placement strategies on design behavior. They can also perform test routing using proposed electrical constraints to ensure high-speed design rules are achievable before passing them on to the PCB layout designer.

### EMCONTROL

By applying a combination of standard rules and user-defined rules, EMControl can eliminate weeks of manual checking and improve product quality and reliability. For a standard rule set, EMControl provides comprehensive, knowledge-based, design rule checking (DRC) for common EMI-related placement and routing issues. For user-defined rules, EMControl allows creation of custom rules that fit within a company's design guidelines. Importantly, these rules capture the high-speed design "experience" as customized rules, which in turn can be reused on future designs.

The EMControl module predicts far-field differential-mode radiated emissions in both SigXplorer and the Allegro PCB SI floorplanner. It also allows for exploration of design strategies required to keep radiation within acceptable levels. Near-field EMI analysis, available within the Allegro PCB SI floorplanner, can predict radiated energy immediately above the board surface. By analyzing near-field EMI patterns, designers can identify which portions of a routed trace are producing the most radiated energy and adapt the design accordingly.

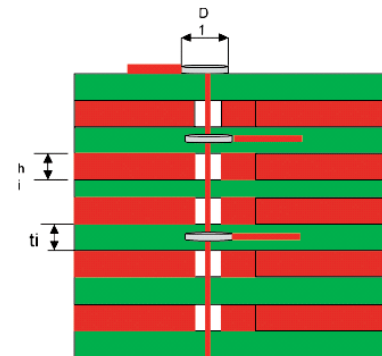
### I/O BUFFER MODELS

Supported I/O buffer model formats include:

- Cadence Allegro PCB SI Device Modeling Language (DML)
- Synopsys HSPICE transistor-level models (requires HSPICE simulator and license, which is not included with Allegro PCB SI GXL)
- Cadence Spectre transistor-level models (available on Sun Solaris, HP UX, and Linux RHEL 3.0 platforms only). This utilizes an integrated and limited capability version of the Spectre simulator, which is included with Allegro PCB SI GXL
- IBIS 4.1 External Model support for HSPICE, Spectre, Verilog-A, and Cadence DML
- Mentor/Quad XTK

### INTEGRATION AND INTERFACES

Allegro PCB SI GXL reads and writes Allegro PCB database (.brd files) and provides interface to Mentor Board Station layout database.



*Via model generator allows users to model stub effects at MGH frequencies during pre-route exploration and analysis phase of the design process*

### OPERATING SYSTEM SUPPORT

- Red Hat Linux 7.3, 8.0, RHEL 3.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9
- HP-UX 11.0, 11.11i
- IBM AIX 5.1

### CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink<sup>®</sup> online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

## ALLEGRO PCB SI FEATURES

Major feature summary for SI, Allegro Design Entry HDL, Allegro PCB SI GXL, and Allegro PCB PI Option XL

	Allegro PCB SI XL	Allegro Design Entry HDL SI XL	Allegro PCB SI GXL	Allegro PCB PI Option XL
Allegro Design Entry HDL XL		x		
Assign Models in Schematics		x		
Create Xnets in Schematics		x		
Apply Constraints and Topologies to Schematic for Single-ended and Differential Nets		x		
Single-line Topology Editor (Graphical Canvas)	x	x	x	
Simulation Setup Advisor	x		x	
Model Integrity: Model Development Environment	x	x	x	
Model Integrity: Syntax Checking for IBIS 3.2 and DML	x	x	x	
Model Integrity: HSPICE-to-IBIS Conversion	x	x	x	
IBIS 4.0 Models Support	x	x	x	
Quad Models Translator	x	x	x	
Spectre Transistor-level Models	x	x	x	x
Macro-models Support (DML)	x	x	x	
Simulation Control: Single-line Simulation	x	x	x	
Waveform Viewer	x	x	x	
Detailed Simulation Reports (Such as Flight Time, Overshoot, Noise Margin)	x	x	x	
Coupled (3 Net) Simulation	x		x	
Coupled (>3nets) Simulation	x		x	
Single Net Pre-layout Extraction from Allegro Design Entry HDL	x	x	x	
Allegro Physical Viewer Plus				
Differential Pair Exploration and Simulation	x	x	x	
Differential Pair Pre- and Postlayout Extraction from Allegro PCB Editor	x		x	
Differential Pair Pre-layout Extraction from Allegro Design Entry HDL	x	x	x	
Differential Signal Constraint Capture	x	x	x	
Coupled Line Simulations	x	x	x	
Crosstalk Simulation	x	x	x	
Sweep Simulations	x	x	x	
Current Probes	x	x	x	
Multiterminal Black Boxes in Topologies	x	x	x	
Constraint Development and Capture of Topologies	x	x	x	
Custom Measurement	x	x	x	
Custom Stimulus	x	x	x	
Batch Simulation	x		x	
EMControl: Rules Development	x		x	
EMControl: Rules Checking	x		x	
EMI Differential Simulation	x	x	x	
Allegro Constraint Manager	x	x	x	
Color-coded Real-time Feedback on Violations			x	
Apply Constraints and Topologies to Board for Single-ended and Differential Nets	x		x	
Floorplanner	x		x	
Constraint-driven Floorplanning and Routing	x		x	
Allegro PCB Router XL	x		x	
HSPICE Simulator Interface	x	x	x	x
S-Parameter Generation from Stackup			x	
S-Parameter Plotting in SigWave			x	
Time Domain Simulation of S-Parameters			x	
Library Management of S-Parameters in Model Integrity			x	
Coupled Via Model Generator for Pre-layout Explorations			x	
High Capacity Simulation Using Channel Analysis Overlay			x	
Optimum Pre-emphasis Bit Configurations ("Tap Settings")			x	
Power Integrity: Design and Analysis Environment				x
Power Integrity: Decoupling Capacitor Database Setup Wizard				x
Power Integrity: Impedance Requirements Calculator				x
Power Integrity: Decoupling Capacitor Selection and Placement Environment				x
Power Integrity: VRM Editor				x
Power Integrity: Decoupling Capacitor Library Editor				x
Power Integrity: Cross-probing Between Waveform Allegro PCB SI Floorplanner				x
Power Integrity: Frequency Domain Analysis				x

## FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223

or visit [www.cadence.com](http://www.cadence.com) for additional information. To locate a Cadence sales office or Cadence Channel Partner in your area, visit [www.cadence.com/contact\\_us](http://www.cadence.com/contact_us).