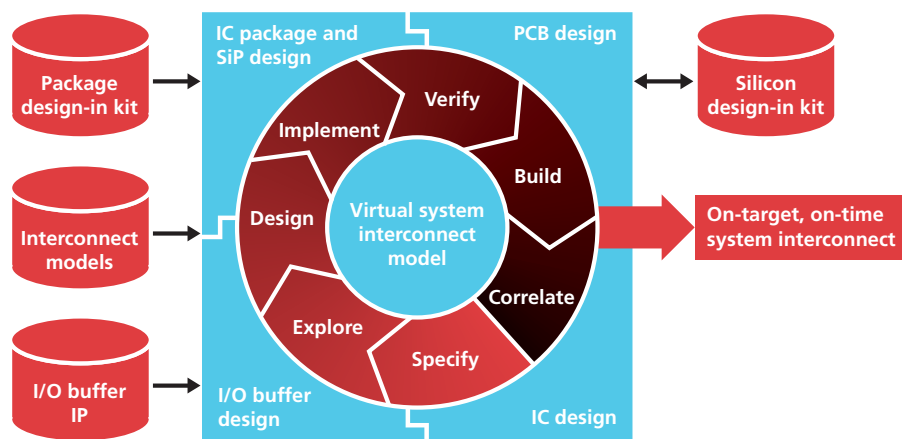


ALLEGRO DESIGN ENTRY HDL SI XL

Cadence® Allegro® Design Entry HDL SI XL allows electrical engineers to develop and embed optimum constraints in printed circuit board (PCB) design intent. Tightly coupled with Allegro Design Entry HDL XL, it allows designers to leverage proven simulation technology to develop and specify constraints on nets as they are created. With Allegro Design Entry HDL SI, engineers can shorten design cycle time by enabling a constraint-driven PCB design process from the outset of a design.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

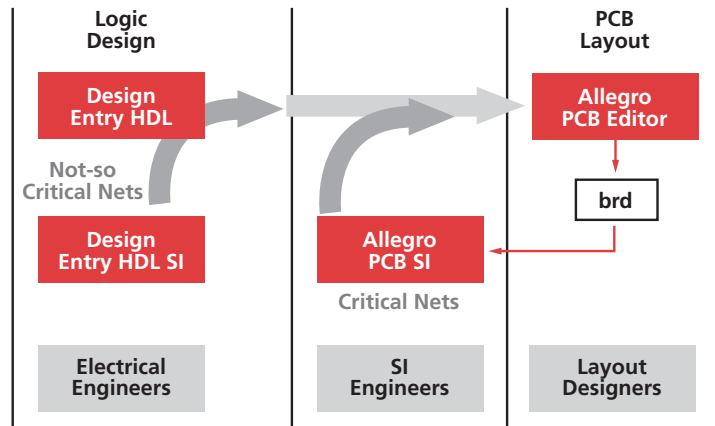
ALLEGRO DESIGN ENTRY HDL SI XL

The number of nets on a PCB system that have high-speed constraints has increased rapidly over the past few years. Today, more than 50 percent of the nets in any given design typically have high-speed constraints. As a result, engineers have seen design cycle time increase, even with a dedicated team of signal integrity (SI) engineers developing constraints through simulation. With the number of constraints growing rapidly, SI engineers can easily become the bottleneck in the design process. This situation, coupled with today's inefficient and disparate methods of communicating high-speed constraints, contributes to unnecessary, expensive, and time-consuming physical prototype iterations.

Cadence Allegro Design Entry HDL SI XL addresses these challenges with a collaborative design environment that fosters teamwork on all aspects of a design. It allows SI engineers to focus on critical leading-edge signals, while leaving the not-so-critical nets for electrical engineers to manage. A constraint-driven PCB flow allows electrical engineers to use proven simulation tools to develop and specify constraints at the very beginning of the design process from a familiar schematic environment. Allegro Design Entry HDL SI XL includes: Allegro Design Entry HDL XL, SigXplorer topology editor and simulation cockpit, Allegro Constraint Manager, a Model Integrity module, and a proven Allegro PCB SI simulation subsystem.

BENEFITS

- Shortens design time by enabling a constraint-driven design flow from the outset
- Eliminates unnecessary iterations between design entry/logic design and physical layout
- Enables development of reusable electrical constraint sets
- Makes constraints part of design intent for the original design and all revisions



Allegro Design Entry HDL SI XL enables a collaborative working environment between SI engineers and EEs to shorten the design cycle

- Improves communication and data flow through a unified constraint management system
- Reduces product cost and improves performance by enabling development of optimum constraints
- Eliminates unnecessary physical prototypes caused by avoidable SI issues

FEATURES

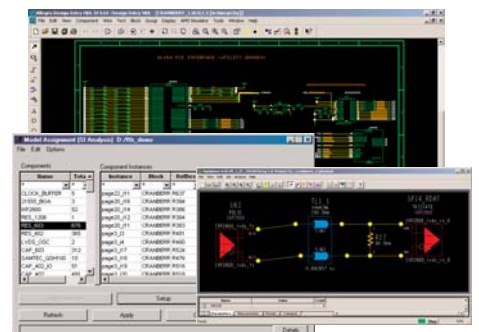
TIGHT INTEGRATION BETWEEN DESIGN ENTRY HDL AND SIMULATION

Tight integration with Allegro Design Entry HDL XL allows the SigXplorer topology editor and simulation cockpit to be leveraged from a schematic environment, and SI models to be assigned to components and specific pins directly in the schematic. Engineers can create extended electrical nets (Xnets) and assign constraints to them in Allegro Constraint Manager accessed from Allegro Design Entry HDL XL.

ALLEGRO DESIGN ENTRY HDL XL

Allegro Design Entry HDL provides a number of benefits including: concurrent and hierarchical design; part creation with HDL or HDL generation from schematics; a standard electrical rules checker plus the ability to create user-defined rules; a part developer for creating and validating parts; a Build Physical Wizard to import Actel, Altera, and

Xilinx FPGAs; support for digital simulation through NC-Verilog® and NC-VHDL simulators; and support for creating design variants. A bill of materials (BOM) can be generated in multiple formats, including those for design variants. Import RF blocks from ADS through IFF interface. For more information, refer to the Allegro Design Entry HDL XL datasheet.



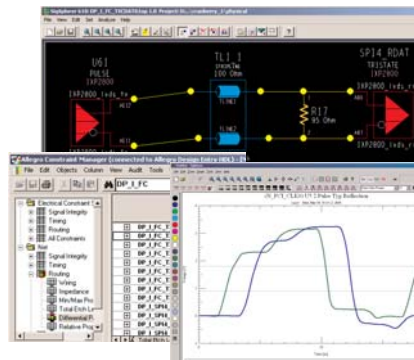
Design Entry HDL SI XL tightly integrates design entry with SigXplorer topology editor and simulation cockpit for developing constraints through simulation

SIGXPLOER TOPOLOGY EXPLORATION

SigXplorer topology explorer provides a graphical environment for exploring, analyzing, and defining interconnect strategies that provide an electrical view of the physical interconnect. Use “what if” analysis to determine the effects of different routing strategies, component values, and design tolerances. The proven topology exploration and simulation cockpit provides capabilities for exploring different topologies to improve performance. Users have the ability to specify routing strategies for critical-signal types including daisy, star, or user-defined.

Designers can develop an optimum set of constraints to ensure reliable performance under a wide range of operating conditions with solution space exploration. Sweep design parameters such as differential impedance and delay/length. Explore physical implementation parameters such as trace width, gap, and maximum uncoupled length for differential signals. Designers can also trade-off electrical performance with reliability and the cost of manufacturing the final PCB system.

Designers can also develop custom measurements associated with the topology using built-in timing measurements with basic arithmetic functions—addition, subtraction, multiplication, and division. Custom measurements can be embedded in the constraint set and reused during the post-layout verification stage. Reusable constraint sets allow design constraints to be captured as an electrical constraint set (ECSet) and embedded in the PCB database to drive the physical design process (placement and routing). Users can include routing strategy for a signal or a group of signals in the constraint set.



Users create an electrical constraint set (ECSet) for a net or a group of nets through simulation to enable a constraint-driven PCB layout process

SPICE-BASED PCB SI SIMULATION

The Allegro PCB SI engine is a SPICE-based simulator that combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. Driver, receiver models, and field solver include a lossy coupled, frequency-dependent transmission line model that accurately predicts the distributed behavior of PCB traces up to several GHz. Support for both structural and behavioral modeling techniques enables complex device behavior accurately and efficiently.

A proven, integrated 2D field solver is used to determine the electrical characteristics of routed etch and to create models of PCB vias. In addition, an IBIS-style behavioral driver element models I/O behavior based on the V-I and V-T data provided by behavioral modeling techniques.

SigWave waveform display allows users to import waveform data directly from various standard test equipment formats as well as from the output formats of popular SI analysis tools. The oscilloscope mode allows users to turn the display of individual waveforms on and off; provides markers for use in making on-screen measurements; and permits notes to be added to the display. The logic-analyzer mode presents waveforms alongside each other, making logic behavior and bus transactions easier to observe. A spectrum analyzer mode displays signal behavior in the

frequency domain using one of several FFT techniques. An eye-diagram mode allows users to view patterns in long simulation sequences and enables them to interactively define the signal period and starting offset.

ALLEGRO CONSTRAINT MANAGER

Allegro Design Entry HDL SI XL includes the same Allegro Constraint Manager that is used with other Allegro products: Allegro PCB Editor, Allegro PCB SI, Allegro Package Designer, and Allegro Package SI. It allows users to capture, manage, and validate various rules hierarchically. Design cycles can be shortened by creation of reusable ECSets for a net or a collection of nets. Different high-speed rules can be checked in real time as the design process proceeds (displays color-coded results). Users can view the actual results of SI analysis to manage simulation-based electrical constraints.

MODEL INTEGRITY

The Model Integrity module allows designers to create, manipulate, and validate models quickly in an easy-to-use editing environment. Device model formats supported are:

- IBIS 4.1 External Model support for Verilog®-A, Spectre®, HSPICE, Cadence eSpice models
- Mentor/Quad XTK
- Cadence Device Modeling Language (DML)

A Spectre-to-DML conversion module assists in creating DML models from Spectre simulation runs. With the output of the Spectre simulation run, buffer options file, users can quickly create DML models. Model integrity identifies V-I and V-T tables for typical, maximum, and minimum corner cases from the Spectre run file. A proven, intelligent best-curve-fitting algorithm provides an accurate DML model. HSPICE-to-IBIS conversion module allows users to create IBIS models from HSPICE simulation runs.

OPERATING SYSTEM SUPPORT

- Red Hat Linux 7.3, 8.0, 9.0 RHEL 3.0
- Windows 2000 with Service Pack 3, XP Professional
- Sun Solaris 8, 9
- HP-UX 11.0, 11.11i
- IBM AIX 5.1

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or Cadence Channel Partner in your area, visit www.cadence.com/contact_us.