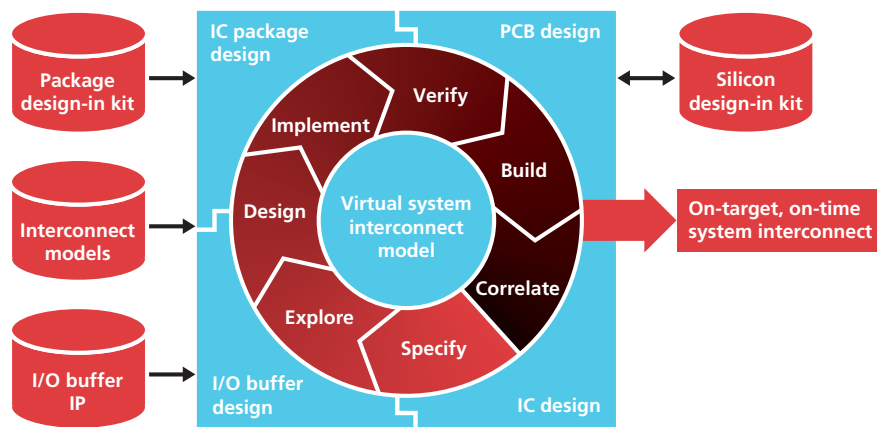


## ALLEGRO DESIGN ENTRY HDL L, XL

Cadence® Allegro® Design Entry HDL is a complete, scalable solution for creating printed circuit board (PCB) schematics. This constraint-driven and highly customizable product provides powerful features for team-based design and design reuse. It comes tightly integrated with Allegro Constraint Manager and Allegro PCB Editor, as well as with solutions for digital, analog, and pre-route signal integrity (SI) simulations. Available on multiple platforms, Allegro Design Entry HDL also supports controlled enterprise deployment.



The Allegro system interconnect design platform

### THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

## ALLEGRO DESIGN ENTRY HDL

Allegro Design Entry HDL is a complete and scalable solution for the design of PCB schematics. Tightly integrated with Allegro PCB Editor and Allegro Constraint Manager, Allegro Design Entry HDL provides a robust and highly customizable solution for constraint-driven PCB design. It supports enterprise deployment and incorporates a number of features and utilities that accelerate schematic creation. Additionally, it supports design reuse at the sheet, block, and design-levels in addition to typical copy/paste features. Multiple users can work simultaneously on a design, giving design teams much needed flexibility on tough projects. Integration with Cadence Incisive® simulators further enables digital simulation (Verilog®, VHDL) and PSpice® for analog simulation.

## BENEFITS

- Reduces design spins via a proven, constraint-driven flow
- Provides special support for buses, extended nets, and differential pairs
- Reduces rework and prevents errors by supporting flexible design reuse
- Integrates with digital and analog simulators
- Reduces total cost of ownership (TCO) through enterprise deployment support
- Provides flow validation—verified end-to-end with Allegro PCB Editor
- Shortens design cycle via team-based design
- Supported by a powerful library creation and management solution
- Integrates with Allegro Design Workbench for workflow management
- Provides ability to import IFF output from Agilent ADS for RF designs

## FEATURES

### CONSTRAINT-DRIVEN DESIGN

Integration with Allegro Constraint Manager makes constraint capture easy and communication of constraints reliable. In addition to simple nets, Allegro Constraint Manager understands all design objects including buses, extended nets, differential pairs, and matched groups. It allows reuse of constraints—within and across designs—by using electrical constraint sets (ECSets). Constraint values between the schematic and layout can be compared and changes communicated in either direction using Design Differences. This feature is extremely useful when board layout is outsourced, as constraints are created by design engineers and compliance must be ensured after layout. The spreadsheet-like constraint management system allows users to capture all electrical constraints within the design database, dispensing with the need to communicate constraints and design data separately. Since the design rule checking (DRC) system in Allegro PCB Editor tracks any constraint violation, the designer can verify that the constraints specified in the schematic database and in Allegro PCB Editor are identical.

### DESIGN REUSE SUPPORT

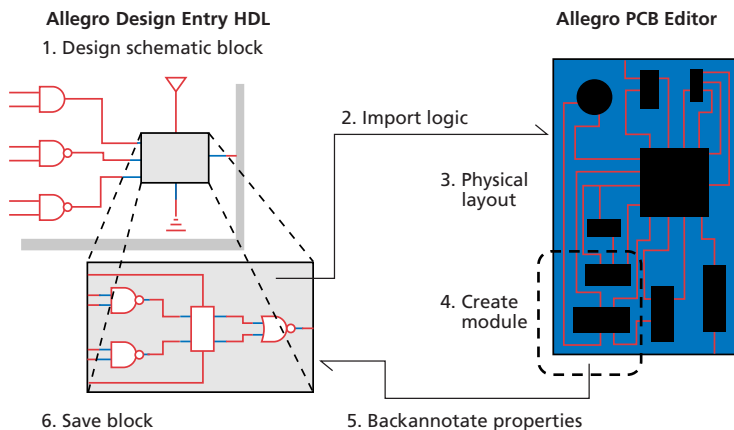
Most designs start from other designs or reuse significant parts of other designs. Allegro Design Entry HDL gives designers the flexibility to choose the most effective design reuse approach, reducing rework and errors typically caused by rework. Designers

can reuse electrical constraints as part of a block or by using ECSets. They can also create a new project with parts of an old design using the Copy Project utility, or copy/paste across projects to share small circuits, or copy single or multiple sheets from one design to another using the Import Sheet UI.

Allegro Design Entry HDL further allows designers to create reused blocks and place them in a library for reuse in other designs just as with components. The connectivity, constraints, and layout from each block can also be reused. The same block can be used multiple times in the same design without renaming or copying. Additionally, designers can use a complete hierarchical design as a block in another design, or reuse constraints and block layouts.

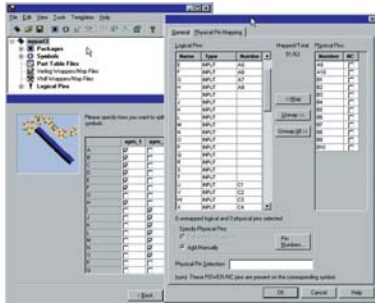
### ENTERPRISE DEPLOYMENT SUPPORT

Allegro Design Entry HDL is network installable and provides support for enterprise-wide deployment, lowering cost of ownership. Default options, menus, and custom utilities can be available at an installation, site, or at the user level. Libraries can be shared at a site level and design teams can employ automated features to make other designers aware of library updates. Scripting and programming language support for specific extensions is also provided, making it easy to deploy organization-specific utilities to all users. Almost all utilities can be run from the command line, and program options can be controlled by the project file, allowing users to launch and run programs from within their customized



*Allegro Design Entry HDL supports full reuse of PCB layout data for hierarchical blocks, increasing reliability and saving time*

workflows and to automate repetitive tasks. Designers can write their own schematic rule checks and deploy them using the powerful design entry HDL rules checker, and UIs for custom commands can be built using JAVA.



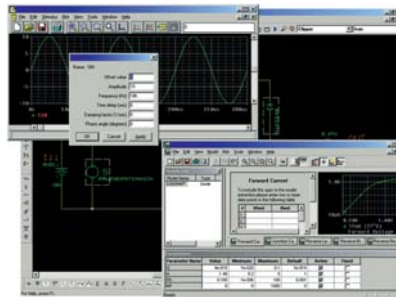
*Comprehensive and intuitive part creation allows designers to quickly create parts that are complete, correct, and verified in the design flow*

### COMPLETE SOLUTION

Allegro Design Entry HDL provides a complete array of utilities:

- Part Manager tracks part usage to ensure that parts are always in sync with the design database
- Global Find and Replace searches for parts with specific attributes and replaces them with other parts on a page, set of sheets, blocks, or in the complete design
- Global Find and Global Navigate make it easy to quickly find a component, pin, or signal anywhere in the design and cross-probe to it
- Cross-probing with Allegro PCB Editor makes it easy to find components by locating them on the schematic and vice versa. The cross-placement features of Allegro PCB Editor are used to select in the schematic and place in the board
- BOM Generator can be customized to fit the requirements of any data management system
- Cross-referencer creates cross-reference tables for signals, parts, and pins and appends them to the pages of a design
- Design Differences compares logical and physical designs for netlist, properties, and constraints
- Design Association is used to update the schematic with connectivity changes made on the board

- Project Manager, a customizable tool launcher, allows users to control program options for all tools in the flow
- Power Group Builder makes it easy to work with invisible power pins to make schematics more compact
- Variant Editor creates designs that share the same common PCB but are populated differently
- Build Physical Wizard makes it easy to integrate output from Xilinx, Actel, and Altera FPGAs into PCB designs



*Tight integration with Allegro AMS Simulator lets designers perform analog simulation and debugging within the Allegro Design Entry HDL environment*

### SIMULATION INTEGRATION

Designs can be simulated in Verilog and VHDL using Cadence Incisive simulators. Allegro Design Entry HDL can also generate hierarchical single file netlists. For analog simulation, tight integration with PSpice allows designers to use the same solution for simulation as for PCB layout, reducing rework and providing cost benefits. Pre-route SI simulation can be done using Signal Explorer, which is integrated with Allegro Constraint Manager.

### SCALABLE SOLUTION

The scalability of Allegro Design Entry HDL to other Allegro products protects initial investment. This is because most design databases are the same, allowing them to be used seamlessly across versions. Allegro Design Entry HDL can be easily upgraded to Allegro Design Editor to accelerate complex designs, or integrated with Allegro Design Workbench to better manage workflow.

### MULTIPLE PLATFORM SUPPORT

Allegro Design Entry HDL is available on Windows, Solaris, Linux, HP-UX, and IBM-AIX. Design databases are

identical across platforms, providing the flexibility to choose a hardware platform in line with other IT needs without having to change the design entry solution. This is important as companies consider a move to Linux and/or Windows, because it allows them to move from AIX or HP-UX in a phased manner.

### FLOW VALIDATION

Allegro Design Entry HDL is fully integrated within the Allegro platform to ensure seamless data flow and integration. In contrast to multi-vendor environments, library creation, schematic designs, constraint capture, logic transfer, PCB design, back annotation, and many other aspects of the flow are tested routinely and thoroughly at every release. Delivery of advanced capabilities often requires enhancements in multiple tools and flow validation ensures that these different tools work in synchronization.

### SYSTEM REQUIREMENTS

- Linux RHEL 3.0, RHEL 4.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9, 10
- HP-UX 11i
- IBM AIX 5.3

### CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

## ALLEGRO DESIGN ENTRY HDL L/XL FEATURE SUMMARY

	Allegro Design Entry HDL L	Allegro Design Entry HDL XL
<b>PRODUCTIVITY FEATURES</b>		
Global Find and Replace	x	x
Page Management UI	x	x
Global Navigate	x	x
Variant Editor	x	x
Project Manager	x	x
Cross Referencer	x	x
Custom Variables	x	x
<b>CONSTRAINT-DRIVEN DESIGN FEATURES</b>		
Component Revision Manager	x	x
Design Association	x	x
Constraint Manager		x
High-speed Model Assignment		x
Topology Editor		x
Support for Constraints on Extended Nets, Differential Pairs, Buses		x
<b>COMPONENT MANAGEMENT FEATURES</b>		
Component Revision Manager		x
Component Research	x	x
Part Developer	x	x
Part Manager		x
Bill-of-Material Generator	x	x
<b>DESIGN REUSE FEATURES</b>		
Physical Design Reuse	x	x
Hierarchical Blocks Reuse	x	x
Import Blocks and Sheets		x
Copy Projects		x
Copy/paste Within and Between Designs	x	x
<b>SIMULATION AND INTERFACES</b>		
Check Plus		x
Verilog, VHDL Netlisting	x	x
PSPice Integration		x
<b>INTERFACES</b>		
SKILL	x	x
Caerviews		x
Import IFF		x
EDIF 300		x
<b>FLOW</b>		
Cross probing with PCB Editor	x	x
Allegro Viewer Plus		x
<b>FPGA INTEGRATION</b>		
Build Physical Wizard for Xilinx, Actel, Altera	x	x

## FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223  
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