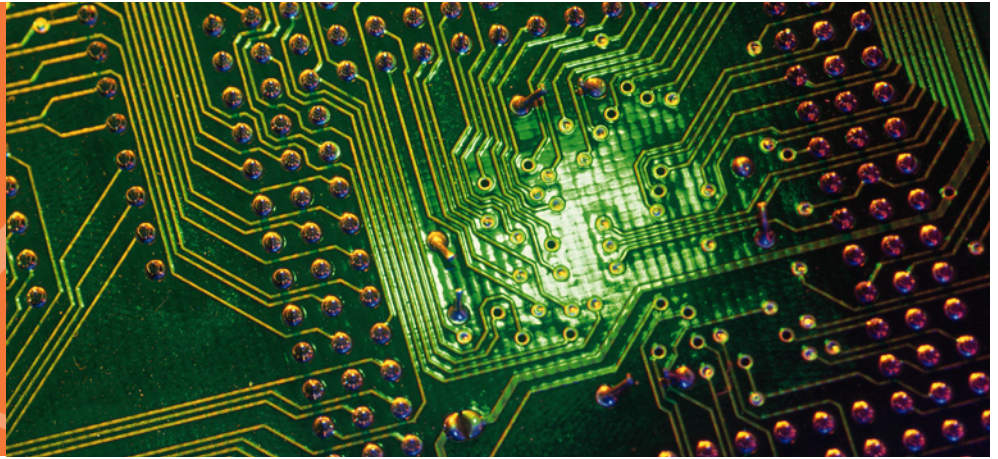


DFM Verification System
for PCB Designers

Enterprise 3000



Design for Excellence

Enterprise 3000 is the ultimate design-for-manufacture (DFM) solution with over 700 physical design verification and manufacturing optimization functions serving the PCB/MCM/HDI layout engineer, as an integral part of the design flow. Enterprise 3000 integrates bi-directionally with the leading PCB design systems to support a fully automated design-for-excellence environment.

Zero Defects, First Time!

Enterprise 3000 is a unique 'predictive engineering' solution where the needs of design and manufacturing come together. It rationalizes the requirements of the electrical engineer and multiple manufacturers who need to build the boards with 'zero defects, first time', while balancing functional constraints with prototype, pre-production, and volume production yields. At the heart of Enterprise 3000 is ODB++, containing all the intelligence from a CAD database as well as the process constraints from the manufacturers; eliminating the need for multiple, unintelligent files and older data exchange methods. ODB++ is the most intelligent, robust, convenient and open data exchange methodology fully supporting the challenging 'design anywhere, build anywhere' requirements of today and the future.

Design Anywhere, Build Anywhere

Increasingly, electronics designers are faced with having to outsource designs to multiple fabricators and electronics manufacturing service providers, each of whom work to different constraints and processes. Additionally the design engineer's own layout constraints and criteria must be incorporated into this process. Enterprise 3000 solves the complex challenge of applying and managing multiple rules sets from multiple sources. Enterprise 3000 optimizes the design by considering, incorporating, and validating these constraints concurrently at the design level.

By integrating the varied manufacturing processes and constraints during design, the engineer can easily and successfully implement and support the 'design anywhere, build anywhere' model, prevalent in today's electronics industry. Enterprise 3000 applies manufacturing rules and producibility ranges, defined in engineering rules files (ERFs),

which are suitable for easy exchange between designers, fabricators and manufacturers. The result is one fully integrated manufacturing data set (ODB++), harnessing the intelligence of the PCB CAD database, yet optimized against all manufacturing and physical design requirements.

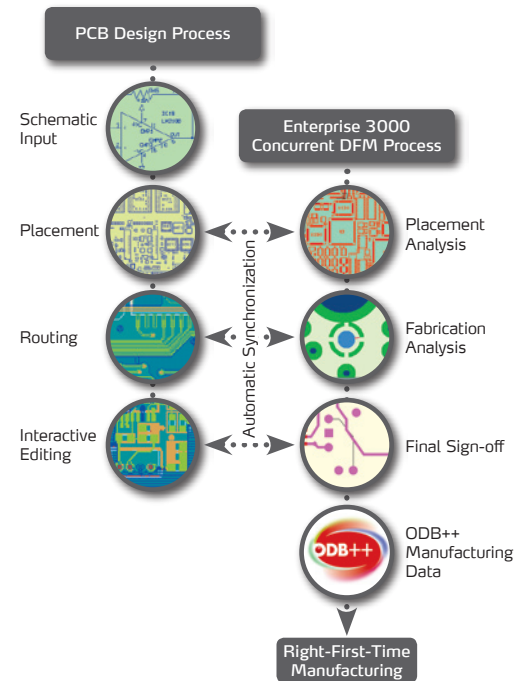
Improved Designer/Manufacturer Communication

ODB++ provides unambiguous, risk-free, bi-directional data exchange throughout the electronics supply chain. ODB++ facilitates the product's quick trip from the design engineer's desktop through right-first-time manufacturing and then out to the market. The result is reduced costs, faster time-to-market and improved quality.

Flexible, Scalable DFM Environment

Enterprise 3000 is a fully scalable system based on the engineer's choice of modules according to specific DFM needs. Building on the core Graphic Station any number or combination of analysis and optimization modules can be added to configure a fully tailored system.

Depending on the design engineer's specific verification requirements, for example assembly and test, bare board fabrication, or HDI technology, Enterprise 3000 provides full flexibility to create the optimum DFM environment, delivering maximum return on investment.



"PCB Design companies using Valor DFM solutions have less than half the design re-spins of companies not using Valor"

Aberdeen Research, June 2007

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Graphic Station

Multi-featured WYSIWYG graphic user interface. Supports all ODB++ based engineering functions, from input, through DFM analysis and optimization, to output of manufacturing datasets. Supports 2D/3D viewing and manipulation of the complete printed circuit assembly data model.



ERF Manager

Provides a structured basis for efficient rules management for integration into the DFM and design process, enabling effective upstream transfer of manufacturing process rules from multiple manufacturing service providers.



Graphic Synchronization

Concurrent design data revision control with hot links from Enterprise 3000 directly to your original layout system, all on the same workstation.



Assembly & Bare Board DFM Optimization

Repeatable engineering data optimization functions for automated yield optimization. Maximize yield. Minimize board cost and scrap. Includes solder paste/solder mask optimization, legend clipping, annular rings/spacings optimizations, sliver filling, copper balancing and more.



Valor Parts Library (VPL)

Integrates parametric physical models of each component into the ODB++ job file, enabling true virtual prototype manufacturing simulation, concurrently in the design process.



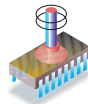
HDI Analysis

A unique set of analysis tools designed to identify potential fabrication issues associated with microvia and sequential lamination technologies.



Assembly/Test Analysis

Type sensitive analysis yields 100+ categories including: fiducial analysis, component analysis, pin-to-pad analysis, testpoint analysis, solder paste analysis.



Sharelist

Sharelist operates within the Graphic Station to capture selected DFM analysis results and package them in an open document format for effective engineering collaboration. Combining graphical text/numerical data records, Sharelist also includes user comments and suggestions. Output formats include HTML, XML and formatted ASCII.



Bare Board Analysis

Shape based analysis yields 100+ categories, for example: signal layer analysis, power and ground analysis, silk screen analysis, soldermask analysis, drill analysis.



3D VRML Simulator

Navigate through a realistic 3D view of the finished board - all it takes is ODB++ data intelligence, Enterprise 3000 and any VRML viewer.



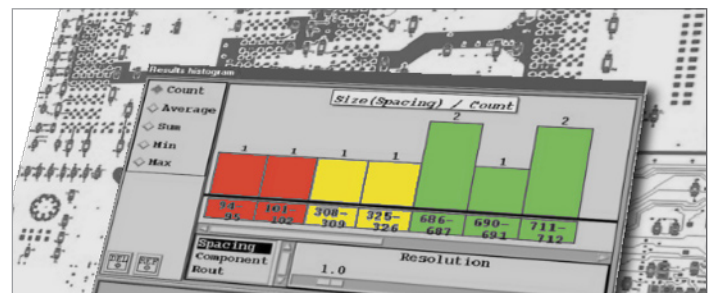
Netlist Analysis

Ensure electrical integrity by running comparisons between actual board connectivity and the EDA schematic netlist.



Signal Quality Analysis

Rules-driven analysis for physical design characteristics of constrained nets, including analysis in 2D and 3D for such issues as parallelism of adjacent layer circuits.



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