

TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Course Title	SiP Layout v16.5
Course Category	System Interconnect Design – Allegro & OrCAD
Duration	5 Days
Course ID	ES_86090_16.5
Product Version	16.5

Course Description

This course takes you through a complete design flow of a *System in Package* (SiP) design, from defining the module outline through placing components, defining a netlist, placement, routing, documentation, and manufacturing output. The course covers the complete design flow for a flip-chip and wire-bonded stacked die module using the Cadence® SiP Layout software.

Learning Objectives

In this course, you

- Develop a process flow to suit your design needs
- Create a cross section and design constraints in your SiP layout database
- Add a co-design die to your SiP layout and edit that co-design die in the I/O planner tool
- Wire bond a stacked die design
- Use the 3-D viewer to view and check your design in three dimensions
- Route an SiP design using interactive and automatic methods
- Generate a variety of manufacturing outputs for your SiP design

Software

Cadence SiP Layout XL 16.5

Audience

- Package MCM Designers

Prerequisites

- None

Course Agenda

Day 1

- User interface
- Creating I/O components
- Creating standard die
- Creating and editing co-design die

Day 2

- Creating co-design die
- Design constraints
- Die stack editing
- 3-D viewing

Day 3

- Adding discrete components
- Power and ground rings
- Wire bonding

Day 4

- Routing
- Conductor planes
- Degassing

Day 5

- Vendor preparation
- Reports
- Manufacturing data

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Related Courses

- [Allegro High-Speed Constraint Management v16.5](#)
- [Allegro Package Designer v16.5](#)