

TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Allegro PCB SI Foundations – v16.01

Description

This course teaches you how to use the Allegro® PCB SI tool to successfully develop and drive design rules for high-speed designs.

You learn to develop high-speed design rules using Allegro PCB SI XL and then add the resulting physical and electrical constraints to the design through topology templates.

These constraints are then used to drive the routing of nets on the printed circuit board.

You perform pre-route and post-route signal simulations to analyze the PCB for reflection, simultaneous switching, crosstalk, and other high-speed design factors.

In this course you will learn to:

- Create, extract, and explore topologies.
- Execute Solution Space Analysis.
- Create an electrical constraint set.
- Use constraints to drive placement and routing.
- Run post-route DRC check.
- Use template revision to update the ECSet applied on the nets/bus.
- Analyze the routed board design for signal integrity.
- Create a DesignLink between boards and use it to run multi-board simulation.

Audience

- PCB Layout Designers
- PCB Designers
- Electrical Engineers

This course is for electrical engineers whose design responsibilities include PCB signal analysis and designers who are concerned with the problems associated with high-speed designs.

Other students are layout designers with a basic knowledge of high-speed electrical issues who want to understand the high-speed process and the interactions between the electrical designer and the PCB SI tools of the process.

Software

You need the Allegro PCB SI XL series product version 16.01.

Prerequisites

- Basic understanding of the UNIX and Windows operating systems and commands
- Familiarity with digital/analog circuit design methodologies

- Working knowledge of printed circuit board design and signal analysis (some SPICE simulation processes; characteristics of electro-magnetic theory; transmission line theory)

Related Courses

- Allegro High-Speed Constraint Management
- Allegro PCB SI GXL
- Allegro PCB SI EMControl
- Allegro PCB Power Integrity

Course Agenda

Day 1

- Allegro PCB SI Design Flow
- Introduction to Allegro PCB SI XL
- Board Setup Requirements
- DC Net Connections
- Model Assignment
- Default and Discrete Models
- Model Integrity
- IBIS to DML Translation
- Net Extraction
- SigXplorer Basics
- Simulations with SigXplorer
- Sweep Simulations
- Trace Models

Day 2

- Constraint Floorplanning
- Constraint DRCs
- DRC Routing
- Creating a DesignLink
- System Analysis
- Post-Route Analysis
- Reflection and Crosstalk Simulation
- Post-Route Bus Analysis
- Differential Pairs
- Creation and Assignment
- Extracting and Simulation
- DRC Errors and Routing