DATASHEET

CADENCE OrCAD SIGNAL INTEGRITY

To stay competitive in today's market, engineers must take a PCB design from engineering through manufacturing with shorter design cycles, tighter project goals and faster time to market. To be successful, designers need a set of powerful, intuitive, and integrated tools that work seamlessly across the entire PCB design flow.

Cadence OrCAD signal integrity technology is available as Cadence OrCAD Signal Explorer.

Cadence® OrCAD® personal productivity tools technologies (including Cadence PSpice® and OrCAD Capture) have a long history of addressing these requirements. Available as standalone products or in comprehensive suites, OrCAD technologies allow designers to take products from conception to final output. The powerful, tightly integrated PCB design technologies include design capture, librarian tools, PCB editing/routing, and analog/signal integrity simulators. Easy-to-use and intuitive, they offer exceptional value and future-proof scalability to the Cadence Allegro® series of PCB design products.

Increasing design density, complexity, and faster edge rates create a multitude of signal integrity issues, which can lead to time-consuming and frustrating simulate-fix-simulate iterations and increased production costs. Cadence® OrCAD® Signal Explorer helps engineers address signal integrity issues throughout the design process—from the very beginning of the cycle through placement and final routing. Seamless integration with Cadence OrCAD PCB Editor eliminates database conversion and possible translation issues. Engineers can now perform signal integrity analysis or topology exploration at any stage of the design cycle—when the board is partially or fully placed, partially or fully routed, and even when no netlist or PCB database exists.

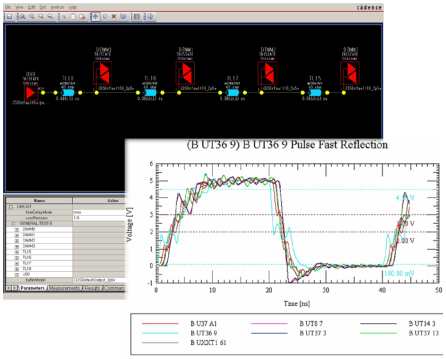

Figure 1:OrCAD Signal Explorer analyzes and validates topologies and interconnect to help minimize potential SI-related issues for fewer re-spins and shorter lab debug time.

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Cadence OrCAD Signal Explorer provides a SPICE-based simulation environment for PCB signal integrity analysis. It consists of the Tlsim simulation engine, the SigWave waveform display, the device modeling language (DML), translators from other modeling formats, and a library model editing/management subsystem.

BENEFITS

- Enables pre- and post-layout signal integrity analysis at any stage of the design cycle, ensuring constraint adherence
- Enables the exploration, analysis, and design of interconnect topologies to increase circuit reliability, improve circuit performance, and reduce prototype re-spins
- Eliminates need to translate design databases to run simulations by importing extracted topologies directly from OrCAD PCB Editor
- Easy-to-use model editing environment creates, manipulates, and validates a variety of models, quickly improving model/simulation performance

FEATURES

SIGXPLORER MODULE

OrCAD Signal Explorer provides an electrical view of the physical interconnect and a simulation cockpit for analysis of critical high-speed signals. Users can explore a net before schematics are created by using the SigXplorer module in a standalone mode. SigXplorer provides various stripline and microstrip models–lossy or lossless–to get started with the exploration. Since OrCAD Signal Explorer integrates seamlessly with OrCAD PCB Editor, users can extract a net in the pre-route or post-route stage right into SigXplorer. Users can then quickly analyze the signal using SPICE-based simulation environment.

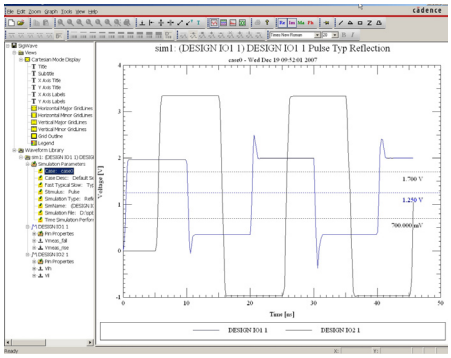

Figure 2: View and analyze simulation results in SigWave.

SPICE-BASED SIMULATION ENVIRONMENT

The Tlsim simulation engine combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. It includes an IBIS-style behavioral driver element that models I/O behavior based on the V-I and V-T data provided by behavioral modeling techniques.

By combining both structural and behavioral modeling techniques, Tlsim enables accurate and efficient modeling of complex device behavior. It includes a lossy, frequency-dependent transmission line model that accurately predicts the

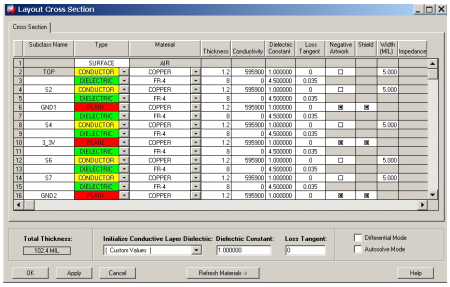

Figure 3: Users can change topologies or stack-up information and perform quick, iterative tradeoffs.

distributed behavior of PCB traces up to several GHz. An integrated electrical field solver determines the electrical characteristics of routed etch and creates electrical models of PCB vias

SALES, TECHNICAL SUPPORT, AND TRAINING

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For a complete list of authorized Cadence Channel Partners, visit **www.cadence.com/partners/channel_partner/index.aspx.**

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