EMA TimingDesigner®

The industry's most accurate static timing analysis

DIGITAL TIMING

What's New: TimingDesigner 9.4

This document covers a list of features that have been, added, enhanced, and/or fixed with the TimingDesigner 9.4 release.

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Sigrity Integration

TimingDesigner provides an interface with Cadence® Allegro® Sigrity® System SI to allow designers to review their parallel bus interface simulation results in an easy to understand context aware timing diagrams. This makes reviewing the complex timing relationships that make up parallel bus interfaces much easier to understand.

Unlike other SI tool integration TimingDesigner provides this integration will generate both the resulting timing data (constraints, delays, etc) AND the waveforms themselves giving users a push button method to create full timing accurate diagrams in the TimingDesigner environment.

This interface is available for the following versions of Sigrity and TimingDesigner

- TimingDesigner version 9.4 and above
- Allegro Sigrity System SI PBA 16.63 and above

Enabling TimingDesigner Export from Allegro Sigrity System SI

The TimingDesigner export is built right in to the Allegro Sigrity System SI interface. To enable the export option to be visible in the Sigrity report generation dialog you will need to enable the TimingDesigner interface in the options menu *(Tools>Options>Edit Options)*

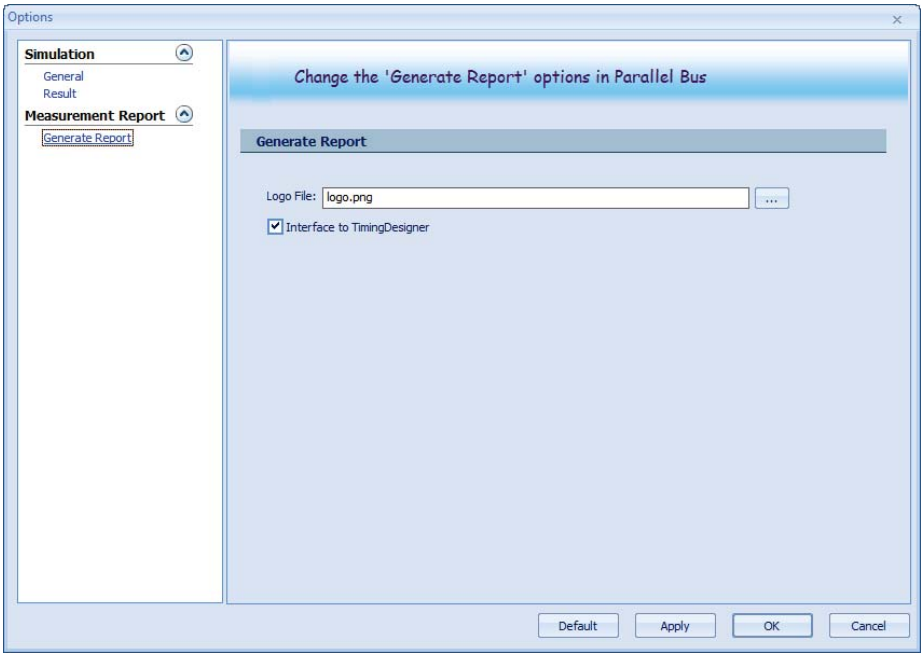


Figure 1 - Configuring Sigrity for TD Export

Generating the Report

Once the interface has been enabled you can proceed to generate timing diagrams in TimingDesigner from your Sigrity simulation data using the standard report dialog

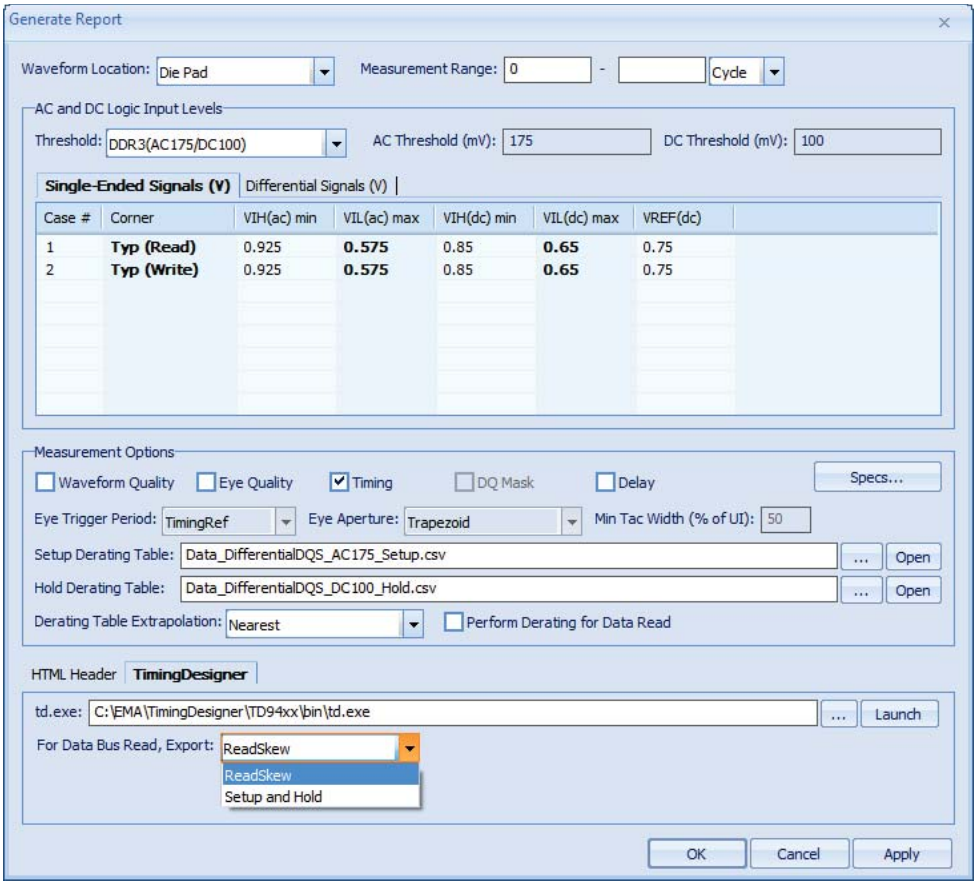


Figure 2 - Sigrity Export Dialog

At the bottom of the report you will notice a TimingDesigner tab. To generate the TimingDesigner diagrams specify the path to the TimingDesigner executable (if it is not already listed) and select *launch*. This will launch TimingDesigner and begin the import process.

Configuring your import in TimingDesigner

After selecting launch you will be presented with a few dialogs to configure how you would like the timing diagrams to be created and define the diagrams you would like to review immediately.

Diagram configuration options

- *Generate Log File:* Will generate a log file of the entire process for reference
- *Use Groups:* Will arrange the measure, variable, and constraint data generated in groups for easier navigation in the parameter spreadsheet

- *Use Constraints:* Will generate constraints in TimingDesigner for each worst case edge event (separate constraints for setup and hold)
- *Use Measures:* Will generate measure events in TimingDesigner for each worst case edge event

Selecting which diagram to open immediately
Since the amount of data to be generated in TimingDesigner can vary widely based on the simulation criteria entered into Sigrity, TimingDesigner offers an option to define what diagrams you'd like to review immediately.

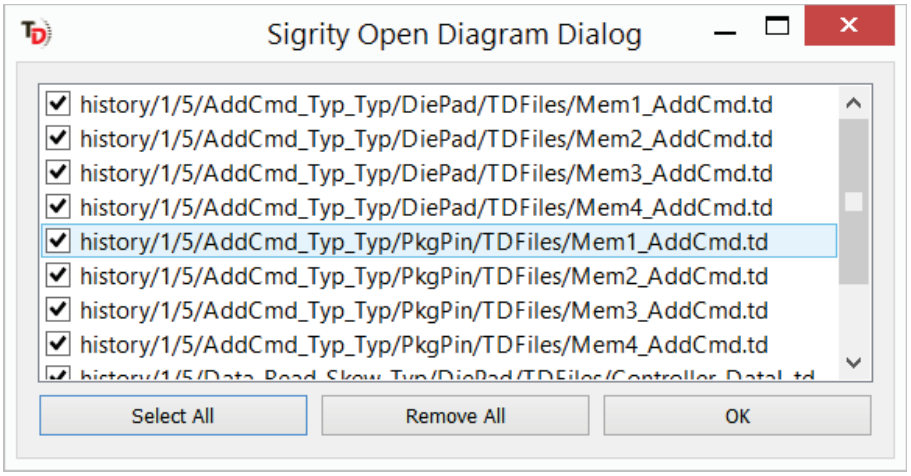


Figure 3 - Open Files Dialog

All diagrams will be created and available to access through the project manager. This option only defines what diagrams are opened for review and editing immediately.

Accessing the diagrams

Once the diagrams have been generated you can then access any of the diagrams you chose to open immediately through the tabs on the diagram window. All diagrams will be included in the User Diagrams section of the TimingDesigner project that was created along with the import.

All the diagrams will be available under the user diagrams folder of the project manager window. The diagrams are organized in a folder structure that matches that of the Allegro Sigrity tools.

Diagrams are organized under the history or results folders just as they are in the Sigrity tool

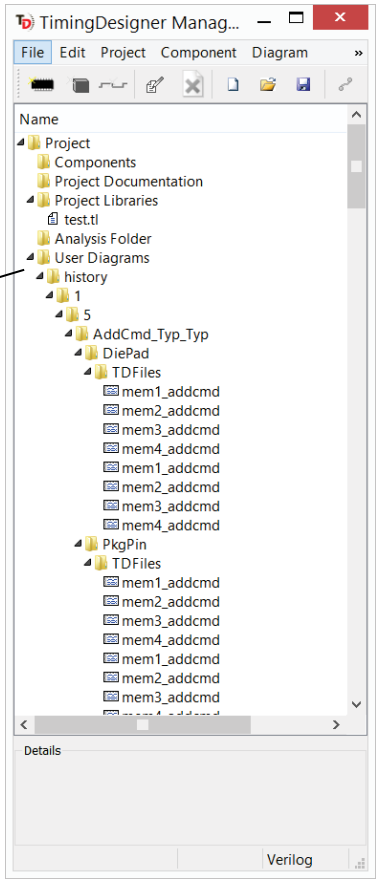


Figure 4 - Sigrity TD Project Structure

Sigrity specific diagram details

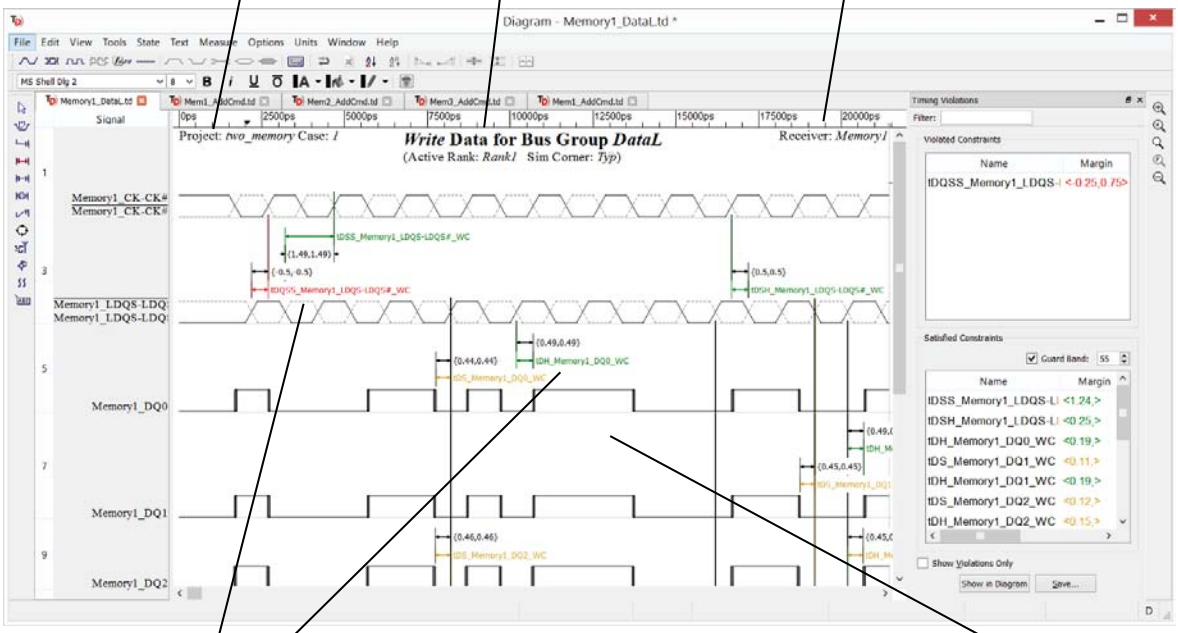
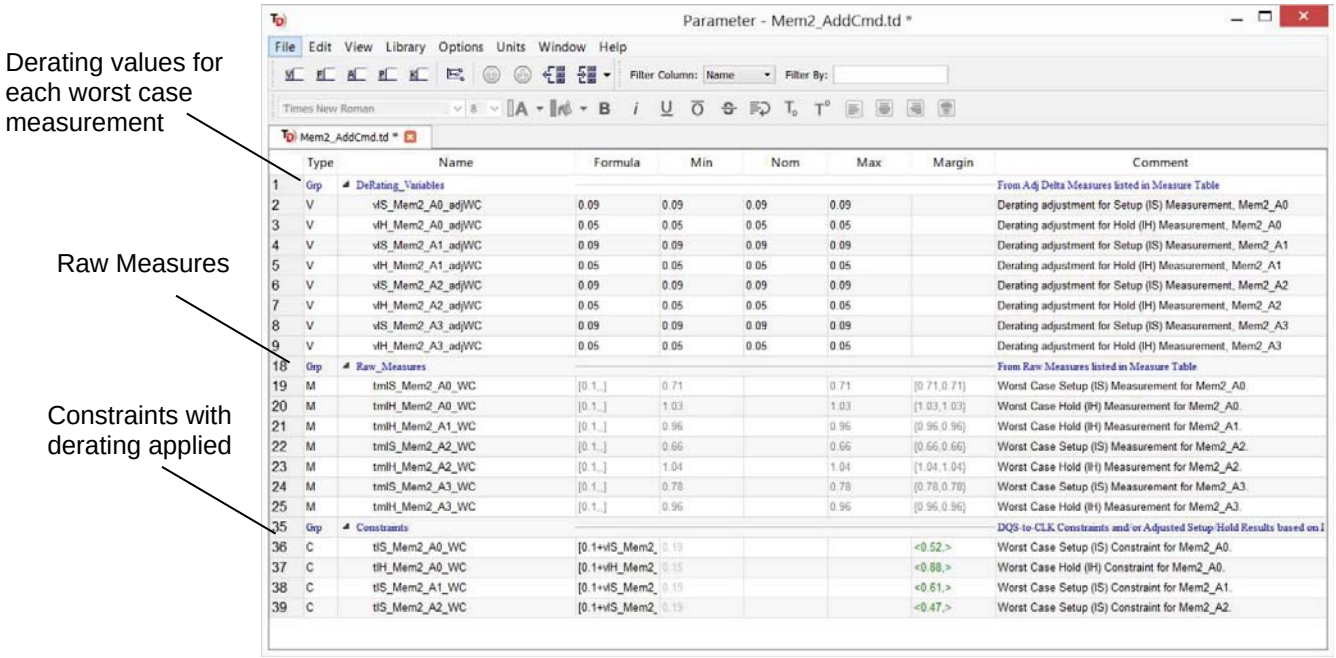


Figure 5 - Sigrity Simulation Data Presented in TimingDesigner



	Type	Name	Formula	Min	Nom	Max	Margin	Comment
1	Grp	DeRating_Variables						From Adj Delta Measures listed in Measure Table
2	V	vIS_Mem2_A0_adjWC	0.09	0.09	0.09	0.09		Derating adjustment for Setup (IS) Measurement, Mem2_A0
3	V	vIH_Mem2_A0_adjWC	0.05	0.05	0.05	0.05		Derating adjustment for Hold (IH) Measurement, Mem2_A0
4	V	vIS_Mem2_A1_adjWC	0.09	0.09	0.09	0.09		Derating adjustment for Setup (IS) Measurement, Mem2_A1
5	V	vIH_Mem2_A1_adjWC	0.05	0.05	0.05	0.05		Derating adjustment for Hold (IH) Measurement, Mem2_A1
6	V	vIS_Mem2_A2_adjWC	0.09	0.09	0.09	0.09		Derating adjustment for Setup (IS) Measurement, Mem2_A2
7	V	vIH_Mem2_A2_adjWC	0.05	0.05	0.05	0.05		Derating adjustment for Hold (IH) Measurement, Mem2_A2
8	V	vIS_Mem2_A3_adjWC	0.09	0.09	0.09	0.09		Derating adjustment for Setup (IS) Measurement, Mem2_A3
9	V	vIH_Mem2_A3_adjWC	0.05	0.05	0.05	0.05		Derating adjustment for Hold (IH) Measurement, Mem2_A3
18	Grp	Raw_Measures						From Raw Measures listed in Measure Table
19	M	tmIS_Mem2_A0_WC	[0.1,..]	0.71		0.71	[0.71,0.71]	Worst Case Setup (IS) Measurement for Mem2_A0.
20	M	tmIH_Mem2_A0_WC	[0.1,..]	1.03		1.03	[1.03,1.03]	Worst Case Hold (IH) Measurement for Mem2_A0.
21	M	tmIH_Mem2_A1_WC	[0.1,..]	0.96		0.96	[0.96,0.96]	Worst Case Hold (IH) Measurement for Mem2_A1.
22	M	tmIS_Mem2_A2_WC	[0.1,..]	0.66		0.66	[0.66,0.66]	Worst Case Setup (IS) Measurement for Mem2_A2.
23	M	tmIH_Mem2_A2_WC	[0.1,..]	1.04		1.04	[1.04,1.04]	Worst Case Hold (IH) Measurement for Mem2_A2.
24	M	tmIS_Mem2_A3_WC	[0.1,..]	0.78		0.78	[0.78,0.78]	Worst Case Setup (IS) Measurement for Mem2_A3.
25	M	tmIH_Mem2_A3_WC	[0.1,..]	0.96		0.96	[0.96,0.96]	Worst Case Hold (IH) Measurement for Mem2_A3.
35	Grp	Constraints						DQS-to-CLK Constraints and/or Adjusted Setup/Hold Results based on I
36	C	tIS_Mem2_A0_WC	[0.1+vIS_Mem2_	0.19			<0.52,>	Worst Case Setup (IS) Constraint for Mem2_A0.
37	C	tIH_Mem2_A0_WC	[0.1+vIH_Mem2_	0.15			<0.88,>	Worst Case Hold (IH) Constraint for Mem2_A0.
38	C	tIS_Mem2_A1_WC	[0.1+vIS_Mem2_	0.19			<0.61,>	Worst Case Setup (IS) Constraint for Mem2_A1.
39	C	tIS_Mem2_A2_WC	[0.1+vIS_Mem2_	0.19			<0.47,>	Worst Case Setup (IS) Constraint for Mem2_A2.

Figure 6 - Parameter Spreadsheet After Sigrity Import

Managing multiple imports in the project manager window

For each import to TimingDesigner from the same Sigrity project the diagrams will be appended to the current list following the same folder structure used by Sigrity.

Guard Band

Users can now define a guard band value to apply to their constraints to give them a second level of checking in their designs. The guard band allows design to teams to apply a "warning" or second level of analysis to their designs to not only see system failure but also be alerted to signal relationships on the verge of failure.

Setting the guard band

The guard band value can be configured by diagram and is based on a percentage of the constraints overall requirement versus the current margin. The guard band dialog is located in the timing violations window (which is newly dock able). Selecting the guard band checkbox will apply the guard band. Define the percentage of guard band you want to apply with the

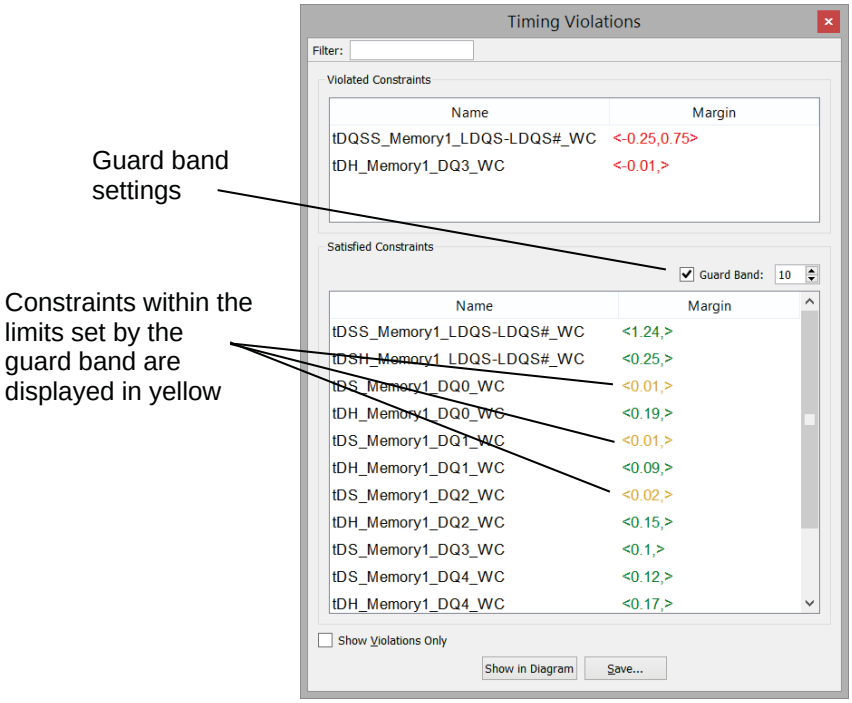


Figure 7 - Guard band

Example

Take a constraint with the following values.

Constraint Name: Guard Band Example
Requirement: min .95 ns
Margin: .05 ns
Guard band: 10%

TimingDesigner will determine if the constraints current margin is within 10% of its overall requirement. If it is then the guard band will be violated and the constraint will be displayed in yellow in the timing violations viewer and the diagram.

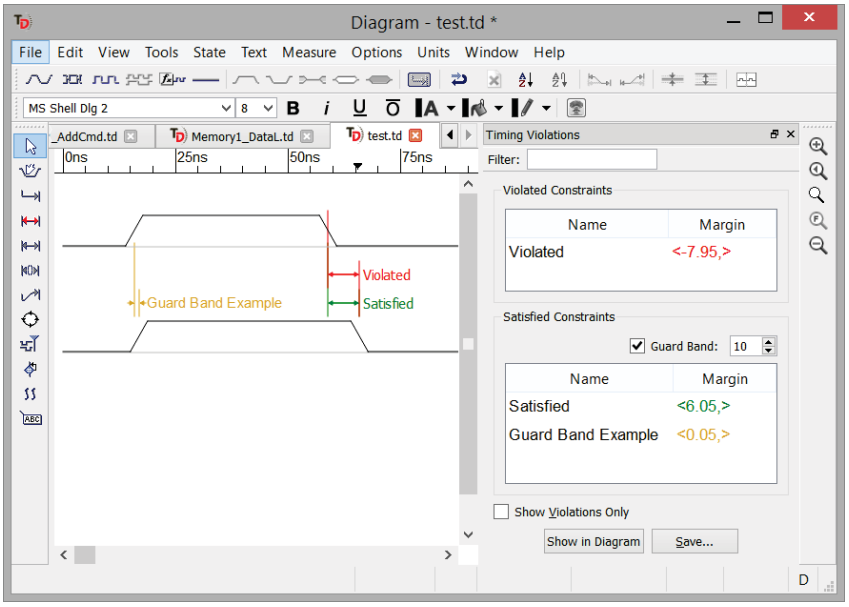


Figure 8 - Guard Band in Diagram Window

The guard band value can be adjusted and the constraints will be updated in real time. This provides a great way to do some additional reliability analysis on your design and identify areas where the design may technically pass but you may want to see if extra margin can be built in to ensure operation in the field.

User Diagrams in Project Manager

There are times when you may not want / need to use the full component structure but would still like to associate specific diagrams to a project. For those scenarios the user diagrams node of the project structure was created.

User Folder

The user diagrams folder works in a similar fashion to the component node with a couple differences.

1. The only file type that can added are diagrams
2. User Diagram structure is based on folders only (no components or blocks)
3. There is no pre-defined library connectivity as there is with component nodes

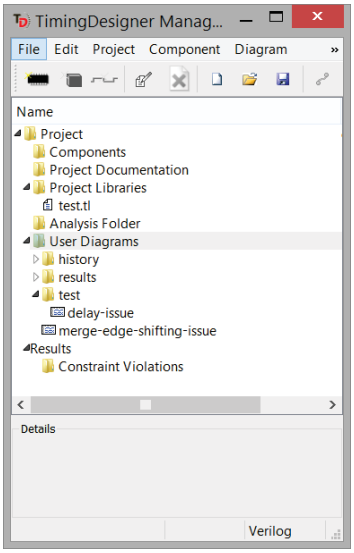


Figure 9 - User Diagrams Node

Diagrams and folders can easily be added to the user diagrams node using the RMB option.

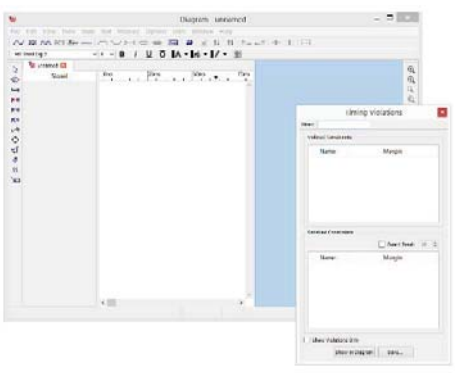
Docking Windows

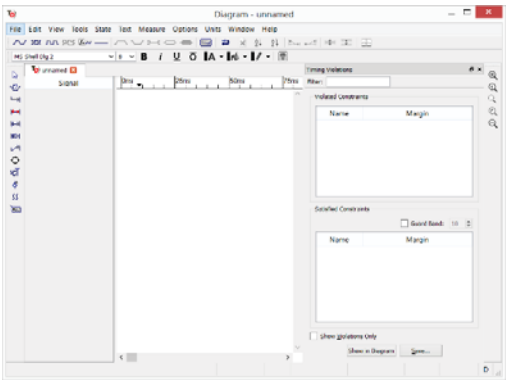
To enable users to better access information and features available in TimingDesigner version 9.4 has enabled docking for the following windows:

- Timing Violations View
- Timing Calculations Viewer

Docking the windows

The timing violations and timing calculations windows can now be docked to the left or right of the diagram window. To dock the window simply drag the dialog to left or right edge of the diagram window. The UI will adjust and present you with a blue space to indicate where the dialog will become docked.

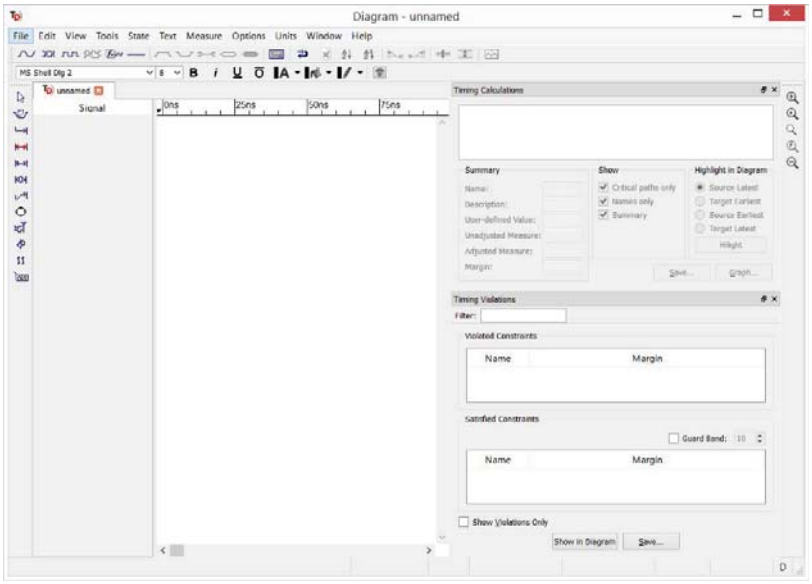




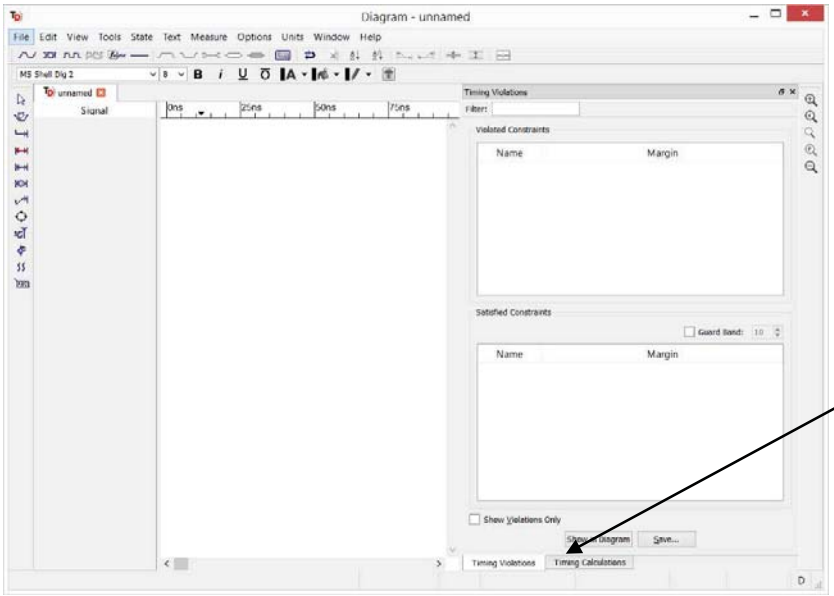
Docking Windows Together

If you want to have both the timing violations and timing calculations windows docked on the same side of the diagram TimingDesigner provides the option to display the windows in stacked or tabbed view.

Stacked View



Tabbed View



Toggle tabs to switch views

PCR's Fixed

The following is a list of PCR's that have been resolved with this release

ID#	Description
13526	TD loses library links after auto-merge completes.
13486	Auto-Merge has Library identity issues with resulting diagram
13485	Cut/Copy/Paste no longer work in Parameter SS, possibly Library SS as well.
13484	TD will close when adding a Diagram to the Analysis Folder
13477	TD will close when opening a specific diagram.
13399	Closing a Library file will close TD
13398	Unexpected close when trying to delete "unnamed" tab from Param SS when containing an open diagram.
13395	Initial opening of diagram that calls Library will encounter "illegal" characters and prompt error message.
13387	close after Auto-Merge, when deleting created merged file and saving project
13384	Text Marker Does not Appear when Comment Field is Selected
13383	Dsig Ignoring Event Changes with overlapping uncertainties
13382	Derived Signal Initial Value Setting Not Being Retained
13381	Selecting a Constraint>RMB>Convert to Guarantee is not Working
13379	TD will close when entering "new" waveform edge transition with the Pulse tool.
13376	Library Root Paths entry of "." not working correctly.
13363	TD close when adding duplicate Part Alias via Browser window
13362	Project-less diagram not responding to Library Parameter assignment.
13329	Undo in Parameter SS will deselect all previously entered variable names.
13316	Close when double-clicking "Group" row id number
13315	TD will close on Zoomed in "scrolling"
13308	close when deleting a Component from Proj. Mgr.
13300	TimingDesigner will close when adding Comments to a diagram in Project Mgr.
12986	Timing Calculations Viewer causes close
12983	Library Paths Error (Root Paths)
12866	Converting signal to bus causes issues when original signal used in Dsig.