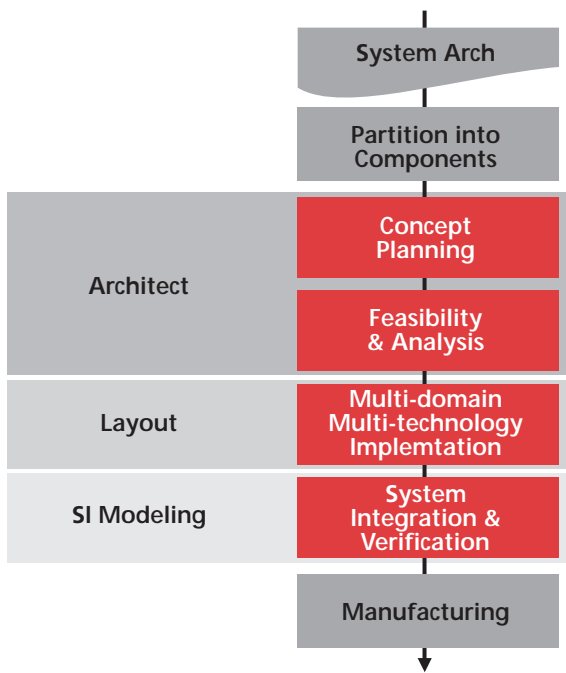


CADENCE SiP DIGITAL SI

To take full advantage of system-in-package (SiP) design, systems engineers require a new set of solutions that address the specific challenges of integrating embedded ICs with the target system interconnect. Cadence® SiP Digital SI fully integrates digital signal integrity (SI), analysis, interconnect extraction, and modeling with the physical SiP design environment. By combining proven SI technology in an environment that permits interactive editing of die-to-die and substrate interconnect, SiP design engineers can optimize a design to meet both electrical and physical requirements—while achieving reduced design cycle times.



The Cadence SiP design technology provides a methodology, flow and toolset for the definition, implementation, and verification of multi-chip and multi-component IC packages

CADENCE SiP DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of advantages over SoC. In addition to reduced cost, lower power, and higher performance, SiP design offers the flexibility to mix RF and high-speed digital circuitry in the same package. However, this also means it requires expert engineering talent in widely divergent fields. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate. This approach allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions

seamlessly integrate into Cadence Encounter® for die abstract co-design, Cadence Virtuoso® for RF module design, and Cadence Allegro® for package/board co-design.

SIP DIGITAL SI

Cadence SIP Digital SI speeds and streamlines SiP design by providing an environment for the co-design and co-simulation of SiP designs—including embedded ICs and the target PCB. By using its integrated signal integrity, parasitic extraction, and 3D modeling, engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect. The result is rapid development of cost-effective and power-friendly SiPs.

The ability to increase density by incorporating 3D structures within packages is one of the key benefits of SiP design—and one of the key challenges. SiPs can include stacked wirebond die, wirebond die stacked on flip-chip die, and direct die-to-die attachment, as well as other complex combinations such as package-on-package. To model and simulate these complex structures, Cadence SIP Digital SI includes an embedded 3D field solver, integrated S-Parameter support, and fast, high-capacity simulation (10,000 bits in seconds) to provide a unique combination of fast and accurate multi-gigahertz package module analysis.

BENEFITS

- Provides a highly integrated physical and electrical design environment
- Includes an industry-proven embedded 3D field solver and SPICE-based simulation engine
- Enables rapid evaluation of cost-versus-performance tradeoffs through its virtual prototyping environment
- Reads/writes Cadence Digital SiP Layout files

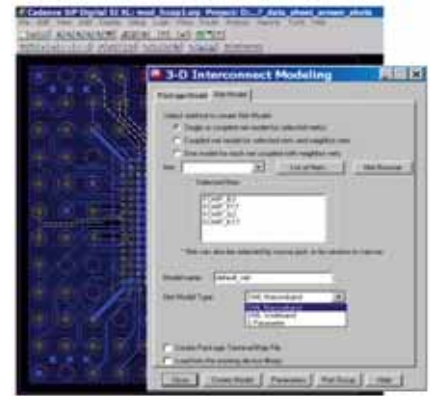
FEATURES

VIRTUAL SYSTEM INTERCONNECT (VSIC) MODELING

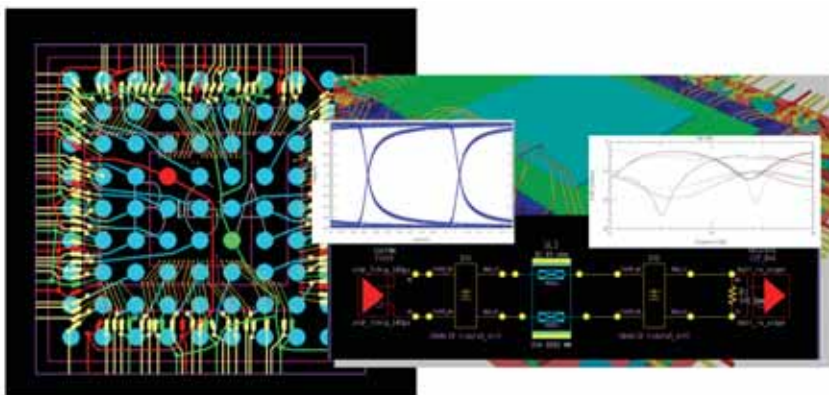
A powerful interconnect modeling environment allows either pre-route, in-route, or post-route package interconnect data to be modeled with increasing levels of detail throughout the design process. PCB interconnect can be linked to the package interconnect to create a complete buffer-to-buffer interconnect environment. SI and power integrity are analyzed using either transistor-level or behavioral I/O models along with a representative model of the power delivery network. The result is an interactive interconnect modeling environment where tradeoffs are made early in the design process and detailed post-route data enables signal quality verification.

EMBEDDED 3D FIELD SOLVER AND SIMULATION TECHNOLOGY

Seamless integration with quasi-static 3D field solver technology and SPICE-based simulation engines—from within the physical SiP design environment—enable modeling and simulation of package interconnect, without the time-consuming setup of stand-alone point tools. Engineers can quickly check tradeoffs to the physical design to ensure that electrical requirements are not compromised. Integration of analysis and design technology also allows analysis tasks that were formerly done by package SI experts to be shared by a broader group within the SiP design community.



3D interconnect model extraction is embedded into the physical design environment



Integrated Signal Integrity analysis of multi-die package designs includes 3D model extraction of complex structures such as differential pairs and power delivery networks in the time and frequency domains

PACKAGE MODELING FOR SYSTEM-LEVEL ANALYSIS

Creation of IBIS, RLC, or Cadence DML interconnect models is easily accomplished, either for a selected set of nets or for the entire package. Design teams can then easily re-use these models at the system level to ensure that package effects are properly considered when optimizing PCB cost/performance tradeoffs.

INTEGRATION WITH IR DROP ANALYSIS

Creation of n-port RLC models and terminal mapping (IC port names to package-pin names) files enhance IC core dynamic IR drop analysis using Cadence VoltageStorm™.

INTEGRATED CONSTRAINT MANAGEMENT

Constraints can either be imported from previous designs or captured early in the design process. The hierarchical, spreadsheet-like interface allows users to ensure package design progresses according to the design intent.

3D DESIGN VIEWER

The Cadence 3D Design Viewer is a full, solid model 3D viewer solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. It provides a common reference point for design reviews.

OTHER SiP DIGITAL SOLUTION PRODUCTS

SiP DIGITAL LAYOUT

This solution is a physical detailed implementation environment for complete SiP substrate place-and-route, final connectivity optimization (IC, substrate, and PCB levels), manufacturing preparation, full design validation, and tapeout.

SiP DIGITAL ARCHITECT

This solution provides the project architect and design team with an environment for the exploration, definition, capture, construction and validation of design concept feasibility prior to final physical detailed implementation. Built around a unique System Connectivity Manager, it provides the architect with a unique environment to explore and define system connectivity/functionality that is optimized between ICs, SiP substrate, and target PCB system.

SPECIFICATIONS

SYSTEM REQUIREMENTS

- OpenGL graphics compliance with a minimum of 64MB of dedicated memory

PLATFORM/OS

- Windows
- Solaris
- Linux
- HP-UX

INTERFACES

- Synopsys HSpice

3RD-PARTY SUPPORT

- Optimal Corporation O-Wave and PowerGrid

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (ILS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

SIP FEATURE SUMMARY

| | SiP Digital Architect GXL | SiP Digital Architect XL | SiP Digital Layout GXL | SiP Digital SI XL | SiP RF Architect XL | SiP RF Layout GXL |
|---|---------------------------|--------------------------|------------------------|-------------------|---------------------|-------------------|
| Front-end Design Creation Features | | | | | | |
| Virtuoso Analog Design Environment, schematic and layout integration & flow | | | | | X | |
| Substrate level embedded RF passive synthesis | | | | | X | |
| System Connectivity Manager | X | X | | | | |
| Full SiP LVS (substrate and IC's) | X | X | | | | |
| Signal Integrity Features | | | | | | |
| SigXplorer topology editor and simulator (pre-route capabilities) | X | | | X | | |
| SigXplorer topology editor and simulator (pre and post route capabilities) | | | | X | | |
| S-parameter interconnect modeling and SI simulation | X | | | X | | |
| 3D PCB package simulation model creation | X | | X | X | | X |
| Quasi-static 3D extraction/modeling engine | X | | | X | | |
| Spectre simulation engine | X | | | X | | |
| Channel analysis for high-capacity SI simulation | X | | | X | | |
| Package/pin delay length report | X | | X | X | | X |
| Substrate Design Features | | | | | | |
| Constraint Manager (Electrical and Physical) | X | X | X | X | | X |
| Export SiP design to .mcm | X | | X | | | X |
| Interactive (i/a) and automatic component (packaged and bare die) placement | X | | X | i/a only | | X |
| Auto/interactive Wirebonding | X | | X | X | | X |
| Full and partial design connectivity assignment and optimization (Router based, closest match and interactive and constraint based) | X | | X | X | | X |
| Interactive and automatic interconnect routing (free angle and multilayer orthogonal) | X | | X | X | | X |
| On-line soldermask checking | | | X | | | X |
| Recursive breakout pattern creator | X | | X | | | X |
| Static style screen rulers | | | | | | X |
| Advanced Design Features | | | | | | |
| I/O Planning co-design editor (using LEF/DEF & OA2.2) | X | | X | | | X |
| Hierarchical GDS2 output | | | X | | | X |
| Embedded RF passive creation and editing | | | | | | X |
| 3D Design Viewer & 3D wirebond DRC | X | | X | X | | X |
| 3D Die Stack Editor | X | | X | | | X |
| Interconnect Cline spreading | | | X | | | X |
| Tiles creation, editing | X | | X | | | X |
| BGA Editor | X | | X | X | | X |
| HDI Via structure support | X | | X | X | | X |
| DFM Preparation/Output | | | | | | |
| Die/BGA footprint compare using DEF/OA.TXT | X | | X | | | X |
| Filled shapes (metal) creation and editing | | | X | X | | X |
| Design documentation such as dimensioning, annotation | | | X | | | X |
| Etch back of plating traces | | | X | | | X |
| Plating bar generation | | | X | | | X |
| Manufacturing / documentation export/import capabilities (stream, dxf, AIF etc) | | | X | | | X |
| Substrate mask output (Gerber, GDS2) | | | X | | | X |
| Full design status reporting capabilities | X | | X | X | | X |
| Waived DRC's (creation and reporting) | X | | X | X | | X |
| Degassing of filled metal shapes | | | X | | | X |
| Thieving (metal area balancing) | | | X | | | X |

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
additional information.