



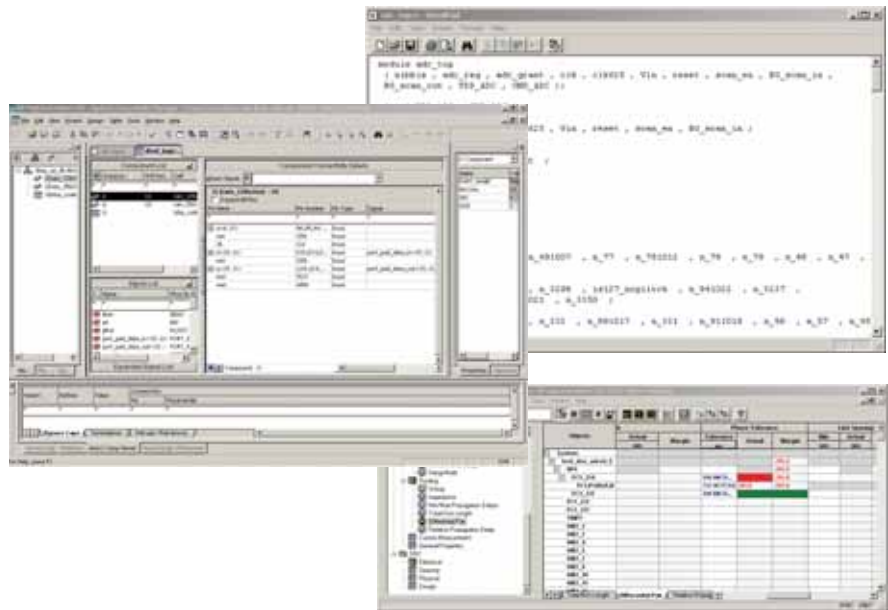
seamlessly integrate into Cadence Encounter® for die abstract co-design, Cadence Virtuoso® for RF module design, and Cadence Allegro® for package/board co-design.

## SIP DIGITAL ARCHITECT

Built around a unique System Connectivity Manager, Cadence SiP Digital Architect provides the architect with a unique environment to explore and define system connectivity/ functionality that is optimized between ICs, SiP package substrate, and target PCB system through concurrent co-design. It allows engineers to perform rapid “what-if” feasibility studies to ensure maximum device functional density performance, while minimizing power consumption. It fully supports IC-driven or package/ board substrate-driven flows with cross-fabric domain engineering change orders (ECO) and layout versus schematic (LVS) validation. As its design focus is predominantly digitally based, analog and/or mixed-signal design content is imported and managed as a hierarchical sub-block.

## BENEFITS

- Allows rapid “what-if” feasibility studies for maximum device functional density, performance, and minimal power consumption
- Enables rapid system-level connectivity capture with ability to bind into alternative physical implementation scenarios to evaluate performance and tradeoffs
- Provides IC I/O padding/array co-design and optimization at the IC, substrate, and system levels



Rapid capture and connectivity is provided by the System Connectivity Manager

## FEATURES

### SYSTEM CONNECTIVITY MANAGER

The System Connectivity Manager is the “cockpit” or “dashboard” of Cadence SiP Digital Architect. It allows the project architect and design team to rapidly capture the connectivity of the SiP—which includes importing IC die Verilog® netlists for chips that comprise the SiP design—and interfacing to the PCB footprint symbol of the completed SiP. For mixed-signal designs, analog/mixed-signal sub-block connectivity can be imported from the Virtuoso environment. A table/spreadsheets-based interface provides a highly productive way to create, import, manage, and validate the connectivity of the complete SiP. By dynamically managing a design’s functional connectivity at the system level, the architect is free to explore unlimited hierarchical fabric binding concepts, including functional partitioning at the IC level. Embedded LVS routines and ECO management capabilities ensure that the logical SiP definition matches the physical SiP implementation, including any ICs that are partitioned and co-designed as part of the SiP.

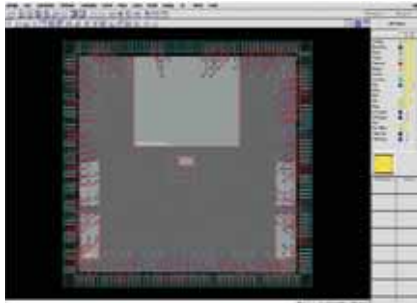
### VIRTUAL SYSTEM INTERCONNECT (VSIC) MODELS

An integrated graphical and topological interconnect modeling and simulation capability provides the architect with the ability to create and explore the signal integrity (SI) performance of proposed system-level connectivity. Such buffer-to-buffer paths can either be extracted from the Connectivity Manager, or constructed on the fly using a graphical canvas and a library of characterized interconnect structures. An embedded simulation capability provides time and frequency domain interconnect simulation, which includes the ability to consume industry-standard S-Parameter models. A full 3D quasi-static field solver provides the extraction and creation of detailed, accurate geometric IBIS, RLGC or S-Parameter models of complex interconnect structures.

### I/O PLANNER

The IC die abstract I/O Planner provides the definition and optimization of co-design die bump matrix, I/O pad ring/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing. It can create either a die abstract from scratch, or load an abstract from the digital IC design

team (LEF/DEF or OA), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O Planner is based on Encounter technology, ensuring it is 100 percent compatible with the chip design team's IC tools and provides complete IC technology file compliance.



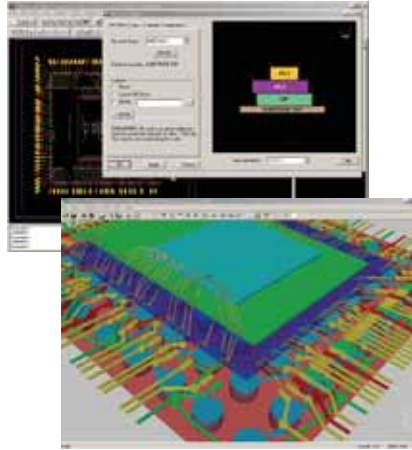
*I/O Planner provides concurrent co-design of IC die pad ring/arrays and package substrate*

### SUBSTRATE FLOORPLANNER

The floorplanner allows the physical prototyping and evaluation of various substrate-level SiP implementation concepts. It provides a full rules-driven, connectivity-based capability that ensures a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data is used to build the physical SiP implementation. The SiP designer can then use the graphical, intuitive editing tools to construct and evaluate critical sections of the design. Typical items for exploration include 3D die stacks using the dedicated Die Stack Editor, wirebonding schemes, die breakout patterns, substrate material options/stackups, and critical signal routing.

### 3D DIE STACK EDITOR

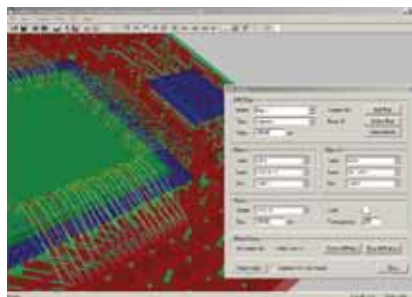
The Die Stack Editor provides a three-dimensional (3D) construction environment for assembling complex die stacks which can include spacers, interposers and die attach methods such as wirebond and flip chip.



*The Die Stack Editor enables accurate 3D stacking and design placement*

### 3D DESIGN VIEWER

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. It provides a common reference point for design reviews.



*3D design viewer and wirebond DRC capability ease design reviews and simplify complex bondshell pattern checking*

## OTHER SiP DIGITAL SOLUTION PRODUCTS

### SiP DIGITAL LAYOUT

This solution is a physical detailed implementation environment for complete SiP substrate place and route, final connectivity optimization (IC, substrate, and PCB levels), manufacturing preparation, full design validation, and tapeout.

### SiP DIGITAL SI

This tightly integrated interconnect SI analysis and modeling solution is built around an SI-focused substrate editor for advanced IC packages. It is architected to handle a range of designs—designs that have a large number of high-speed signals or designs having signals that operate in the multi-gigahertz (MGH) range. For today's serial interface designs (SERDES) it offers complete, integrated S-Parameter support, and fast (10,000 bits in seconds) high-capacity simulation for jitter and bit-error-rate prediction.

## SPECIFICATIONS

### SYSTEM REQUIREMENTS

- OpenGL graphics compliance with a minimum of 64MB of dedicated memory

### PLATFORM/OS

- Windows XP
- Solaris
- Linux
- HP-UX

### INTERFACES

- LEF/DEF 5.1 to 5.6
- OA 2.2
- Verilog
- Virtuoso Schematic Capture (Composer) netlist import (for A/MS sub-blocks)

## SIP FEATURE SUMMARY

	SIP Digital Architect GXL	SIP Digital Architect XL	SIP Digital Layout GXL	SIP Digital SI XL	SIP RF Architect XL	SIP RF Layout GXL
<b>Front-end Design Creation Features</b>						
Virtuoso Analog Design Environment, schematic and layout integration & flow					X	
Substrate level embedded RF passive synthesis					X	
System Connectivity Manager	X	X				
Full SIP LVS (substrate and IC's)	X	X				
<b>Signal Integrity Features</b>						
SigXplorer topology editor and simulator (pre-route capabilities)	X			X		
SigXplorer topology editor and simulator (pre and post route capabilities)				X		
S-parameter interconnect modeling and SI simulation	X			X		
3D PCB package simulation model creation	X		X	X		X
Quasi-static 3D extraction/modeling engine	X			X		
Spectre simulation engine	X			X		
Channel analysis for high-capacity SI simulation	X			X		
Package/pin delay length report	X		X	X		X
<b>Substrate Design Features</b>						
Constraint Manager (Electrical and Physical)	X	X	X	X		X
Export SiP design to .mcm	X		X			X
Interactive (i/a) and automatic component (packaged and bare die) placement	X		X	i/a only		X
Auto/interactive Wirebonding	X		X	X		X
Full and partial design connectivity assignment and optimization (Router based, closest match and interactive and constraint based)	X		X	X		X
Interactive and automatic interconnect routing (free angle and multilayer orthogonal)	X		X	X		X
On-line soldermask checking			X			X
Recursive breakout pattern creator	X		X			X
Static style screen rulers						X
<b>Advanced Design Features</b>						
I/O Planning co-design editor (using LEF/DEF & OA2.2)	X		X			X
Hierarchical GDS2 output			X			X
Embedded RF passive creation and editing						X
3D Design Viewer & 3D wirebond DRC	X		X	X		X
3D Die Stack Editor	X		X			X
Interconnect Cline spreading			X			X
Tiles creation, editing	X		X			X
BGA Editor	X		X	X		X
HDI Via structure support	X		X	X		X
<b>DFM Preparation/Output</b>						
Die/BGA footprint compare using DEF/OA.TXT	X		X			X
Filled shapes (metal) creation and editing			X	X		X
Design documentation such as dimensioning, annotation			X			X
Etch back of plating traces			X			X
Plating bar generation			X			X
Manufacturing / documentation export/import capabilities (stream, dxf, AIF etc)			X			X
Substrate mask output (Gerber, GDS2)			X			X
Full design status reporting capabilities	X		X	X		X
Waived DRC's (creation and reporting)	X		X	X		X
Degassing of filled metal shapes			X			X
Thieving (metal area balancing)			X			X

## CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet— they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom

- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

## FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit [www.cadence.com](http://www.cadence.com) for additional information.