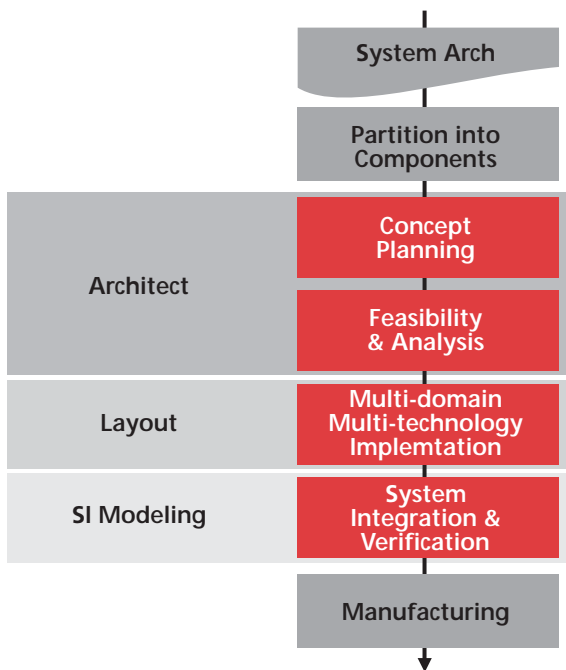


CADENCE SiP RF ARCHITECT

While system-in-package (SiP) design makes it possible to combine RF and analog content on the same substrate, it presents a number of challenges. These include designing and integrating RF/analog chips with substrate-level buried RF passive devices as well as enabling top-level pre- and post-layout circuit simulation of the entire SiP design. Cadence® SiP RF Architect provides the proven path between analog design and simulation and SiP RF layout. It enables designers to create a single, system-level, circuit simulation-ready schematic for RF/analog die, SiP substrate, and packaged and embedded discrettes.



The Cadence SiP design technology provides a methodology, flow and toolset for the definition, implementation, and verification of multi-chip and multi-component IC packages

CADENCE SiP DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of advantages over SoC. In addition to reduced cost, lower power, and higher performance, SiP design offers the flexibility to mix RF and high-speed digital circuitry in the same package. However, this also means it requires expert engineering talent in widely divergent fields. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate. This approach allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions

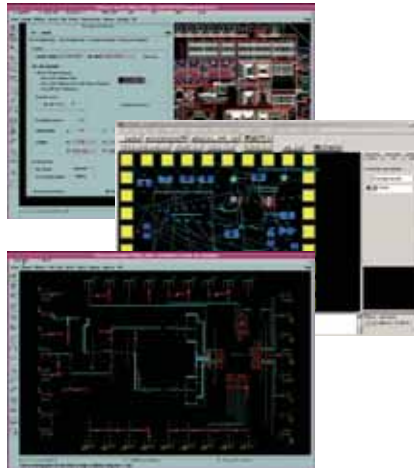
seamlessly integrate into Cadence Encounter® for die abstract co-design, Cadence Virtuoso® for RF module design, and Cadence Allegro® for package/board co-design.

SIP RF ARCHITECT

SiP RF Architect provides the integration and flow environment between the Virtuoso Analog Design Environment (ADE) and the SiP RF Layout solution. It enables the creation of a single, circuit-simulation-capable, top-level SiP RF module schematic that includes the RF/analog ICs that are part of the final SiP design. It also provides schematic-level pre-layout definition and characterization of substrate-level embedded RF passive devices and a bi-direction engineering change order (ECO) and layout versus simulation (LVS) flow between the substrate layout and the Virtuoso ADE environment. RF/Analog ICs can be exported from the Virtuoso Layout Editor as design-ready SiP die footprints that include post-wafer processing geometry adjustments.

BENEFITS

- Provides a single, top-level Virtuoso schematic and simulation driven environment for RF ICs, SiP RF module substrate, and embedded RF passive elements
- Supports bi-directional ECO and LVS flow between RF design team and SiP RF module layout team
- Supports substrate-level RF Passive parameterized cell (P-cell) creation via Virtuoso top-level design
- Speeds design with direct export of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Provides rapid adoption path via RF SiP Methodology Kit for wireless application implementation



An integrated RF SiP design flow

FEATURES

INTEGRATED FLOW

SiP RF Architect provides a single integrated design flow built around the Virtuoso DFII framework. It also provides a single, system-level, simulation-ready Virtuoso schematic for RF/analog die, SiP substrate, and packaged and embedded discretives. It allows direct export of SiP-level IC die footprints from Virtuoso Layout Editor and schematic-driven substrate level RF P-cell creation.

OTHER SiP SOLUTION PRODUCTS

SiP RF LAYOUT

This physical detailed implementation environment for complete SiP RF substrate place and route includes final connectivity optimization; die stack creation; support for flip-chip and wirebond attach die; RF embedded passive creation and optimization; manufacturing preparation; and full design validation and tapeout.

SiP DIGITAL SI

This tightly integrated interconnect signal integrity analysis and modeling solution is built around an SI-focused substrate editor for advanced IC packages. It is designed to handle a variety of designs—from one that have a large number of high-speed signals to those having signals that

operate in the multi-gigahertz (MGH) range. For today's serial interface designs (SERDES), it offers complete, integrated S-Parameter support and fast (10,000 bits in seconds) high-capacity simulation for jitter and bit-error-rate prediction.

SPECIFICATIONS

SYSTEM REQUIREMENTS

PLATFORM/OS

- Solaris
- Linux
- HP-UX

INTERFACES

- LEF/DEF 5.1 to 5.6

VIRTUOSO COMPATIBILITY

- CIC-4.x to 5.x

3RD-PARTY SUPPORT

- Agilent RFDE (ADS and MoMentum) for pre- and post- layout extraction and simulation

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet— they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

SIP FEATURE SUMMARY

| | SIP Digital Architect GXL | SIP Digital Architect XL | SIP Digital Layout GXL | SIP Digital SI XL | SIP RF Architect XL | SIP RF Layout GXL |
|-------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------------|------------------------|-------------------|---------------------|-------------------|
| Front-end Design Creation Features | | | | | | |
| Virtuoso Analog Design Environment, schematic and layout integration & flow | | | | | X | |
| Substrate level embedded RF passive synthesis | | | | | X | |
| System Connectivity Manager | X | X | | | | |
| Full SIP LVS (substrate and IC's) | X | X | | | | |
| Signal Integrity Features | | | | | | |
| SigXplorer topology editor and simulator (pre-route capabilities) | X | | | X | | |
| SigXplorer topology editor and simulator (pre and post route capabilities) | | | | X | | |
| S-parameter interconnect modeling and SI simulation | X | | | X | | |
| 3D PCB package simulation model creation | X | | X | X | | X |
| Quasi-static 3D extraction/modeling engine | X | | | X | | |
| Spectre simulation engine | X | | | X | | |
| Channel analysis for high-capacity SI simulation | X | | | X | | |
| Package/pin delay length report | X | | X | X | | X |
| Substrate Design Features | | | | | | |
| Constraint Manager (Electrical and Physical) | X | X | X | X | | X |
| Export SiP design to .mcm | X | | X | | | X |
| Interactive (i/a) and automatic component (packaged and bare die) placement | X | | X | i/a only | | X |
| Auto/interactive wirebonding | X | | X | X | | X |
| Full and partial design connectivity assignment and optimization (Router based, closest match and interactive and constraint based) | X | | X | X | | X |
| Interactive and automatic interconnect routing (free angle and multilayer orthogonal) | X | | X | X | | X |
| On-line soldermask checking | | | X | | | X |
| Recursive breakout pattern creator | X | | X | | | X |
| Static style screen rulers | | | | | | X |
| Advanced Design Features | | | | | | |
| I/O Planning co-design editor (using LEF/DEF & OA2.2) | X | | X | | | X |
| Hierarchical GDS2 output | | | X | | | X |
| Embedded RF passive creation and editing | | | | | | X |
| 3D Design Viewer & 3D wirebond DRC | X | | X | X | | X |
| 3D Die Stack editor | X | | X | | | X |
| Interconnect cline spreading | | | X | | | X |
| Tiles creation, editing | X | | X | | | X |
| BGA Editor | X | | X | X | | X |
| HDI via structure support | X | | X | X | | X |
| DFM Preparation/Output | | | | | | |
| Die/BGA footprint compare using DEF/OA.TXT | X | | X | | | X |
| Filled shapes (metal) creation and editing | | | X | X | | X |
| Design documentation such as dimensioning, annotation | | | X | | | X |
| Etch back of plating traces | | | X | | | X |
| Plating bar generation | | | X | | | X |
| Manufacturing / documentation export/import capabilities (stream, dxf, AIF etc) | | | X | | | X |
| Substrate mask output (Gerber, GDS2) | | | X | | | X |
| Full design status reporting capabilities | X | | X | X | | X |
| Waived DRCs (creation and reporting) | X | | X | X | | X |
| Degassing of filled metal shapes | | | X | | | X |
| Thieving (metal area balancing) | | | X | | | X |

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
additional information.