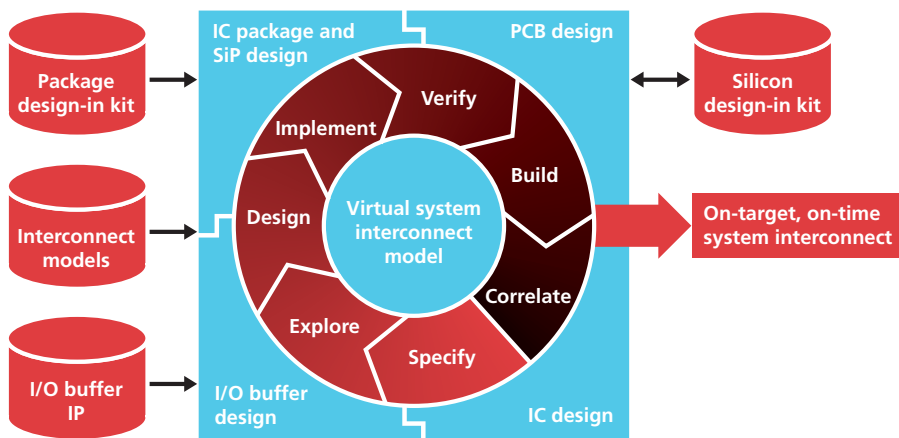


ALLEGRO PCB ROUTER L, XL

The Cadence® Allegro® PCB Router routing environment is the leading solution for automatic and interactive interconnect routing for printed circuit boards (PCBs). Designed to handle routing challenges from simple designs to high-density PCBs requiring complex, high-speed design rules, it uses powerful shape-based algorithms to make the most efficient use of the routing area. The results are increased completion rates, higher productivity, and shortened design cycle times.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

INTERCONNECT ENVIRONMENT

Increased design complexity, density, and high-speed routing constraints make manual routing of PCBs difficult as well as time-consuming. Allegro PCB Router solves the challenges of complex interconnect routing with powerful, automated technology. This robust, production-proven autorouter includes a batch routing mode with extensive routing strategy control and built-in automatic strategy capability. Its high-speed routing features provide capabilities to handle the net scheduling, timing, crosstalk, layer set routing, and special geometry requirements demanded by today's high-speed circuits. An interactive routing environment—that features real-time interactive trace pushing and shoving—aids in making quick manual edits to traces. An interactive placement environment with extensive floorplanning functionality and complete component placement features eliminates the need to switch applications to make placement changes. By using the auto-interactive floorplanning and placement capability, designers can improve routing quality and productivity, which are directly related to component placement. In addition, an extensive rule set allows designers to control a wide range of constraints from default board-level rules to rules by net/net class, and regions rules.

BENEFITS

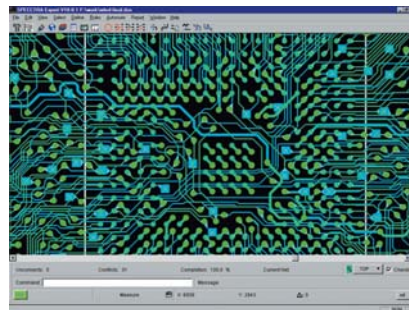
- Provides a scalable, cost-effective, proven interconnect solution
- Offers a complete interconnect environment including floorplanning and routing
- Speeds design with high-speed rules/constraint routing for delay, crosstalk, impedance control, differential pairs, and net scheduling—including virtual pins
- Includes a comprehensive feature set
- Reduces route-fix-route iterations
- Allows shape-based, 45-degree, interactive, and automatic routing

FEATURES

AUTOROUTING

Allegro PCB Router provides powerful, shape-based autorouting with fast, high completion rates. Its routing algorithms are designed to handle a wide range of PCB interconnect challenges—from simple to complex, low density to high density—as well as the demands of high-speed constraints. These powerful algorithms make the most efficient use of the routing area. To find the best routing solution for each case, Allegro PCB Router uses a multipass, cost-based conflict resolution algorithm.

An extensive rule set provides the capability for physical and electrical constraint control. Allegro PCB Router's rule set has the flexibility to handle specific rules on various routing elements in a design. Users define rules required to meet the common physical net rules and class rules to complex, hierarchical high-speed rules.



Allegro PCB Router effectively handles dense, highly constrained, multilayer designs

HIGH-SPEED CONSTRAINTS

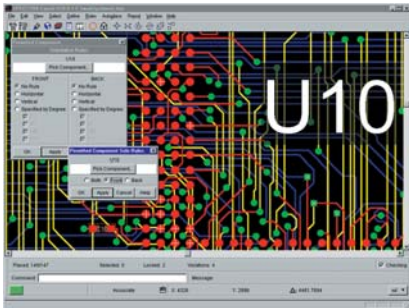
High-speed routing constraints handle differential pairs, net scheduling, timing, crosstalk, layer set routing, and the special geometry requirements demanded by today's high-speed circuits. For differential pair routing, users define the gap between the two conductors and the autorouter takes care of the rest. Allegro PCB Router intelligently handles routing around or through vias and automatically conforms to defined length or timing criteria. Automatic net shielding is used to reduce noise on noise-sensitive nets. Separate design rules may be applied to different regions of the design. For example, users can specify tight clearance rules in the connector area of a design and less stringent rules elsewhere.

DESIGN FOR MANUFACTURING

The design for manufacturing capability provided by Allegro PCB Router significantly improves manufacturing yields with a spread command that automatically increases conductor clearances on a space-available basis. It also automatically miters corners and adds test points after autorouting. Automatic conductor spreading is used to improve manufacturability by repositioning conductors to create extra space between conductors and pins, conductors and SMD pads, and adjacent conductor segments. Users have the flexibility to define a range of spacing values or to use the default values. Mitered corners automatically replace 90-degree corners with a chamfer by using either the default or a user-specified setback value. Allegro PCB Router enables designers to miter corners throughout the design, or on specific layers, and specify a single value or a range of setback values. The design for manufacturing capability automatically uses the optimal setback within the range, starting from the largest to the smallest value.

TEST POINT INSERTION

Test point insertion automatically adds testable vias or pads as test points. Testable vias can be probed on the front, back, or both sides of the PCB, supporting both single side and clamshell testers. Designers have the flexibility to select the test point insertion methodology that conforms to their manufacturing requirements. Test points can be “fixed” to avoid costly test fixture modifications. Test point constraints include test probe surfaces, via sizes, via grids, and minimum center-to-center distance.



Allegro PCB Router is a complete interconnect environment offering interactive and automatic component floorplanning as well as shape-based, 45-degree, interactive, and automatic routing

INTERACTIVE ROUTE EDITOR

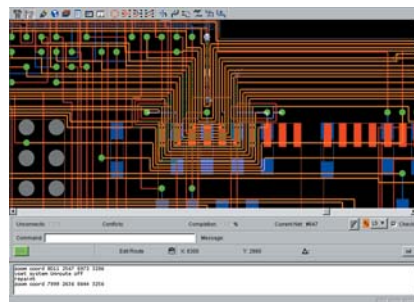
The fully integrated Route Editor simplifies and streamlines the editing process. As new conductors are routed, the plowing feature automatically pushes aside existing conductors and routes around pins. Using the shoving feature, designers can move conductor segments or vias against existing traces and push ahead over other pins and vias if necessary. A ghosting feature makes it easy to evaluate “what if” scenarios. As a conductor segment or via is moved under cursor control, the surrounding conductor is shoved and displayed dynamically so the adjusted routing can be evaluated before accepting a final configuration.

The Route Editor is ideal for dense, multilayer boards where legal via sites can be difficult to find. Vias are positioned by simply clicking twice at a chosen location. If possible, the chosen site is made available by shoving conductors aside on layers as needed.

If not, the Route Editor displays a design rule violation and shows the legal via sites nearby. In addition, the copyroute feature, which allows an existing route to be copied to complete unrouted bus connections, simplifies bus construction.

PLACEMENT EDITOR

The Placement Editor allows designers to quickly place components while simultaneously evaluating space, logic flow, and congestion before beginning to route a PCB. The Move mode allows components to be flipped, rotated, aligned, pushed, and moved either as individual components or as a group. The Guided-Place mode selects the component with the highest connectivity and computes an optimal placement location that does not violate design rules or constraints. The location can be accepted or rejected by the user. Components can be placed by directly entering their X-Y locations. This capability is particularly useful for placing connectors and components with fixed locations. Density analysis graphically displays circuit congestion by overlaying the PCB with a color map showing a range of areas—from highly congested areas to lightly congested. This helps determine where placement adjustments could be made to relieve congestion and improve routing completion.



Dynamic push-and-shove capabilities make interactive editing easy, even on the most advanced designs

ALLEGRO PCB EDITOR INTEGRATION

The Allegro PCB Router is tightly integrated with the Allegro PCB Editor. Through the PCB Editor interface, all design information and constraints are automatically passed to Allegro PCB Router. Once the route is

completed, all route information is automatically passed back to the Allegro PCB Editor.

OPERATING SYSTEM SUPPORT

- Red Hat Linux 3.0, 4.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9, 10
- HP-UX 11.11i
- IBM AIX 5.3

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

ALLEGRO PCB ROUTER FEATURE SUMMARY FOR PCB DESIGN

	PCB Design L Series	PCB Design L Series Options	PCB Design XL Series
ALLEGRO PCB ROUTER FEATURES			
6 Signal Layer Limit	x		
256 Signal Layer Limit		Router Auto/Interactive	x
Shape-based or Gridded Autorouting	x		x
SMD Fanout to Vias	x		x
Trace Width by Net and Net Classes	x		x
Staggered Pin Support	x		x
45-degree ECO Routing	x		x
Memory Pattern Routing (SMD or Through-hole)	x		x
Interactive Via Search	x		x
Interactive Routing with Shoving and Plowing	x		x
Interactive Floorplanning	x		x
Autoplacement			x
Online Design Rule Checking	x		x
Flip, Rotate, Align, Push, and Move Components	x		x
Placement Density Analysis	x		x
Router Support for PCB Design Partitioning Files	x		x
PCB Router ADV 6U or 256U		Router Performance*	x
Layer Set Rules and Routing Support		Router Performance*	x
Signals on Specific Layers		Router Performance*	x
Width and Clearance Rules by Layer		Router Performance*	x
Via Rules by Net and/or Net Class		Router Performance*	x
Net and/or Net Class Rules by Layer		Router Performance*	x
Crosstalk Violation Report		Router Performance*	x
Trace Length Violation Report		Router Performance*	x
Blind and Buried Via Support		Router Performance*	x
Via Under SMD Pad Checking		Router Performance*	x
Automatic Wire Bonding		Router Performance*	x
Plural Vias		Router Performance*	x
Stacked Vias		Router Performance*	x
Enhanced Via Fanout		Router Performance*	x
PCB Router DFM 6U or 256U		Router Performance*	x
Automatic Trace Spreading		Router Performance*	x
Automatic Via Reduction		Router Performance*	x
Automatic Miter 90 to 45		Router Performance*	x
Automatic Test Point Generation		Router Performance*	x
Test Point Specific Clearance Rules		Router Performance*	x
PCB Router HP 6U or 256U		PCB Performance	x
Minimum, Maximum, and Matched Length Rules		PCB Performance	x
Crosstalk Controls on Same and Adjacent Layers		PCB Performance	x
Virtual Pins, Which can be Moved During Autorouting		PCB Performance	x
Parallelism Controlled by Length and Gap		PCB Performance	x
Differential Pair Routing		PCB Performance	x
Automatic Net Shielding		PCB Performance	x
Design Rules by Area		PCB Performance	x
Online Display of Length Tolerance		PCB Performance	x
Global Violation Indicator		PCB Performance	x
Dynamic Display of Available Length		PCB Performance	x
Automatic Single Net Routing		PCB Performance	x
Multiple Net/Bus Routing		PCB Performance	x
Relative Delay Rules		PCB Performance	x
Z-Axis Delay Support (PCB Editor Integration Only)		PCB Performance	x
Extended Timing Path Support (PCB Editor Integration Only)		PCB Performance	x
Pin-pair Multi/Matched Nested Group Support (PCB Editor Integration Only)		PCB Performance	x

* Router Auto/Interactive Required

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
additional information. To locate a
Cadence sales office or Cadence
Channel Partner in your area, visit
www.cadence.com/contact_us