

# TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

<b>Course Title</b>	<b>Allegro PCB SI Foundations v16.3</b>
<b>Course Category</b>	<b>System Interconnect Design – Allegro &amp; OrCAD</b>
<b>Duration</b>	<b>2 Days</b>
<b>Course ID</b>	<b>ES_86046_16.3</b>
<b>Product Version</b>	<b>16.3</b>

## Course Description

In this course, you use the Allegro® PCB SI XL software to develop design rules for high-speed designs. You add the resulting physical and electrical constraints to the design through topology templates. These constraints drive the routing of nets on the printed circuit board. You run preroute and postroute signal simulations to analyze the PCB for reflection, simultaneous switching, crosstalk, and other high-speed design factors.

## Learning Objectives

After completing this course, you will be able to:

- o Create, extract, and explore topologies
- o Run solution space analysis
- o Create an electrical constraint set
- o Apply constraints to drive placement and routing
- o Run postroute DRC check
- o Use template revision to update the ECSet applied to the nets
- o Analyze the routed board design for signal integrity
- o Create a DesignLink between boards and use it to run multiboard simulation

## Software Used in This Course

- o Allegro PCB SI - XL

## Software Release(s)

- o SPB 16.3

## Audience

- o Electrical Engineers
- o PCB Designers

## Prerequisites

You must have

- o A familiarity with digital and analog circuit design methodology
- o A working knowledge of PCB signal analysis and transmission line theory

## Course Agenda

*Note that this course can be tailored to better meet your needs – [contact the Cadence training staff](#) for specifics.*

### Day 1

- o Allegro PCB SI design flow
- o Board setup requirements
- o DC net connections
- o Model assignment
- o Default and discrete models
- o Model integrity
- o IBIS to DML translation
- o Net extraction
- o SigXplorer basics
- o Simulation with SigXplorer
- o Sweep simulations
- o Trace models

### Day 2

- o Constraint floorplanning
- o Constraint DRCs
- o DRC routing
- o Creating a DesignLink
- o System analysis
- o Postroute analysis
- o Reflection and crosstalk simulation
- o Postroute bus analysis
- o Differential pairs

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## Related Courses

- [Allegro High-Speed Constraint Management v16.3](#)
- [Allegro PCB Editor Intermediate Techniques v16.3](#)