

# TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

<b>Course Title</b>	<b>Allegro Design Reuse v16.2</b>
<b>Course Category</b>	<b>System Interconnect Design – Allegro &amp; OrCAD, Advance with Engineer Explorer Series</b>
<b>Duration</b>	<b>1 Day</b>
<b>Course ID</b>	<b>ES_86083_16.2</b>
<b>Product Version</b>	<b>16.2</b>

## Course Description

Design Reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse. Any EDA user who has time-to-market pressures will benefit from Design Reuse. Design Reuse adds scalability and modularity to your design process, saving time and reducing error by facilitating the reuse of known good IP.

## Learning Objectives

After completing this course, you will be able to:

- o Create a subdesign state file
- o Create a layout module file
- o Document and store the reuse design
- o Use properties to control reuse packaging
- o Work with hierarchical constraints
- o Make changes to subdesigns while in reuse
- o Customize packaging with Occurrence Edit
- o Apply reuse methodology to existing (flat) designs
- o Use macros and parameters
- o Search for related solutions on Cadence Online Support (COS)

## Software Used in This Course

- o Allegro PCB Design HDL - XL

## Software Release(s)

- o SPB 16.2

## Course Agenda

*Note that this course can be tailored to better meet your needs – [contact the Cadence training staff](#) for specifics.*

### Day 1

- o Exploring a Design Reuse Example
- o Creating a Reusable Block
- o Reusing the Block in Other Designs
- o Managing Changes
- o Advanced Topics
- o Summary and Conclusion

## Audience

- o Engineering Managers
- o PCB Designers
- o Design Engineers

## Prerequisites

You must have experience with or knowledge of the following:

- o Allegro® Design Entry HDL and PCB Editor tools. This course does not teach basic tool operations.
- o Hierarchical design and the need to reuse logical blocks and associated part placement and signal routing.

Or you must have completed the following courses:

- o Allegro Design Entry HDL Front-to-Back Flow

## Related Courses

- [Allegro Design Entry HDL Front-to-Back Flow v16.3](#)