

TRAINING

Bei dem hier beschriebenen Training handelt es sich um ein Cadence Standard Training. Sie erhalten eine Dokumentation in englischer Sprache. Die Trainingssprache ist deutsch, falls nicht anders angekündigt.

Course Title	Allegro Package Designer v16.5
Course Category	System Interconnect Design – Allegro & OrCAD
Duration	4 Days
Course ID	ES_85022_16.5
Product Version	16.5

Course Description

In this course, you use the Allegro® Package Designer system for the design and specification of manufacturing single-chip modules for single-, double-, or multilayered analog and digital packages.

Learning Objectives

After completing this course, you will be able to:

- Develop a process flow to suit your design needs
- Create a cross section and design constraints in your package designer database
- Create bond pads and blind and buried pad stacks
- Construct single-chip module connectivity
- Use interactive routing techniques to route a design
- Output manufacturing data in Gerber or GDSII format, as well as create manufacturing documentation

Software Used in This Course

- Allegro Package Designer - L

Software Release(s)

- SPB16.5

Audience

- This course is intended for Package SCM designers and design engineers.

Prerequisites

You must have experience with or knowledge of the following:

- Single or multichip design and construction
- Foundry design guidelines
- UNIX, Linux, or Windows operating system

Course Agenda

Note that this course can be tailored to better meet your needs – [contact the Cadence training staff](#) for specifics.

Day 1

- Environment
- Library Structure
- Constraints
- Technology Files
- Importing Netlists

Day 2

- Power and Ground Plane Creation
- Placement
- Bond Wiring

Day 3

- Pin and Net Assignment
- Edit Net Logic

Day 4

- Routing
- Vendor Preparation
- Manufacturing Output