

Allegro PCB Power Delivery Network Analysis

An integrated design and analysis environment for faster development of power-optimized PCBs

Cadence® Allegro® PCB Power Delivery Network (PDN) Analysis allows you to quickly find and fix power-related issues throughout the design process and speed PDN closure. Tight integration with Allegro PCB Designer enables you to rapidly modify the design and move quickly through analysis iterations—free from tedious and error-prone translations. Using this unified environment, you can create power guidelines early in the design process, make changes on-the-fly, and optimize the PCB stack-up to maximize electrical performance while minimizing costs.

Allegro PCB PDN Analysis

Power delivery network (PDN) analysis is a critical component of contemporary PCB design. Higher frequency designs being powered by lower voltages leaves little margin for IR drop or ground bounce. These issues are further challenged by the need to reduce PCB costs by decreasing layer count and minimizing board size, coupled with market demand for boards shaped to fit inside stylish and ergonomic enclosures.

PCB designers and electrical engineers can now benefit from a tightly integrated Allegro PCB Designer and PCB PDN analysis environment, which enables rapid design modification and analysis iterations without having to go through time-consuming and error-prone translations. This unified design and analysis environment lets you work early in the design process (pre-netlist) to create abstract plane definitions with virtual source and sink components, to create plane design guidelines, and to optimize the PCB stack-up.

Post-layout analysis provides accurate modeling of the details of carved-up power and ground planes. Impedance

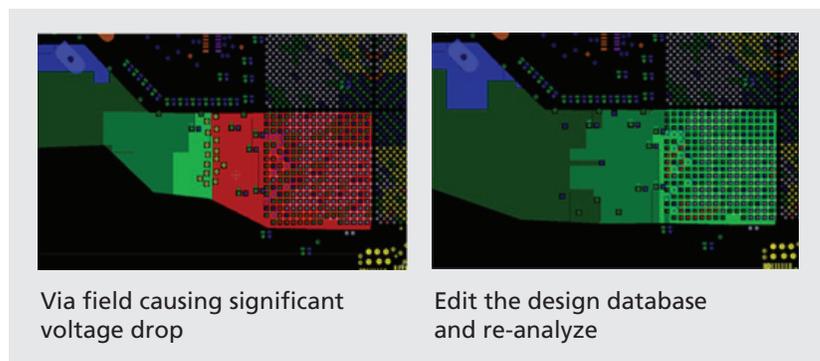


Figure 1: When Allegro PCB PDN analysis technology finds a power integrity problem, the design can be edited and re-analyzed without any design translation required speeding the time to PDN closure

is measured at all power and ground planes, ensuring that stable and sufficient power can be delivered efficiently. Any modifications required to the post-route design can be tested on-the-fly without translation, allowing you to achieve PDN closure in compressed PCB design development schedules.

Benefits

- Provides an accurate full-wave solver for planes
- Easy pre-netlist analysis guides plane design and optimizes PCB stack-up

- Voltage drop combined with current vectors helps identify problem areas
- Analyzes impedance for every power and ground pin on the PCB
- Optimizes decoupling capacitor values and locations
- Integrates seamlessly with Allegro PCB design and signal integrity analysis environments

Features

Static IR drop analysis

The tightly integrated design and analysis environment allows for identification of power delivery issues that have the potential to damage board-level components due to excessive IR drop. Graphical depiction of the changes in voltage, current, and temperature will guide you to any potential “hotspots” on the PCB. Current vectors graphically guide you to potential current return-path problems.

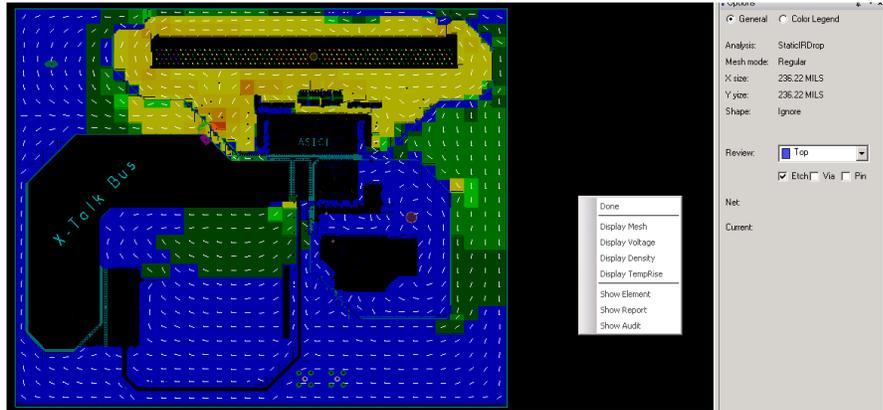


Figure 2: Graphical representation of voltage drop, temperature rise, and current density guide engineers to PDN problem areas

Pre-netlist power plane analysis

Early in the design process, abstract power and ground shapes can be created and virtual power source and sink components can be placed to provide early insight into PDN planning. From the early analysis, design guidelines can be created and the PCB stack-up can be optimized. Leveraging the power of Allegro PCB Designer editing tools available to you, you can add as much detail as desired during early analysis.

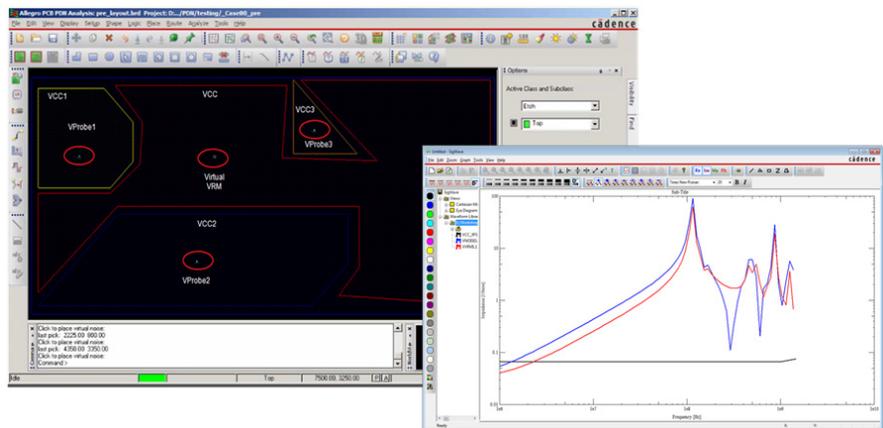


Figure 3: Using abstract power and ground shapes, virtual power and ground component pins, and a virtual VRM, early what-if analysis can be performed before a netlist is available to optimize the PCB stackup and guide final PCB PDN design

Power delivery network analysis

As components and the netlist are added to the board, PDN analysis can be run throughout the design implementation process to ensure that potential problems are caught early. PDN analysis enables impedance calculations at every pin connected to power and ground. Resonant frequencies can be identified and validated that they do not interfere with the PCB operating frequency. Decoupling capacitor values and locations can be optimized, ensuring that the cost of the PCB is minimized while PDN performance meets specifications.

- What-if PDN analysis (edit the design and re-analyze it, without translation)
- Make edits to the PDN and commit them to the final PCB design (no translation required)
- Optimize decoupling capacitor values and locations
- Adjust and commit an optimized stack-up to the final PCB design (no translation required)
- Create text or graphical (2D or 3D) impedance profile reports for the PDN

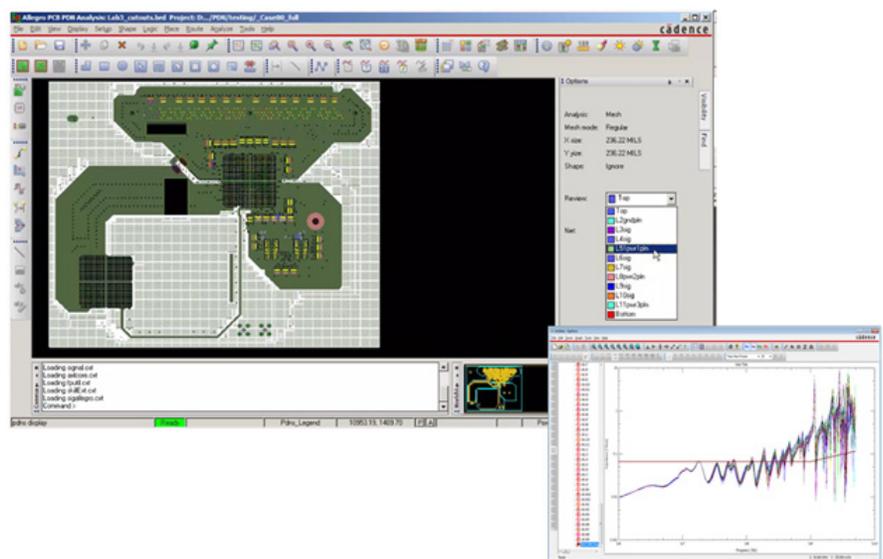


Figure 4: Using integrated full-wave field solver technology, complex power and ground shapes are accurately modeled and analyzed to insure sufficient and stable power is delivered to all PCB components

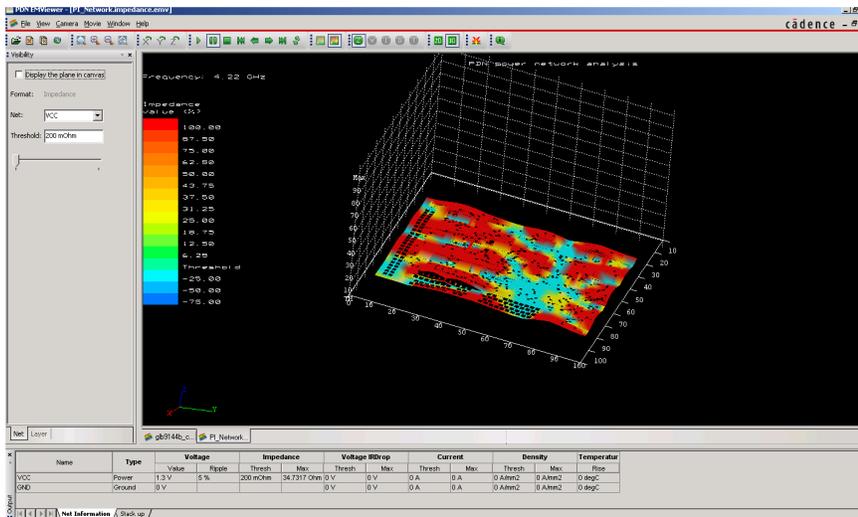


Figure 5: The integrated 3D EM Viewer shows analysis results at a single frequency or animates the results of multiple frequencies

3D visualization

Understanding and documenting your analysis results is best done with a 3D representation. Allegro PCB PDN Analysis includes a 3D EM Viewer that provides 3D visualization of meshing details, impedance results, IR drop results, and voltage ripple across the PCB. Animation is provided to see how these results differ across multiple frequencies.

To verify PDN closure, a threshold plane can be inserted to see if the results exceed or drop below the threshold at any point. Worst-case results can be displayed on a layer-by-layer basis.

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